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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	70
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f8627t-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- Fail-Safe Clock Monitor: This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

### 1.1.4 EXTERNAL MEMORY INTERFACE

In the unlikely event that 128 Kbytes of program memory is inadequate for an application, the PIC18F8527/8622/8627/8722 members of the family also implement an external memory interface. This allows the controller's internal program counter to address a memory space of up to 2 Mbytes, permitting a level of data access that few 8-bit devices can claim.

With the addition of new operating modes, the external memory interface offers many new options, including:

- Operating the microcontroller entirely from external memory
- Using combinations of on-chip and external memory, up to the 2-Mbyte limit
- Using external Flash memory for reprogrammable application code or large data tables
- Using external RAM devices for storing large amounts of variable data

### 1.1.5 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also aids in migrating to the next larger device. This is true when moving between the 64-pin members, between the 80-pin members, or even jumping from 64-pin to 80-pin devices.

### 1.2 Other Special Features

- Communications: The PIC18F8722 family incorporates a range of serial communication peripherals, including 2 independent Enhanced USARTs and 2 Master SSP modules capable of both SPI and I<sup>2</sup>C (Master and Slave) modes of operation. Also, one of the general purpose I/O ports can be reconfigured as an 8-bit Parallel Slave Port for direct processor-to-processor communications.
- CCP Modules: All devices in the family incorporate two Capture/Compare/PWM (CCP) modules and three Enhanced CCP (ECCP) modules to maximize flexibility in control applications. Up to four different time bases may be used to perform several different operations at once. Each of the three ECCP modules offer up to four PWM outputs, allowing for a total of 12 PWMs. The ECCPs also offer many beneficial features, including polarity selection, Programmable Dead-Time, Auto-Shutdown and Restart and Half-Bridge and Full-Bridge Output modes.
- Self-Programmability: These devices can write to their own program memory spaces under internal software control. By using a bootloader routine located in the protected boot block at the top of program memory, it becomes possible to create an application that can update itself in the field.
- Extended Instruction Set: The PIC18F8722 family introduces an optional extension to the PIC18 instruction set, which adds 8 new instructions and an Indexed Addressing mode. This extension, enabled as a device configuration option, has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as C.
- **10-bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduce code overhead.
- Extended Watchdog Timer (WDT): This enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See Section 28.0 "Electrical Characteristics" for time-out periods.

Din Nome	Pin Number	Pin	Buffer	Description			
Pin Name	TQFP	Туре	Туре	Description			
				PORTA is a bidirectional I/O port.			
RA0/AN0 RA0 AN0	30	I/O I	TTL Analog	Digital I/O. Analog input 0.			
RA1/AN1 RA1 AN1	29	I/O I	TTL Analog	Digital I/O. Analog input 1.			
RA2/AN2/VREF- RA2 AN2 VREF-	28	I/O I I	TTL Analog Analog	Digital I/O. Analog input 2. A/D reference voltage (low) input.			
RA3/AN3/VREF+ RA3 AN3 VREF+	27	I/O I I	TTL Analog Analog	Digital I/O. Analog input 3. A/D reference voltage (high) input.			
RA4/T0CKI RA4 T0CKI	34	I/O I	ST/OD ST	Digital I/O. Open-drain when configured as output. Timer0 external clock input.			
RA5/AN4/HLVDIN RA5 AN4 HLVDIN	33	I/O I I	TTL Analog Analog	Digital I/O. Analog input 4. High/Low-Voltage Detect input.			
RA6				See the OSC2/CLKO/RA6 pin.			
RA7			See the OSC1/CLKI/RA7 pin.				
Legend: $TTL = TTL c$ ST = Schmin I = Input P = Power	ompatible input itt Trigger input	CMC with CN O I <sup>2</sup> C™	DS IOS levels //SMB	= CMOS compatible input or output evels Analog= Analog input = Output 3 = I <sup>2</sup> C/SMBus input buffer			
Note 1: Alternate assi Microcontrolle	<b>lote 1:</b> Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode)						

### TABLE 1-4: PIC18F8527/8622/8627/8722 PINOUT I/O DESCRIPTIONS (CONTINUED)

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

3: Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

4: Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

5: Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

### TABLE 5-3: REGISTER FILE SUMMARY

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
TOSU	— — Top-of-Stack Upper Byte (TOS<20:16>)								0 0000	57, 66
TOSH	Top-of-Stack High Byte (TOS<15:8>)								0000 0000	57, 66
TOSL	Top-of-Stack	Low Byte (TOS	S<7:0>)						0000 0000	57, 66
STKPTR	STKFUL <sup>(6)</sup>	STKUNF <sup>(6)</sup>	—	SP4	SP3	SP2	SP1	SP0	00-0 0000	57, 67
PCLATU	—	—	—	Holding Regi	ster for PC<20	:16>			0 0000	57, 66
PCLATH	Holding Regis	ster for PC<15	:8>						0000 0000	57, 66
PCL	PC Low Byte	(PC<7:0>)							0000 0000	57, 66
TBLPTRU	—	—	bit 21 <sup>(7)</sup>	Program Mer	nory Table Poi	nter Upper By	te (TBLPTR<2	0:16>)	00 0000	57, 90
TBLPTRH	Program Men	nory Table Poi	nter High Byte	(TBLPTR<15	:8>)				0000 0000	57, 90
TBLPTRL	Program Men	nory Table Poi	nter Low Byte	(TBLPTR<7:0	>)				0000 0000	57, 90
TABLAT	Program Men	nory Table Late	ch						0000 0000	57, 90
PRODH	Product Regis	ster High Byte							xxxx xxxx	57, 117
PRODL	Product Regis	ster Low Byte							xxxx xxxx	57, 117
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INTOIE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	57, 121
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	INTEDG3	TMR0IP	INT3IP	RBIP	1111 1111	57, 122
INTCON3	INT2IP	INT1IP	INT3IE	INT2IE	INT1IE	INT3IF	INT2IF	INT1IF	1100 0000	57, 123
INDF0	Uses contents	s of FSR0 to a	ddress data m	iemory – value	e of FSR0 not o	changed (not a	a physical regi	ster)	N/A	57, 82
POSTINC0	Uses contents	s of FSR0 to a	ddress data m	iemory – value	of FSR0 post	-incremented	(not a physica	register)	N/A	57, 82
POSTDEC0	Uses contents of FSR0 to address data memory – value of FSR0 post-decremented (not a physical register)							al register)	N/A	57, 82
PREINC0	Uses contents	s of FSR0 to a	ddress data m	emory – value	of FSR0 pre-	incremented (I	not a physical	register)	N/A	57, 82
PLUSW0	Uses contents value of FSR	s of FSR0 to a 0 offset by W	ddress data m	emory – value	e of FSR0 pre-	incremented (I	not a physical	register) –	N/A	57, 82
FSR0H	—	—	—	—	Indirect Data	Memory Addre	ess Pointer 0 H	ligh	0000	57, 82
FSR0L	Indirect Data	Memory Addre	ess Pointer 0 L	ow Byte					xxxx xxxx	57, 82
WREG	Working Regi	ster							xxxx xxxx	57
INDF1	Uses contents	s of FSR1 to a	ddress data m	iemory – value	e of FSR1 not o	changed (not a	a physical regi	ster)	N/A	57, 82
POSTINC1	Uses contents	s of FSR1 to a	ddress data m	iemory – value	e of FSR1 post	-incremented	(not a physica	register)	N/A	57, 82
POSTDEC1	Uses contents	s of FSR1 to a	ddress data m	iemory – value	e of FSR1 post	-decremented	(not a physica	al register)	N/A	57, 82
PREINC1	Uses contents	s of FSR1 to a	ddress data m	iemory – value	of FSR1 pre-	incremented (I	not a physical	register)	N/A	57, 82
PLUSW1	Uses contents value of FSR	s of FSR1 to a 1 offset by W	ddress data m	emory – value	e of FSR1 pre-	incremented (I	not a physical	register) –	N/A	57, 82
FSR1H	_	_	_	_	Indirect Data	Memory Addre	ess Pointer 1 H	High	0000	58, 82
FSR1L	Indirect Data	Memory Addre	ess Pointer 1 L	ow Byte					xxxx xxxx	58, 82
BSR	_	_	—	_	Bank Select F	Register			0000	58, 72
INDF2	Uses contents	s of FSR2 to a	ddress data m	emory – value	of FSR2 not of	changed (not a	a physical regi	ster)	N/A	58, 82
POSTINC2	Uses contents	s of FSR2 to a	ddress data m	emory – value	e of FSR2 post	-incremented	(not a physica	register)	N/A	58, 82
POSTDEC2	Uses contents	s of FSR2 to a	ddress data m	emory – value	e of FSR2 post	-decremented	(not a physica	al register)	N/A	58, 82
PREINC2	Uses contents	s of FSR2 to a	ddress data m	emory – value	of FSR2 pre-	incremented (I	not a physical	register)	N/A	58, 82
PLUSW2	Uses contents value of FSR2	s of FSR2 to a 2 offset by W	ddress data m	emory – value	of FSR2 pre-	incremented (I	not a physical	register) –	N/A	58, 82
FSR2H	_	_		_	Indirect Data	Memory Addre	ess Pointer 2 I	ligh	0000	58, 82
FSR2L	Indirect Data	Memory Addre	ess Pointer 2 L	ow Byte					xxxx xxxx	58, 82

Note 1: The SBOREN bit is only available when the BOREN<1:0> Configuration bits = 01; otherwise, this bit reads as '0'.

2: These registers and/or bits are not implemented on 64-pin devices and are read as '0'. Reset values are shown for 80-pin devices; individual unimplemented bits should be interpreted as '-'.

3: The PLLEN bit is only available in specific oscillator configuration; otherwise, it is disabled and reads as '0'. See Section 2.6.4 "PLL in INTOSC Modes".

4: RA6/RA7 and their associated latch and direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

5: RG5 and LATG5 are only available when Master Clear is disabled (MCLRE Configuration bit = 0); otherwise, RG5 and LATG5 read as '0'.
6: Bit 7 and Bit 6 are cleared by user software or by a POR.

7: Bit 21 of TBLPTRU allows access to the device Configuration bits.





### REGISTER 10-9: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	
SSP2IE	BCL2IE	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	
bit 7		-					bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'		
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown	
bit 7	SSP2IE: MSS	SP2 Interrupt E	nable bit					
	1 = Enables 0 = Disables	the MSSP2 inte the MSSP2 int	errupt errupt					
bit 6	BCL2IE: MSS	SP2 Bus Collisi	on Interrupt E	Enable bit				
	1 = Enabled							
1.5.5	0 = Disabled							
DIT 5	RC2IE: EUSA	ARI2 Receive I	nterrupt Ena	DIE DIT				
	1 = Enabled 0 = Disabled							
bit 4	TX2IE: EUSA	RT2 Transmit	Interrupt Ena	ble bit				
	1 = Enabled							
	0 = Disabled							
bit 3	TMR4IE: TM	R4 to PR4 Mate	ch Interrupt E	nable bit				
	1 = Enabled							
bit 2	CCP5IF: CCF	P5 Interrupt En	able bit					
5112	1 = Enabled	o intorrupt En						
	0 = Disabled							
bit 1	CCP4IE: CCF	P4 Interrupt En	able bit					
	1 = Enabled							
	0 = Disabled							
bit 0	CCP3IE: EC(	CP3 Interrupt E	nable bit					
	⊥ = Enabled 0 = Disabled							

### 12.1 Timer0 Operation

Timer0 can operate as either a timer or a counter; the mode is selected with the TOCS bit (T0CON<5>). In Timer mode (T0CS = 0), the module increments on every clock by default unless a different prescaler value is selected (see **Section 12.3 "Prescaler"**). If the TMR0 register is written to, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

The Counter mode is selected by setting the TOCS bit (= 1). In this mode, Timer0 increments either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit, T0SE (T0CON<4>); clearing this bit selects the rising edge. Restrictions on the external clock input are discussed below.

An external clock source can be used to drive Timer0; however, it must meet certain requirements to ensure that the external clock can be synchronized with the internal phase clock (Tosc). There is a delay between synchronization and the onset of incrementing the timer/counter.

## 12.2 Timer0 Reads and Writes in 16-bit Mode

TMR0H is not the actual high byte of Timer0 in 16-bit mode; it is actually a buffered version of the real high byte of Timer0 which is not directly readable nor writable (refer to Figure 12-2). TMR0H is updated with the contents of the high byte of Timer0 during a read of TMR0L. This provides the ability to read all 16 bits of Timer0 without having to verify that the read of the high and low byte were valid, due to a rollover between successive reads of the high and low byte.

Similarly, a write to the high byte of Timer0 must also take place through the TMR0H Buffer register. The high byte is updated with the contents of TMR0H when a write occurs to TMR0L. This allows all 16 bits of Timer0 to be updated at once.

### FIGURE 12-1: TIMER0 BLOCK DIAGRAM (8-BIT MODE)



### FIGURE 12-2: TIMER0 BLOCK DIAGRAM (16-BIT MODE)



Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	57
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	60
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	60
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	60
PIR3	SSP2IF	BCL2IF	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	60
PIE3	SSP2IE	BCL2IE	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	60
IPR3	SSP2IP	BCL2IP	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	60
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	60
TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	60
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	60
TMR2	Timer2 Reg	gister							58
PR2	Timer2 Per	iod Register							58
SSP1BUF	MSSP1 Re	ceive Buffer	/Transmit R	egister					58
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	58
SSP1STAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	58
SSP2BUF	MSSP2 Receive Buffer/Transmit Register								
SSP2CON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	61
SSP2STAT	SMP	CKE	D/Ā	Р	S	R/W	UA	BF	61

### TABLE 19-2: REGISTERS ASSOCIATED WITH SPI OPERATION

Legend: Shaded cells are not used by the MSSP module in SPI mode.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	57
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	60
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	60
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	60
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	60
TRISG	—	—	_	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0	60
RCSTAx	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	59
RCREGx	EUSARTx F	Receive Regi	ster						59
TXSTAx	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	59
BAUDCONx	ABDOVF	RCIDL	_	SCKP	BRG16	—	WUE	ABDEN	61
SPBRGHx	EUSARTx E	Baud Rate Ge	enerator Reg	ister High By	⁄te				61
SPBRGx	EUSARTx E	Baud Rate Ge	enerator Reg	ister Low By	te				59

### TABLE 20-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous master reception.

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM		ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 7	ADFM: A/D R	esult Format S	Select bit				
	1 = Right justi 0 = Left justifi	ified ed					
bit 6	Unimplemen	ted: Read as '	0'				
bit 5-3	ACQT<2:0>:	A/D Acquisition	n Time Select	bits			
	$111 = 20 \text{ TAD}$ $110 = 16 \text{ TAD}$ $101 = 12 \text{ TAD}$ $100 = 8 \text{ TAD}$ $011 = 6 \text{ TAD}$ $010 = 4 \text{ TAD}$ $001 = 2 \text{ TAD}$ $000 = 0 \text{ TAD}^{(1)}$	)					
bit 2-0	ADCS<2:0>: 111 = FRC (cl 110 = FOSC/6 101 = FOSC/1 100 = FOSC/4 011 = FRC (cl 010 = FOSC/3 001 = FOSC/8 000 = FOSC/2	A/D Conversio ock derived fro 4 6 ock derived fro 2	n Clock Selec om A/D RC os om A/D RC os	ct bits cillator) <sup>(1)</sup> cillator) <sup>(1)</sup>			

## **Note 1:** If the A/D FRC clock source is selected, a delay of one TCY (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

### REGISTER 21-3: ADCON2: A/D CONTROL REGISTER 2

#### 21.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 21-3. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). The maximum recommended impedance for analog sources is 2.5 k $\Omega$ . After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

Note:	When	the	conversion	is	started,	the
	holding	, capa	acitor is disco	nne	ected from	the
	input p	in.				

EQUATION 21-1: ACQUISITION TIME

TACO Amplifier Settling Time + Holding Capacitor Charging Time + Temperature Coefficient = = TAMP + TC + TCOFF

### EQUATION 21-2: A/D MINIMUM CHARGING TIME

VHOLD	=	$(\text{VREF} - (\text{VREF}/2048)) \bullet (1 - e^{(-\text{TC}/\text{CHOLD}(\text{Ric} + \text{Rss} + \text{Rs}))})$
or		$\langle C_{\text{trov}} \mathbf{p} \rangle \langle \mathbf{p}_{\text{res}} \rangle \mathbf{p}_{\text{res}} \rangle \mathbf{p}_{\text{res}} \rangle 1 \langle 1 \langle 0 \rangle \langle 0 \rangle$
TC	=	-(CHOLD)(RIC + RSS + RS) ln(1/2048)

#### EQUATION 21-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

TACQ	=	TAMP + TC + TCOFF
TAMP	=	0.2 μs
TCOFF	=	(Temp – 25°C)(0.02 μs/°C) (85°C – 25°C)(0.02 μs/°C) 1.2 μs
Tempera	ture co	befficient is only required for temperatures > $25^{\circ}$ C. Below $25^{\circ}$ C, TCOFF = 0 ms.
ТС	=	-(Chold)(Ric + Rss + Rs) $\ln(1/2047) \ \mu s$ -(25 pF) (1 k $\Omega$ + 2 k $\Omega$ + 2.5 k $\Omega$ ) $\ln(0.0004883) \ \mu s$ 1.05 $\mu s$
TACQ	=	0.2 μs + 1 μs + 1.2 μs 2.4 μs

То calculate the minimum acquisition time. Equation 21-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 21-3 shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following application svstem assumptions:

Chold	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	$\leq$	1/2 LSb
Vdd	=	$5V \rightarrow Rss = 2 \ k\Omega$
Temperature	=	85°C (system max.)

					•		,
R/P-1	R/P-1	R/P-1	R/P-1	U-0	U-0	R/P-1	R/P-1
WAIT	BW	ABW1	ABW0	—	_	PM1	PM0
bit 7							bit 0
Legend:							
R = Readat	ole bit	W = Writable	bit	U = Unimplei	mented bit, rea	nd as '0'	
-n = Value a	at POR	'1' = Bit is set	t	'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 7	WAIT: Extern	al Bus Data W	ait Enable bit				
	1 = Wait sele	ections are una	vailable for ta	ble reads and t	table writes		
	0 = Wait sele	ections for table	e reads and ta	ble writes are	determined by	the WAIT<1:0>	bits
bit 6	BW: Data Bu	s Width Select	bit				
	1 = 16-bit Ex	ternal Bus mo	de				
	0 = 8-bit Exte	ernal Bus mod	Э				
bit 5-4	ABW<1:0>: /	Address Bus W	idth Select bi	ts			
	11 = 20-bit a	address bus					
	10 = 16-bit a	address bus					
	01 = 12-bit a	address bus					
	00 = 8-bit a	ddress bus					
bit 3-2	Unimplemen	ited: Read as '	0'				
bit 1-0	<b>PM&lt;1:0&gt;:</b> Pr	ocessor Data N	lemory Mode	Select bits			
	11 = Microco	ontroller mode					
	10 = Micropr	rocessor mode					
	01 = Micropr	ocessor with E	1001 BIOCK MO	ae			
			lier mode				

### REGISTER 25-4: CONFIG3L: CONFIGURATION REGISTER 3 LOW (BYTE ADDRESS 300004h)<sup>(1)</sup>

Note 1: This register is unimplemented in PIC18F6527/6622/6627/6722 devices.

ADDWFC	ADD W an	d Carry	bit to f	
Syntax:	ADDWFC	f {,d {,	a}}	
Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$			
Operation:	(W) + (f) +	$(C) \rightarrow de$	st	
Status Affected:	N,OV, C, D	C, Z		
Encoding:	0010	00da	fff	f ffff
Description:	Add W, the location 'f'. placed in V placed in d	Carry fla If 'd' is '0 V. If 'd' is ata mem	g and o )', the r '1', the ory loc	data memory result is result is ation 'f'.
	If 'a' is '0', t If 'a' is '1', t GPR bank	he Acces he BSR i (default).	s Banl s used	k is selected. to select the
	If 'a' is '0' a set is enab in Indexed mode when Section 26 Bit-Oriente Literal Offe	Ind the e. Ied, this i Literal O never f ≤ 5.2.3 "By ed Instru set Mode	xtende nstruct ffset Ac 95 (5F te-Orie ctions or cons	d instruction ion operates ddressing h). See ented and in Indexed letails.
Words:	1			
Cycles:	1			
Q Cycle Activity:				
Q1	Q2	Q3		Q4
Decode	Read register 'f'	Proce Data	SS 1	Write to destination
Example:	ADDWFC	REG,	0, 1	
Before Instruc Carry bit REG W	tion = 1 = 02h = 4Dh			
After Instructio Carry bit REG W	on = 0 = 02h = 50h			

AND	olw	AND Litera	al with W	,		
Synt	ax:	ANDLW	k			
Oper	rands:	$0 \le k \le 255$	5			
Oper	ration:	(W) .AND.	$k \rightarrow W$			
Statu	us Affected:	N, Z				
Enco	oding:	0000	1011	kkk	ck	kkkk
Desc	cription:	The conter 8-bit literal	nts of W a 'k'. The r	are AN esult i	IDed s pla	I with the aced in W
Word	ds:	1				
Cycle	es:	1				
QC	cycle Activity:					
	Q1	Q2	Q3			Q4
	Decode	Read literal	Proce	SS	Write to	/rite to
		·Κ	Data	a		VV
<u>Exar</u>	<u>mple:</u>	ANDLW	05Fh			
	Before Instruc	tion				
	W After Instruction	= A3h				
	W	= 03h				

BRA Unconditional Branch								
Synta	ax:	BRA n	BRA n					
Oper	ands:	-1024 ≤ n ≤	1023					
Operation: $(PC) + 2 + 2n \rightarrow PC$								
Statu	s Affected:	None	None					
Enco	ding:	1101	0nnn	nnn	n	nnnn		
Description: Add the 2's complement number '2n' the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is a two-cycle instruction.					oer '2n' to e vill be s a			
Word	s:	1	1					
Cycle	es:	2	2					
QC	ycle Activity:							
	Q1	Q2	Q3	Q4		Q4		
	Decode	Read literal 'n'	Proce Data	ss 1	V	/rite to PC		
	No	No	No			No		
	operation	operation	operat	ion	ор	eration		
Exan	nple: Before Instruc PC After Instructic	HERE tion = ad	BRA dress (F	Jump HERE)				
	PC	= ad	aress (	Jump)				

BSF		Bit Set f							
Synta	ax:	BSF f, b	{,a}						
Oper	ands:	0 ≤ f ≤ 255 0 ≤ b ≤ 7 a ∈ [0,1]	$0 \le f \le 255$ $0 \le b \le 7$ $a \in [0,1]$						
Oper	ation:	$1 \rightarrow \text{f}$							
Statu	s Affected:	None							
Enco	ding:	1000	bbba	ffff	ffff				
Desc	ription:	Bit 'b' in re	gister 'f' i	s set.					
		If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).							
	If 'a' is '0' and the extended instruction set is enabled, this instruction operate in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 26.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed								
Word	ls:	1							
Cycle	es:	1							
QC	ycle Activity:								
	Q1	Q2	Q3	}	Q4				
	Decode	Read	Proce	SS	Write				
		register 'f'	Data	a	register 'f'				

Example:

Before Instruction FLAG\_REG = 0Ah After Instruction FLAG\_REG = 8Ah

BSF

FLAG\_REG, 7, 1

COMF	Compleme	ent f		CPFSEQ		Compare f	with W, Skip	if f = W
Syntax:	COMF f	{,d {,a}}		Syntax:		CPFSEQ	f {,a}	
Operands:	$\begin{array}{l} 0 \leq f \leq 255 \\ d  \in  [0,1] \end{array}$			Operands:		$\begin{array}{l} 0 \leq f \leq 255 \\ a \in [0,1] \end{array}$		
Operation:	$a \in [0,1]$ $(\overline{f}) \rightarrow de$	st		Operation:		(f) - (W), skip if $(f) =$	(W)	
Status Affected:	N, Z			Statua Affaat	la di	(unsigned d	comparison)	
Encoding:	0001	11da ff	ff ffff	Status Allect	led.		001a ff	ee eeee
Description:	The conten complemer stored in W stored back	ts of register " nted. If 'd' is '0 '. If 'd' is '1', th c in register 'f'	f' are ', the result is e result is (default).	Description:		Compares to location 'f' to performing	the contents of o the contents an unsigned s	f data memory of W by subtraction.
	If 'a' is '0', t If 'a' is '1', t GPR bank	he Access Ba he BSR is use (default).	nk is selected. d to select the			If 'f' = W, th discarded a instead, ma instruction.	en the fetched and a NOP is ex aking this a two	l instruction is xecuted o-cycle
	If 'a' is '0' a set is enabl in Indexed	nd the extend led, this instru Literal Offset $\mu$	ed instruction ction operates Addressing Eb) See			lf 'a' is '0', t lf 'a' is '1', t GPR bank	he Access Bar he BSR is use (default).	nk is selected. d to select the
	Section 26 Bit-Oriente Literal Offs	.2.3 "Byte-Or ed Instruction set Mode" for	iented and is in Indexed details.			If 'a' is '0' a set is enabl in Indexed	nd the extende ed, this instruc Literal Offset A pever $f < 95$ (5)	ed instruction ction operates Addressing Eb) See
Words:	1					Section 26	.2.3 "Byte-Or	iented and
Cycles:	1					Bit-Oriente	d Instruction	s in Indexed
Q Cycle Activity:						Literal Offs	set Mode" for	details.
Q1	Q2	Q3	Q4	Words:		1		
Decode	Read register 'f'	Process Data	Write to destination	Cycles:		1(2) <b>Note:</b> 3 cy by a	cles if skip and 2-word instrue	d followed
Fyomolo	COME	556 0 0		Q Cycle Act	tivity:			
Example.	COMP	REG, 0, 0		Q	1	Q2	Q3	Q4
Before Instruc	tion – 13h			Deco	ode	Read	Process	No
After Instruction	on			If skip:		register T	Data	operation
REG	= 13h			li skip. Q	1	Q2	Q3	Q4
vv	= ECII			No	c	No	No	No
				opera	ation	operation	operation	operation
				If skip and f	ollowed	by 2-word in	struction:	<i></i>
				Q	1	Q2	Q3	Q4
				opera	ation	operation	operation	operation
				No	D	No	No	No
				opera	ation	operation	operation	operation
				<u>Example:</u>		HERE NEQUAL EOUAL	CPFSEQ REG : :	<b>5</b> , 0
				Before PC W RE	Instruct C Addre EG	ion SS = HE = ? = ?	RE	

After Instruction If REG PC If REG PC

= ≠ W; Address (EQUAL) W; Address (NEQUAL)

RRN	CF	Rotate Ri	ght f (no	carry)	
Synta	ax:	RRNCF	f {,d {,a}}		
Oper	ands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$	5		
Oper	ation:	$(f < n >) \rightarrow c$ $(f < 0 >) \rightarrow c$	dest <n 1<br="" –="">dest&lt;7&gt;</n>	>,	
Statu	s Affected:	N, Z			
Enco	ding:	0100	00da	fff	f ffff
Description: The contents of register 'f' are one bit to the right. If 'd' is '0', t is placed in W. If 'd' is '1', the r placed back in register 'f' (defa				' are rotated '0', the result the result is (default).	
		If 'a' is '0', selected, o is '1', then per the BS	the Acce overriding the bank SR value (	ss Bar the B will be defaul	nk will be SR value. If 'a' e selected as lt).
		If 'a' is '0' set is enal in Indexec mode whe Section 2 Bit-Orient Literal Of	and the e bled, this i I Literal O enever f ≤ 6.2.3 "By ted Instru fset Mode	xtende instruc ffset A 95 (5F te-Ori ictions e" for	ed instruction ttion operates addressing Fh). See ented and s in Indexed details.
			► re	egister	
Word	ls:	1			
Cycle	es:	1			
QC	ycle Activity:				
	Q1	Q2	Q	3	Q4
	Decode	Read register 'f'	Proce Data	ess a	Write to destination
<u>Exan</u>	<u>nple 1:</u>	RRNCF	REG, 1	, 0	
	Before Instruc	tion			
	REG	= 1101	0111		
	After Instructio REG	on = 1110	1011		
<u>Exan</u>	<u>nple 2:</u>	RRNCF	REG, 0	, 0	
	Before Instruc	tion			
	W REG	= ? = 1101	0111		
	After Instructio	on			
	W REG	= 1110 = 1101	1011 0111		

Syntax:	SETF f {,;	a}		
Operands:	$0 \le f \le 255$			
	$a \in [0,1]$			
Operation:	$FFh\tof$			
Status Affected:	None			
Encoding:	0110	100a	ffff	ffff
Description:	The conten are set to F	ts of the Fh.	specified	register
	If 'a' is '0', t If 'a' is '1', t GPR bank	he Acces he BSR i (default).	ss Bank is s used to	s selected select the
	If 'a' is '0' a set is enabl in Indexed mode wher	nd the ex led, this i Literal Of never f $\leq$	ktended i nstruction ffset Add 95 (5Fh).	nstruction n operates ressing See
	Section 26 Bit-Oriente Literal Offs	.2.3 "By ed Instru set Mode	te-Orient ctions ir e" for det	ted and Indexed ails.
Words:	Section 26 Bit-Oriente Literal Offs	.2.3 "By ed Instru set Mode	ctions ir ctions ir " for det	ted and Indexed ails.
Words: Cycles:	Section 26 Bit-Oriente Literal Offs 1	.2.3 "By ed Instru set Mode	te-Orient ctions ir e" for det	ted and Indexed ails.
Words: Cycles: Q Cycle Activity:	Section 26 Bit-Oriente Literal Offs 1 1	.2.3 "By ed Instru set Mode	te-Orient ctions ir ?" for det	ted and Indexed ails.
Words: Cycles: Q Cycle Activity: Q1	Section 26 Bit-Oriente Literal Offs 1 1 Q2	.2.3 "By ed Instru set Mode	te-Orient ctions ir of for det	ted and Indexed ails. Q4
Words: Cycles: Q Cycle Activity: Q1 Decode	Section 26 Bit-Oriente Literal Offs 1 1 2 Q2 Read	.2.3 "By ed Instru set Mode Q3 Proce	te-Orient ctions ir e" for det	ted and Indexed ails. Q4 Write
Words: Cycles: Q Cycle Activity: Q1 Decode	Section 26 Bit-Oriente Literal Offs 1 1 Q2 Read register 'f'	.2.3 "By ed Instru set Mode Q3 Proce Data	te-Orient ctions ir ? for det	eed and ails. Q4 Write egister 'f'
Words: Cycles: Q Cycle Activity: Q1 Decode <u>Example:</u>	Section 26 Bit-Oriente Literal Offs 1 1 Q2 Read register 'f'	2.3 "By ed Instru set Mode Q3 Proce Data	te-Orien ctions ir " for det ss a re 3, 1	ed and Indexed ails. Q4 Write egister 'f'
Words: Cycles: Q Cycle Activity: Q1 Decode Example: Before Instruct	Section 26 Bit-Oriente Literal Offs 1 1 2 Read register 'f' SETF :tion	.2.3 "By ed Instru set Mode Q3 Proce Data	te-Orien ctions ir " for det ss a re	eed and a Indexed ails. Q4 Write egister 'f'
Words: Cycles: Q Cycle Activity: Q1 Decode Example: Before Instruct REG After Instruct	Section 26 Bit-Oriente Literal Offs 1 1 1 Q2 Read register 'f' SETF tion = 5A	.2.3 "By d Instru set Mode Q3 Proce Data RE0	te-Ornen ctions ir a" for det ss a re	eed and ails. Q4 Write egister 'f'
Words: Cycles: Q Cycle Activity: Q1 Decode <u>Example:</u> Before Instruct REG After Instructio REG	Section 26 Bit-Oriente Literal Offs 1 1 1 Q2 Read register 'f' SETF tion = 5A on = FF	2.3 "By ed Instru set Mode Q3 Proce Data RE0 h	te-Orien ctions ir " for det ss a re	ed and Indexed ails. Q4 Write egister 'f'

SUB	FSR	Subtract	Literal fr	om F	SR			
Syntax: SUBFSR f, k								
Oper	ands:	$0 \le k \le 63$						
		f ∈ [ 0, 1, 2 ]						
Oper	ation:	FSRf – k	$\rightarrow$ FSRf					
Statu	s Affected:	None						
Enco	ding:	1110	1001	ffk}	c.	kkkk		
Desc	ription:	The 6-bit the conte by 'f'.	literal 'k' is nts of the	s subti FSR s	racte spec	ed from cified		
Word	ls:	1	1					
Cycle	es:	1	1					
QC	ycle Activity:							
	Q1	Q2	Q3			Q4		
	Decode	Read	Proce	SS	V	Vrite to		
		register 'f'	Data	1	de	stination		
<u>Exan</u>	<u>nple:</u>	SUBFSR	2, 23h					

<u>xample:</u>	SUBFSR 2,	, 23h
Before Instruction	า	
FSR2 =	03FFh	
After Instruction		
FSR2 =	03DCh	

SUB	ULNK	Subtract Literal from FSR2 and Return						
Synta	ax:	SUBULNK	k					
Oper	ands:	$0 \le k \le 63$						
Oper	ation:	$FSR2 - k \rightarrow FSR2$						
		$(TOS) \rightarrow PC$						
Statu	s Affected:	None						
Enco	ding:	1110	1001	L	11kk		kkkk	
Desc	ription:	The 6-bit literal 'k' is subtracted from the contents of the FSR2. A RETURN is then executed by loading the PC with the TOS.						
		The instruction takes two cycles to execute; a NOP is performed during the second cycle.						
		This may b of the SUB (binary '11	e thou FSR in '); it op	ght o struo perat	of as a s ction, wh es only	peo hero on	cial case e f = 3 FSR2.	
Word	ls:	1						
Cycle	es:	2						
QC	ycle Activity:							
	Q1	Q2		C	23		Q4	
	Decode	Read		Proc	cess	١	Write to	
		register	f'	Da	ita	de	estination	
	No	No		Ν	0		No	
	Operation	Operatio	n (	Dper	ation	0	peration	

Example: SUBULNK 23h

Before Instruction								
FSR2	=	03FFh						
PC	=	0100h						
After Instruct	ion							
FSR2	=	03DCh						
PC	=	(TOS)						



Param. No	Symbol	Characteristics	Min	Тур	Max	Units
150	TadV2alL	Address Out Valid to ALE $\downarrow$ (address setup time)	0.25 Tcy – 10	_	—	ns
151	TalL2adl	ALE $\downarrow$ to Address Out Invalid (address hold time)	5			ns
155	TalL2oeL	ALE $\downarrow$ to $\overline{OE} \downarrow$	10	0.125 Tcy	—	ns
160	TadZ2oeL	AD high-Z to $\overline{OE} \downarrow$ (bus release to $\overline{OE}$ )	0		—	ns
161	ToeH2adD	OE ↑ to AD Driven	0.125 Tcy – 5		—	ns
162	TadV2oeH	LS Data Valid before $\overline{OE}$ $\uparrow$ (data setup time)	20		—	ns
163	ToeH2adl	$\overline{OE}$ $\uparrow$ to Data In Invalid (data hold time)	0	_	—	ns
164	TalH2alL	ALE Pulse Width	—	Тсү	—	ns
165	ToeL2oeH	OE Pulse Width	0.5 Tcy – 5	0.5 TCY	_	ns
166	TalH2alH	ALE $\uparrow$ to ALE $\uparrow$ (cycle time)	—	0.25 TCY	—	ns
167	Tacc	Address Valid to Data Valid	0.75 Tcy – 25		—	ns
168	Тое	$\overline{OE} \downarrow$ to Data Valid			0.5 Tcy – 25	ns
169	TalL2oeH	ALE ↓ to OE ↑	0.625 Tcy – 10		0.625 Tcy + 10	ns
171	TalH2csL	Chip Enable Active to ALE $\downarrow$	0.25 Tcy – 20		—	ns
171A	TubL2oeH	AD Valid to Chip Enable Active	_	_	10	ns

TARI E 28-10·	CLKO	TIMING	REQUIREMENTS
IADEL 20-10.	OLINO .		

### 64-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



**RECOMMENDED LAND PATTERN** 

	Units	MILLIM	ETERS	
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085A

### 80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIM	ETERS	
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X80)	X1			0.30
Contact Pad Length (X80)	Y1			1.50
Distance Between Pads	G	0.20		

### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2092A

RC	
RCIO	
XT	
Oscillator Selection	
Oscillator Start-up Timer (OST)	
Oscillator Switching	
Oscillator Transitions	
Oscillator, Timer1	
Oscillator, Timer3	

### Ρ

Packaging	419
Details	420
Marking	419
Parallel Slave Port (PSP)	158
Associated Registers	160
RE0/RD Pin	158
RE1/WR Pin	158
RE2/CS Pin	158
Select (PSPMODE Bit)	158
PICSTART Plus Development Programmer	374
PIE Registers	127
Pin Functions	
	20
	20 30
AV55	20 20
AVSS	
05C1/CLKI/RA7	13, 21
OSC2/CLKO/RA6	13, 21
RA0/AN0	14, 22
RA1/AN1	14, 22
RA2/AN2/VREF	14, 22
RA3/AN3/VREF+	14, 22
RA4/T0CKI	14, 22
RA5/AN4/HLVDIN	14, 22
RB0/INT0/FLT0	15, 23
RB1/INT1	15. 23
RB2/INT2	15,23
RB3/INT3	
RB3/INT3/ECCP2/P2A	10 23
	15 23
	15 23
	10, 20
	15, 23
	15, 23
RC0/110S0/113CKI	16, 24
RC1/T1OSI/ECCP2/P2A	16, 24
RC2/ECCP1/P1A	16, 24
RC3/SCK1/SCL1	16, 24
RC4/SDI1/SDA1	16, 24
RC5/SDO1	16, 24
RC6/TX1/CK1	16, 24
RC7/RX1/DT1	16, 24
RD0/AD0/PSP0	
RD0/PSP0	
RD1/AD1/PSP1	25
RD1/PSP1	20
RD 7/1 01 1	
	20 17
RD2/F3F2	17 25
RD3/AD3/P3P3	20
	1/
KU4/AU4/YSY4/SUU2	
KD4/PSP4/SDO2	17
RD5/AD5/PSP5/SDI2/SDA2	25
RD5/PSP5/SDI2/SDA2	17
RD6/AD6/PSP6/SCK2/SCL2	25
RD6/PSP6/SCK2/SCL2	17

RD7/AD7/P <u>SP7</u> /SS2	25
RD7/PSP7/SS2	17
RE0/ <u>AD</u> 8/RD/P2D	26
RE0/RD/P2D	18
RE1/AD9/WR/P2C	26
RE1/WR/P2C	18
RE2/AD10/CS/P2B	26
RE2/CS/P2D	18
RE3/AD11/P3C	26
RE3/P3C	18
RE4/AD12/P3B	26
RE4/P3B	. 18
RE5/AD13/P1C	
RE5/P1C	. 18
RE6/AD14/P1B	26
RE6/P1B	20
RE7/AD15/ECCP2/P2A	26
RE7/ECCD2/D2A	18
RE1/ECCF2/F2A	10
RF0/ANS	2, Z1
	), ZI
RF2/AN7/C1001	9, 27
RF3/AN8	9,27
RF4/AN9	9,27
RF5/AN10/CVREF	9, 27
RF6/ <u>AN1</u> 119	9, 27
RF7/SS119	9, 27
RG0/ECCP3/P3A	), 28
RG1/TX2/CK2	), 28
RG2/RX2/DT2 20	), 28
RG3/CCP4/P3D	), 28
RG4/CCP5/P1D20	), 28
RG5	), 28
RG5 20 RG5/MCLR/VPP 13	), 28 3, 21
RG5 20 RG5/MCLR/VPP 13 RH0/A16	), 28 3, 21 29
RG5 20 RG5/MCLR/VPP13 RH0/A16 RH1/A17	), 28 3, 21 29 29
RG5 20 RG5/MCLR/VPP13 RH0/A16 RH1/A17 RH2/A18	), 28 3, 21 29 29 29
RG5 20 RG5/MCLR/VPP	), 28 3, 21 29 29 29 29 29
RG5 20 RG5/MCLR/VPP	), 28 3, 21 29 29 29 29 29 29
RG5 20 RG5/MCLR/VPP	), 28 3, 21 29 29 29 29 29 29
RG5 20 RG5/MCLR/VPP	), 28 3, 21 29 29 29 29 29 29 29
RG5       20         RG5/MCLR/VPP       13         RH0/A16       15         RH1/A17       17         RH2/A18       18         RH3/A19       19         RH4/AN12/P3C       16         RH5/AN13/P3B       17         RH6/AN14/P1C       17         RH7/AN15/P1B       17	), 28 3, 21 29 29 29 29 29 29 29 29 29
RG5       20         RG5/MCLR/VPP       13         RH0/A16       15         RH1/A17       17         RH2/A18       18         RH3/A19       19         RH4/AN12/P3C       16         RH5/AN13/P3B       17         RH6/AN14/P1C       17         RH7/AN15/P1B       10/ALF	), 28 3, 21 29 29 29 29 29 29 29 29 29 30
RG5       20         RG5/MCLR/VPP       13         RH0/A16       13         RH1/A17       13         RH2/A18       14         RH3/A19       14         RH4/AN12/P3C       14         RH5/AN13/P3B       14         RH6/AN14/P1C       14         RH7/AN15/P1B       14         RJ0/ALE       14	), 28 3, 21 29 29 29 29 29 29 29 29 29 30 30
RG5       20         RG5/MCLR/VPP       13         RH0/A16       13         RH1/A17       13         RH2/A18       14         RH3/A19       14         RH4/AN12/P3C       14         RH5/AN13/P3B       14         RH6/AN14/P1C       14         RH7/AN15/P1B       14         RJ0/ALE       12         RJ1/OE       12	), 28 3, 21 29 29 29 29 29 29 29 29 29 30 30 30
RG5       20         RG5/MCLR/VPP       13         RH0/A16       13         RH1/A17       13         RH2/A18       14         RH3/A19       14         RH4/AN12/P3C       14         RH5/AN13/P3B       14         RH6/AN14/P1C       14         RJ0/ALE       15         RJ1/OE       14         RJ2/WRL       14	), 28 3, 21 29 29 29 29 29 29 29 29 29 30 30 30
RG5       20         RG5/MCLR/VPP       13         RH0/A16       13         RH1/A17       13         RH2/A18       14         RH3/A19       14         RH4/AN12/P3C       14         RH5/AN13/P3B       14         RH6/AN14/P1C       14         RJ0/ALE       15         RJ2/WRL       16         RJ3/WRH       17         RJ4/BA0       14	), 28 3, 21 29 29 29 29 29 29 29 29 29 30 30 30 30
RG5       20         RG5/MCLR/VPP       13         RH0/A16       13         RH1/A17       13         RH2/A18       14         RH3/A19       14         RH4/AN12/P3C       14         RH5/AN13/P3B       14         RH6/AN14/P1C       14         RJ0/ALE       15         RJ3/WRH       14         RJ4/BA0       14	), 28 3, 21 29 29 29 29 29 29 29 29 29 30 30 30 30 30
RG5       20         RG5/MCLR/VPP       13         RH0/A16       13         RH1/A17       13         RH2/A18       14         RH3/A19       14         RH4/AN12/P3C       14         RH5/AN13/P3B       14         RH6/AN14/P1C       14         RJ0/ALE       17         RJ2/WRL       17         RJ3/WRH       17         RJ4/BA0       16         RJ6/E       16	), 28 3, 21 29 29 29 29 29 29 29 29 29 30 30 30 30
RG5       20         RG5/MCLR/VPP       13         RH0/A16       13         RH1/A17       13         RH2/A18       14         RH3/A19       14         RH4/AN12/P3C       14         RH5/AN13/P3B       14         RH6/AN14/P1C       14         RJ0/ALE       17         RJ2/WRL       17         RJ3/WRH       17         RJ4/BA0       14         RJ6/LB       14         RJ7/UB       14	<ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 30</li> </ul>
RG5       20         RG5/MCLR/VPP       13         RH0/A16       13         RH1/A17       13         RH2/A18       14         RH3/A19       14         RH4/AN12/P3C       14         RH5/AN13/P3B       14         RH6/AN14/P1C       14         RJ0/ALE       17         RJ2/WRL       16         RJ3/WRH       17         RJ4/BA0       14         RJ5/CE       14         RJ6/LB       14         RJ7/UB       14	<ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 30</li> <li>c), 40</li> <li>c), 4</li></ul>
RG5       20         RG5/MCLR/VPP       13         RH0/A16       13         RH1/A17       13         RH2/A18       14         RH3/A19       14         RH4/AN12/P3C       14         RH5/AN13/P3B       15         RH6/AN14/P1C       16         RJ0/ALE       17         RJ2/WRL       17         RJ3/WRH       17         RJ4/BA0       16         RJ5/CE       16         RJ7/UB       17         VDD       16	<ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 20</li> </ul>
RG5       20         RG5/MCLR/VPP       13         RH0/A16       13         RH1/A17       14         RH1/A17       15         RH2/A18       14         RH3/A19       15         RH4/AN12/P3C       15         RH5/AN13/P3B       16         RH6/AN14/P1C       17         RJ0/ALE       17         RJ1/OE       17         RJ3/WRL       17         RJ3/WRH       17         RJ4/BA0       16         RJ7/UB       17         VDD       17         VDD       17	<ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 30</li> <li>c), 30</li> <li>c), 20</li> <li>c), 30</li> <li>c), 20</li> <li>c), 30</li> </ul>
RG5       20         RG5/MCLR/VPP       13         RH0/A16       13         RH1/A17       13         RH2/A18       14         RH3/A19       15         RH4/AN12/P3C       15         RH5/AN13/P3B       16         RH6/AN14/P1C       17         RJ0/ALE       17         RJ2/WRL       17         RJ3/WRH       17         RJ4/BA0       17         RJ5/CE       16         RJ7/UB       17         VDD       17         VDD       10         VSS       10	<ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 20</li> <li>c), 30</li> <li>c), 40</li> <li>c), 4</li></ul>
RG5       20         RG5/MCLR/VPP       13         RH0/A16       13         RH1/A17       14         RH1/A17       15         RH2/A18       15         RH3/A19       15         RH4/AN12/P3C       16         RH5/AN13/P3B       17         RH6/AN14/P1C       17         RJ0/ALE       17         RJ1/OE       17         RJ2/WRL       17         RJ3/WRH       17         RJ4/BA0       17         RJ7/UB       17         VDD       17         VDD       17         VDD       17         VSS       17	<ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 20</li> <li>c), 20</li> <li>c), 20</li> <li>c), 20</li> <lic), 20<="" li=""> <li>c), 20</li> <lic), 20<="" li=""> <li>c), 20</li> <lic), 20<="" li=""> <li>c), 20</li> <lic), 20<="" li=""> <li>c), 20</li> <li>c), 20</li></lic),></lic),></lic),></lic),></ul>
RG5       20         RG5/MCLR/VPP       13         RH0/A16       14         RH1/A17       15         RH1/A17       15         RH2/A18       15         RH3/A19       15         RH4/AN12/P3C       16         RH5/AN13/P3B       17         RH6/AN14/P1C       17         RJ0/ALE       17         RJ1/OE       17         RJ2/WRL       17         RJ3/WRH       17         RJ3/WRH       17         RJ4/BA0       17         RJ5/CE       16         RJ7/UB       17         VDD       17         VDD       17         VD       17         VD       17         RJ6/LB       17         RJ7/UB       17         VD       17         VD       17         VD       17         RUB       17         RJ6/LB       17         RJ7/UB       17         VD       17         VD       17         RUB       17         RUB       17         RUB       10	<ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 2</li></ul>
RG5       20         RG5/MCLR/VPP       13         RH0/A16       14         RH1/A17       15         RH1/A17       15         RH2/A18       16         RH3/A19       17         RH4/AN12/P3C       16         RH5/AN13/P3B       17         RH6/AN14/P1C       17         RJ0/ALE       17         RJ1/OE       17         RJ2/WRL       17         RJ3/WRH       17         RJ3/WRH       17         RJ4/BA0       17         RJ5/CE       17         RJ6/LB       17         VDD       17         VDD       17         VD       17         VB       17         RJ6/LB       17         RJ7/UB       17         VDD       17         VD       17         VB       17         RU       17         RJ6/LB       17         RJ7/UB       17         VDD       17         VB       17         RU       17         RU       17         RU       17 </td <td><ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <lic), 29<="" li=""> <li>c), 29</li> <lic), 29<<="" td=""></lic),></lic),></ul></td>	<ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <lic), 29<="" li=""> <li>c), 29</li> <lic), 29<<="" td=""></lic),></lic),></ul>
RG5       20         RG5/MCLR/VPP       13         RH0/A16       14         RH1/A17       15         RH1/A17       15         RH2/A18       16         RH3/A19       17         RH3/A19       17         RH3/A19       17         RH3/A19       17         RH4/AN12/P3C       17         RH5/AN13/P3B       17         RH6/AN14/P1C       17         RJ0/ALE       17         RJ1/OE       17         RJ2/WRL       17         RJ3/WRH       17         RJ3/WRH       17         RJ4/BA0       17         RJ5/CE       17         RJ6/LB       17         VDD       17         VDD       17         VDD       17         VSS       17         VSS       17         VB       17         VD       17         RJ6/LB       17         RJ7/UB       17         VDD       17         VD       17         VD       17         RJ8       17         RJ7	<ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 2</li></ul>
RG5       20         RG5/MCLR/VPP       13         RH0/A16       14         RH1/A17       15         RH2/A18       16         RH3/A19       17         RH4/AN12/P3C       17         RH5/AN13/P3B       17         RH6/AN14/P1C       17         RJ0/ALE       17         RJ1/OE       17         RJ2/WRL       17         RJ3/WRH       17         RJ4/BA0       17         RJ5/CE       17         RJ6/LB       17         VDD       17         VD       17         VD       17         VB       17         VD       17         RJ3/WRH       17         RJ6/LB       17         RJ7/UB       10         VD       10         VD       10         VD       10         VD       10         VB       10         VD       10         VB       10         VD       10         VB       10         VD       10         VB       10	<ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 2</li></ul>
RG5       20         RG5/MCLR/VPP       13         RH0/A16       14         RH1/A17       15         RH2/A18       16         RH3/A19       17         RH4/AN12/P3C       17         RH5/AN13/P3B       17         RH6/AN14/P1C       17         RJ0/ALE       17         RJ1/OE       17         RJ2/WRL       17         RJ3/WRH       17         RJ5/CE       17         RJ6/LB       17         VDD       17         VD       17         VD       17         VB       17         VB       17         RJ6/LB       17         RJ7/UB       17         VD       17	<ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 2</li></ul>
RG5       20         RG5/MCLR/VPP       13         RH0/A16       14         RH1/A17       15         RH2/A18       16         RH3/A19       17         RH4/AN12/P3C       17         RH5/AN13/P3B       17         RH5/AN13/P3B       17         RH6/AN14/P1C       17         RJ0/ALE       17         RJ1/OE       17         RJ2/WRL       17         RJ3/WRH       17         RJ5/CE       17         RJ6/LB       17         VDD       17         VDD       17         VDD       17         VB       17         VB       17         VD       17         RJ3/ZE       17         RJ3/WRH       16         RJ3/ZE       17         VD       17         VD       17         VD       17         RJ3/ZE       17         RJ3/ZE       17         RJ3/ZE       17         RJ3/ZE       17         RUB       16         RJ3/ZE       17         RJ3/ZE <td><ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 30</li> <li>c), 40</li> <li>c), 4</li></ul></td>	<ul> <li>a), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 30</li> <li>c), 40</li> <li>c), 4</li></ul>
RG5       20         RG5/MCLR/VPP       13         RH0/A16       14         RH1/A17       15         RH2/A18       16         RH3/A19       17         RH4/AN12/P3C       17         RH5/AN13/P3B       17         RH5/AN13/P3B       17         RH6/AN14/P1C       17         RJ0/ALE       17         RJ1/OE       17         RJ2/WRL       17         RJ3/WRH       17         RJ3/WR       17         RJ3/WR       17         RJ3/WR       17         RJ3/WR       17         RJ3/WR       17         RJ3/ZE       17         WD       10         VDD       10         VD       10         VD       10         VS       10	<ul> <li>b), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 30</li> <li>c), 40</li> <li>c), 4</li></ul>
RG5       20         RG5/MCLR/VPP       13         RH0/A16       14         RH1/A17       15         RH2/A18       16         RH3/A19       17         RH4/AN12/P3C       17         RH5/AN13/P3B       17         RH5/AN13/P3B       17         RH6/AN14/P1C       17         RJ0/ALE       17         RJ1/OE       17         RJ2/WRL       17         RJ3/WRH       17         WD       10         VD	<ul> <li>b), 28</li> <li>b), 28</li> <li>c), 29</li> <li>c), 2</li></ul>