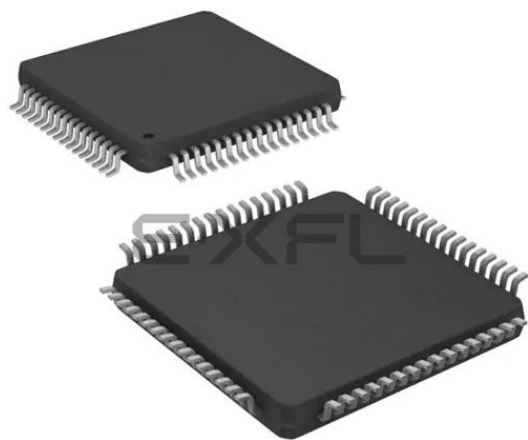




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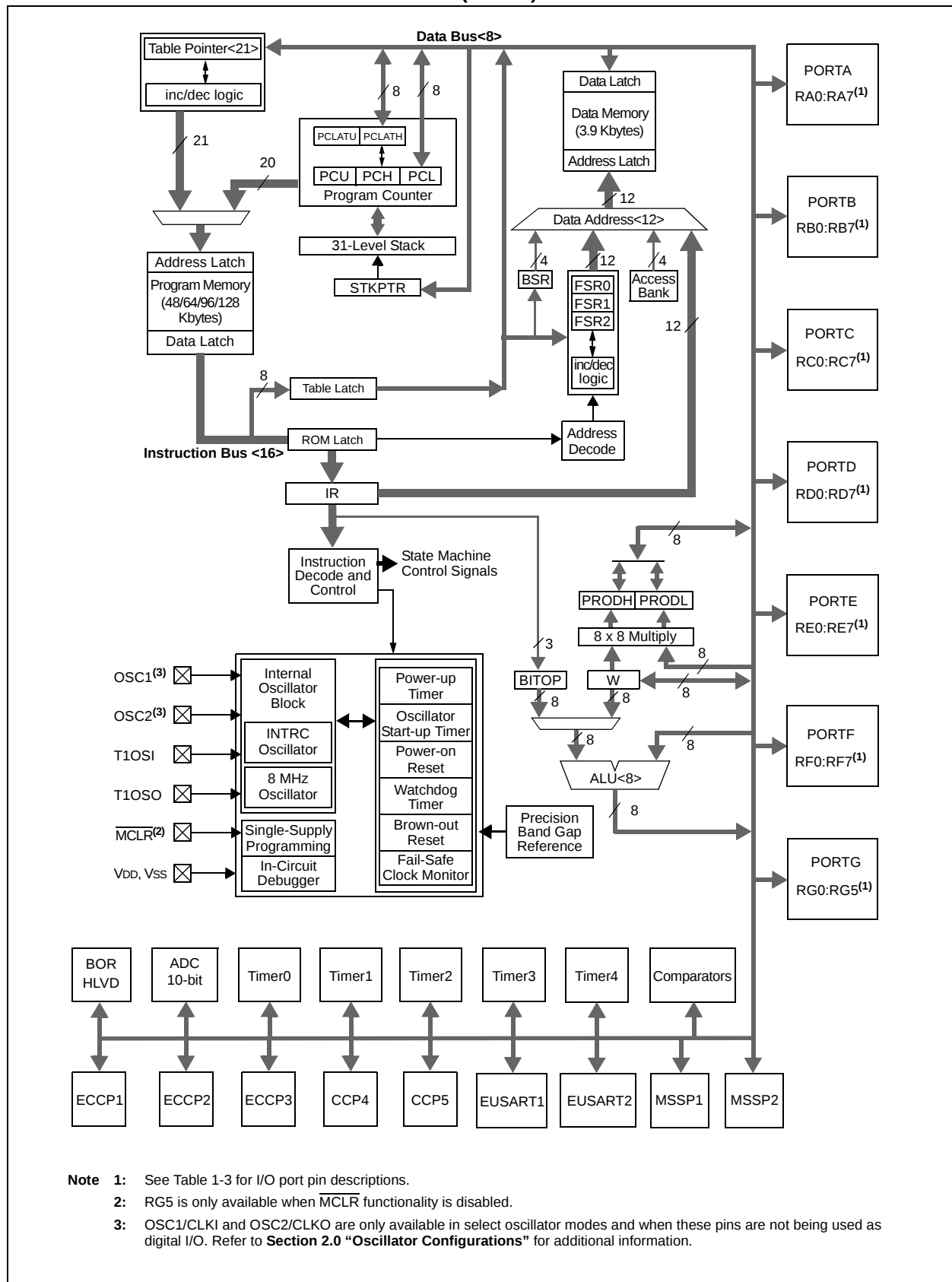
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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf6627-i-pt

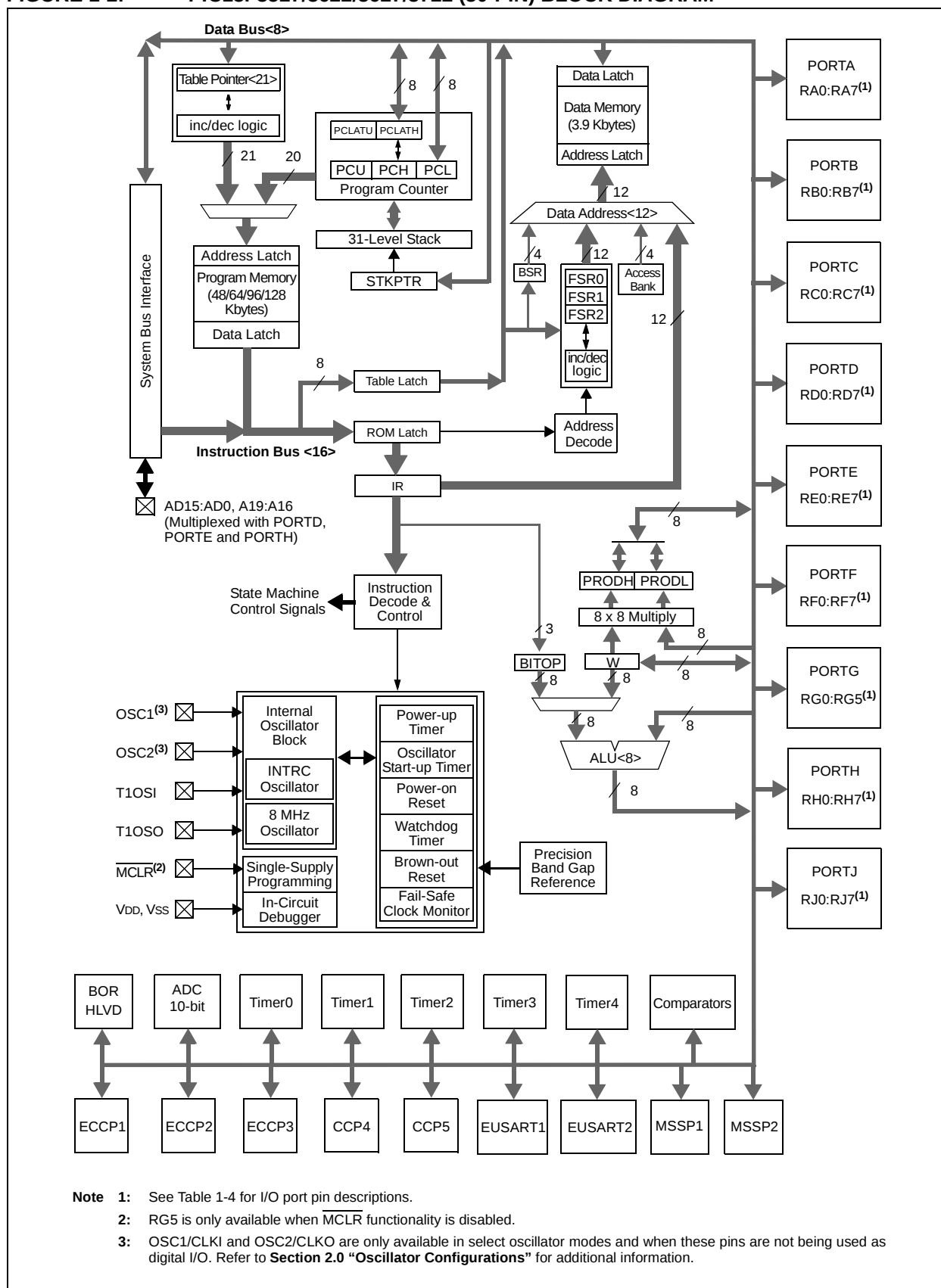
PIC18F8722 FAMILY

FIGURE 1-1: PIC18F6527/6622/6627/6722 (64-PIN) BLOCK DIAGRAM



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FIGURE 1-2: PIC18F8527/8622/8627/8722 (80-PIN) BLOCK DIAGRAM



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REGISTER 2-2: OSCCON: OSCILLATOR CONTROL REGISTER

R/W-0	R/W-1	R/W-0	R/W-0	R ⁽¹⁾	R-0	R/W-0	R/W-0
IDLEN	IRCF2	IRCF1	IRCF0	OSTS	IOFS	SCS1	SCS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **IDLEN:** Idle Enable bit

1 = Device enters an Idle mode when a SLEEP instruction is executed

0 = Device enters Sleep mode when a SLEEP instruction is executed

bit 6-4 **IRCF<2:0>:** Internal Oscillator Frequency Select bits⁽⁵⁾

111 = 8 MHz (INTOSC drives clock directly)

110 = 4 MHz

101 = 2 MHz

100 = 1 MHz⁽³⁾

011 = 500 kHz

010 = 250 kHz

001 = 125 kHz

000 = 31 kHz (from either INTOSC/256 or INTRC directly)⁽²⁾

bit 3 **OSTS:** Oscillator Start-up Time-out Status bit⁽¹⁾

1 = Oscillator Start-up Timer (OST) time-out has expired; primary oscillator is running

0 = Oscillator Start-up Timer (OST) time-out is running; primary oscillator is not ready

bit 2 **IOFS:** INTOSC Frequency Stable bit

1 = INTOSC frequency is stable

0 = INTOSC frequency is not stable

bit 1-0 **SCS<1:0>:** System Clock Select bits⁽⁴⁾

1x = Internal oscillator block

01 = Secondary (Timer1) oscillator

00 = Primary oscillator

Note 1: Reset state depends on state of the IESO Configuration bit.

2: Source selected by the INTSRC bit (OSCTUNE<7>), see text.

3: Default output frequency of INTOSC on Reset.

4: Modifying the SCS<1:0> bits will cause an immediate clock source switch.

5: Modifying the IRCF<3:0> bits will cause an immediate clock frequency switch if the internal oscillator is providing the device clocks.

FIGURE 4-6: SLOW RISE TIME ($\overline{\text{MCLR}}$ TIED TO V_{DD} , V_{DD} RISE $> T_{PWRT}$)

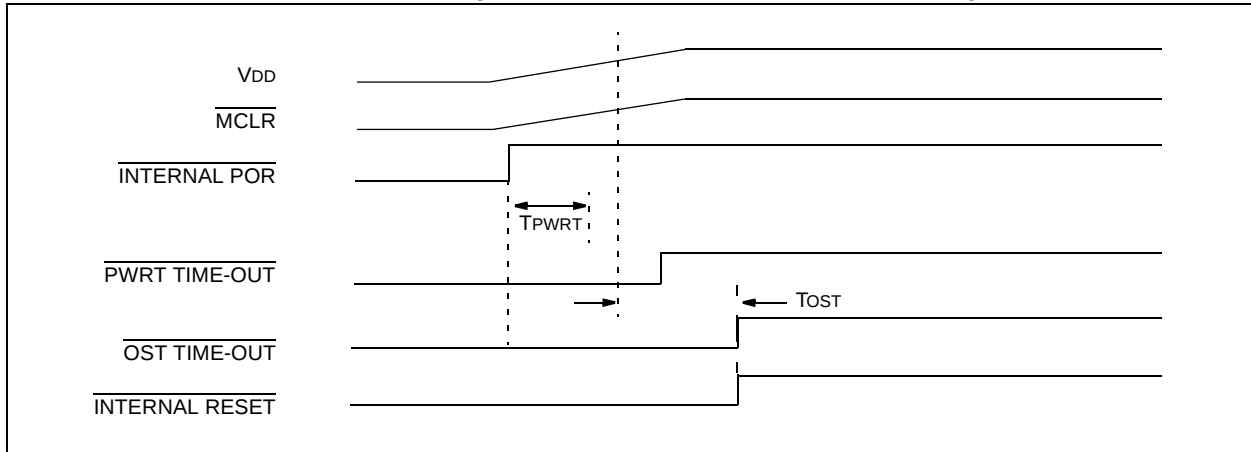


FIGURE 4-7: TIME-OUT SEQUENCE ON POR w/PLL ENABLED ($\overline{\text{MCLR}}$ TIED TO V_{DD})

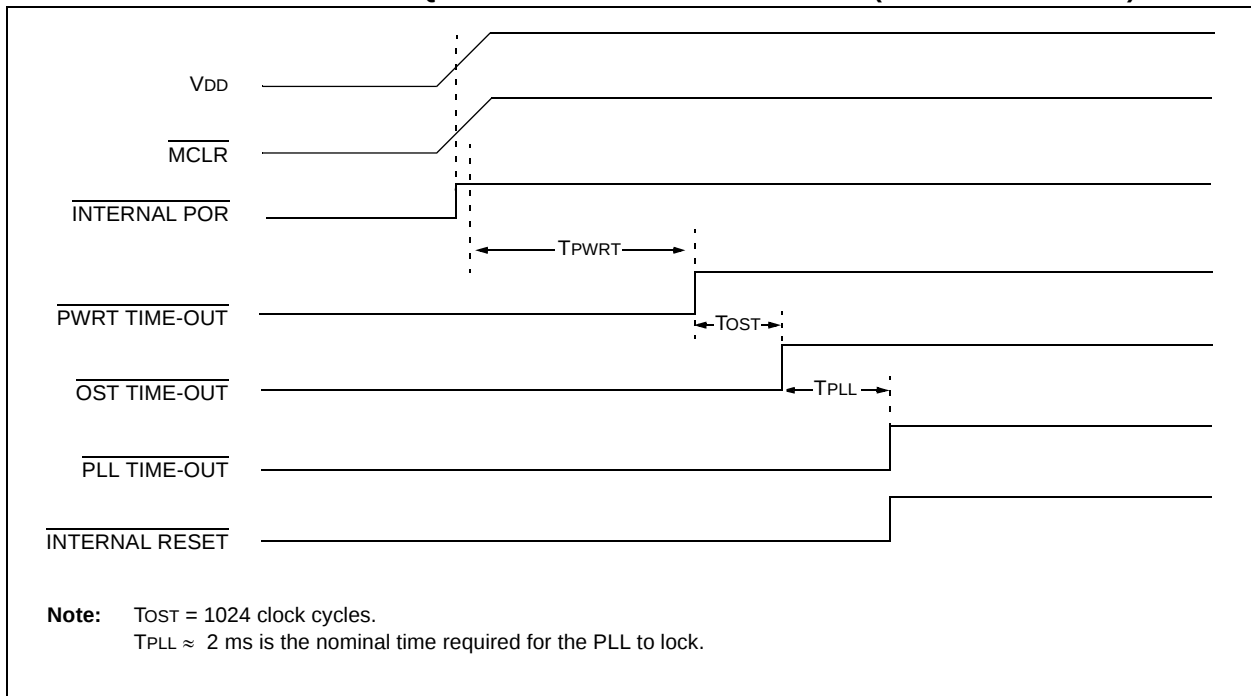
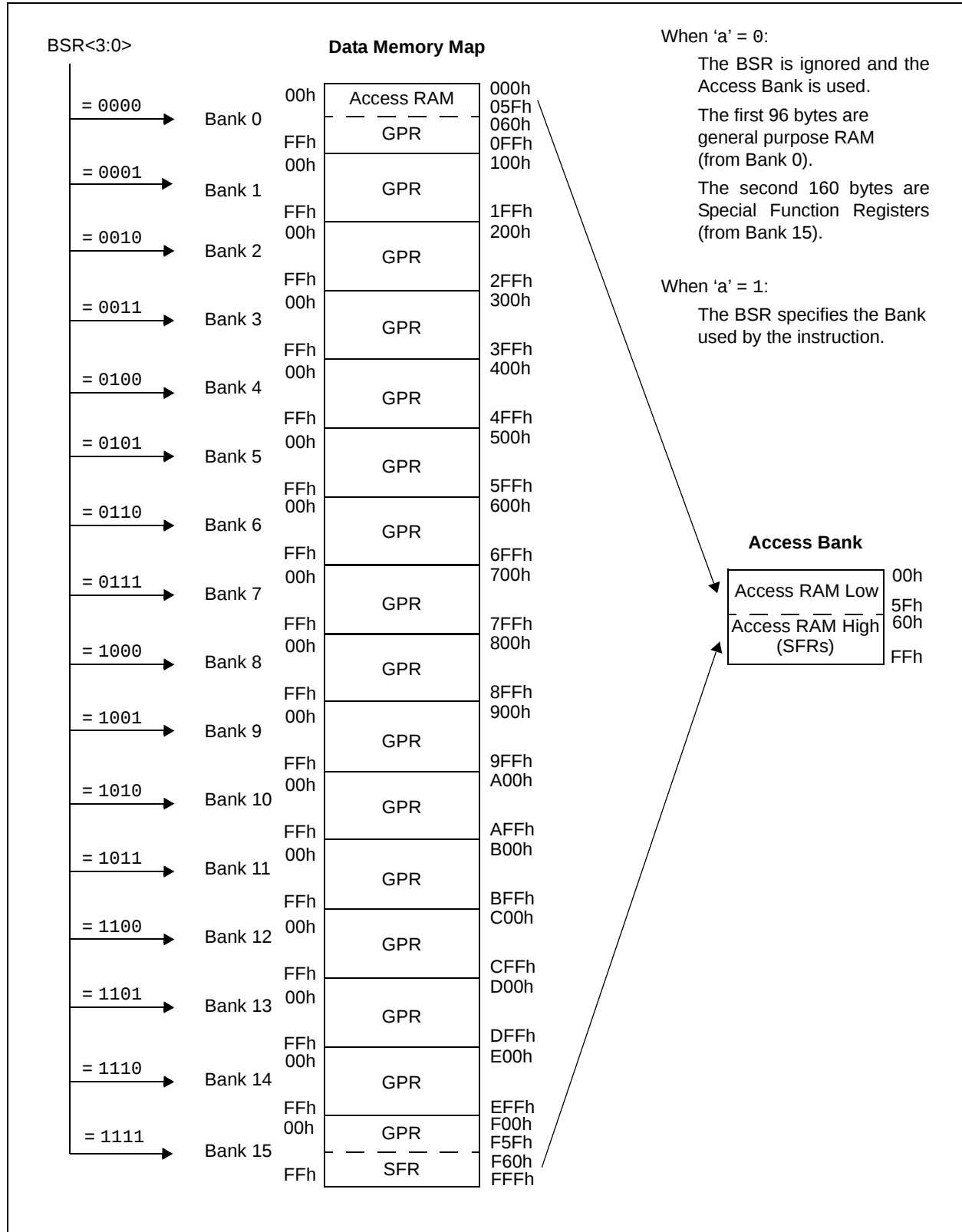


FIGURE 5-6: DATA MEMORY MAP FOR THE PIC18F8722 FAMILY OF DEVICES



PIC18F8722 FAMILY

TABLE 5-3: REGISTER FILE SUMMARY

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
TOSU	—	—	—	Top-of-Stack Upper Byte (TOS<20:16>)					-- -0 0000	57, 66
TOSH	Top-of-Stack High Byte (TOS<15:8>)								0000 0000	57, 66
TOSL	Top-of-Stack Low Byte (TOS<7:0>)								0000 0000	57, 66
STKPTR	STKFUL ⁽⁶⁾	STKUNF ⁽⁶⁾	—	SP4	SP3	SP2	SP1	SP0	00-0 0000	57, 67
PCLATU	—	—	—	Holding Register for PC<20:16>					-- -0 0000	57, 66
PCLATH	Holding Register for PC<15:8>								0000 0000	57, 66
PCL	PC Low Byte (PC<7:0>)								0000 0000	57, 66
TBLPTRU	—	—	bit 21 ⁽⁷⁾	Program Memory Table Pointer Upper Byte (TBLPTR<20:16>)					-- 00 0000	57, 90
TBLPTRH	Program Memory Table Pointer High Byte (TBLPTR<15:8>)								0000 0000	57, 90
TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								0000 0000	57, 90
TABLAT	Program Memory Table Latch								0000 0000	57, 90
PRODH	Product Register High Byte								xxxx xxxx	57, 117
PRODL	Product Register Low Byte								xxxx xxxx	57, 117
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	57, 121
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	INTEDG3	TMR0IP	INT3IP	RBIP	1111 1111	57, 122
INTCON3	INT2IP	INT1IP	INT3IE	INT2IE	INT1IE	INT3IF	INT2IF	INT1IF	1100 0000	57, 123
INDF0	Uses contents of FSR0 to address data memory – value of FSR0 not changed (not a physical register)								N/A	57, 82
POSTINC0	Uses contents of FSR0 to address data memory – value of FSR0 post-incremented (not a physical register)								N/A	57, 82
POSTDEC0	Uses contents of FSR0 to address data memory – value of FSR0 post-decremented (not a physical register)								N/A	57, 82
PREINC0	Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented (not a physical register)								N/A	57, 82
PLUSW0	Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented (not a physical register) – value of FSR0 offset by W								N/A	57, 82
FSR0H	—	—	—	—	Indirect Data Memory Address Pointer 0 High				---- 0000	57, 82
FSR0L	Indirect Data Memory Address Pointer 0 Low Byte								xxxx xxxx	57, 82
WREG	Working Register								xxxx xxxx	57
INDF1	Uses contents of FSR1 to address data memory – value of FSR1 not changed (not a physical register)								N/A	57, 82
POSTINC1	Uses contents of FSR1 to address data memory – value of FSR1 post-incremented (not a physical register)								N/A	57, 82
POSTDEC1	Uses contents of FSR1 to address data memory – value of FSR1 post-decremented (not a physical register)								N/A	57, 82
PREINC1	Uses contents of FSR1 to address data memory – value of FSR1 pre-incremented (not a physical register)								N/A	57, 82
PLUSW1	Uses contents of FSR1 to address data memory – value of FSR1 pre-incremented (not a physical register) – value of FSR1 offset by W								N/A	57, 82
FSR1H	—	—	—	—	Indirect Data Memory Address Pointer 1 High				---- 0000	58, 82
FSR1L	Indirect Data Memory Address Pointer 1 Low Byte								xxxx xxxx	58, 82
BSR	—	—	—	—	Bank Select Register				---- 0000	58, 72
INDF2	Uses contents of FSR2 to address data memory – value of FSR2 not changed (not a physical register)								N/A	58, 82
POSTINC2	Uses contents of FSR2 to address data memory – value of FSR2 post-incremented (not a physical register)								N/A	58, 82
POSTDEC2	Uses contents of FSR2 to address data memory – value of FSR2 post-decremented (not a physical register)								N/A	58, 82
PREINC2	Uses contents of FSR2 to address data memory – value of FSR2 pre-incremented (not a physical register)								N/A	58, 82
PLUSW2	Uses contents of FSR2 to address data memory – value of FSR2 pre-incremented (not a physical register) – value of FSR2 offset by W								N/A	58, 82
FSR2H	—	—	—	—	Indirect Data Memory Address Pointer 2 High				---- 0000	58, 82
FSR2L	Indirect Data Memory Address Pointer 2 Low Byte								xxxx xxxx	58, 82

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition

Note 1: The SBOREN bit is only available when the BOREN<1:0> Configuration bits = 01; otherwise, this bit reads as '0'.

Note 2: These registers and/or bits are not implemented on 64-pin devices and are read as '0'. Reset values are shown for 80-pin devices; individual unimplemented bits should be interpreted as '- '.

Note 3: The PLLEN bit is only available in specific oscillator configuration; otherwise, it is disabled and reads as '0'. See **Section 2.6.4 “PLL in INTOSC Modes”**.

Note 4: RA6/RA7 and their associated latch and direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

Note 5: RG5 and LATG5 are only available when Master Clear is disabled (MCLRE Configuration bit = 0); otherwise, RG5 and LATG5 read as '0'.

Note 6: Bit 7 and Bit 6 are cleared by user software or by a POR.

Note 7: Bit 21 of TBLPTRU allows access to the device Configuration bits.

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REGISTER 10-11: IPR2: PERIPHERAL INTERRUPT PRIORITY REGISTER 2

R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
OSCFIP	CMIP	—	EEIP	BCL1IP	HLVDIP	TMR3IP	CCP2IP
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	OSCFIP: Oscillator Fail Interrupt Priority bit 1 = High priority 0 = Low priority
bit 6	CMIP: Comparator Interrupt Priority bit 1 = High priority 0 = Low priority
bit 5	Unimplemented: Read as '0'
bit 4	EEIP: Interrupt Priority bit 1 = High priority 0 = Low priority
bit 3	BCL1IP: MSSP1 Bus Collision Interrupt Priority bit 1 = High priority 0 = Low priority
bit 2	HLVDIP: High/Low-Voltage Detect Interrupt Priority bit 1 = High priority 0 = Low priority
bit 1	TMR3IP: TMR3 Overflow Interrupt Priority bit 1 = High priority 0 = Low priority
bit 0	CCP2IP: ECCP2 Interrupt Priority bit 1 = High priority 0 = Low priority

11.4 PORTD, TRISD and LATD Registers

PORTD is an 8-bit wide, bidirectional port. The corresponding Data Direction register is TRISD. Setting a TRISD bit (= 1) will make the corresponding PORTD pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISD bit (= 0) will make the corresponding PORTD pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATD) is also memory mapped. Read-modify-write operations on the LATD register read and write the latched output value for PORTD.

All pins on PORTD are implemented with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

Note: On a Power-on Reset, these pins are configured as digital inputs.

In 80-pin devices, PORTD is multiplexed with the system bus as part of the external memory interface. I/O port and other functions are only available when the interface is disabled by setting the EBDIS bit (MEMCON<7>). When the interface is enabled, PORTD is the low-order byte of the multiplexed address/data bus (AD<7:0>). The TRISD bits are also overridden.

PORTD can also be configured to function as an 8-bit wide parallel microprocessor port by setting the PSPMODE control bit (PSPCON<4>). In this mode, parallel port data takes priority over other digital I/O (but not the external memory interface). When the parallel port is active, the input buffers are TTL. For more information, refer to **Section 11.10 “Parallel Slave Port”**.

EXAMPLE 11-4: INITIALIZING PORTD

```
CLRF    PORTD    ; Initialize PORTD by
                  ; clearing output
                  ; data latches
CLRF    LATD     ; Alternate method
                  ; to clear output
                  ; data latches
MOVLW   0CFh     ; Value used to
                  ; initialize data
                  ; direction
MOVWF   TRISD    ; Set RD<3:0> as inputs
                  ; RD<5:4> as outputs
                  ; RD<7:6> as inputs
```

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TABLE 11-7: PORTD FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RD0/AD0/PSP0	RD0	0	O	DIG	LATD<0> data output.
		1	I	ST	PORTD<0> data input.
	AD0 ⁽¹⁾	x	O	DIG	External memory interface, address/data bit 0 output. Takes priority over PSP and port data.
		x	I	TTL	External memory interface, data bit 0 input.
	PSP0	x	O	DIG	PSP read data output (LATD<0>). Takes priority over port data.
		x	I	TTL	PSP write data input.
RD1/AD1/PSP1	RD1	0	O	DIG	LATD<1> data output.
		1	I	ST	PORTD<1> data input.
	AD1 ⁽¹⁾	x	O	DIG	External memory interface, address/data bit 1 output. Takes priority over PSP and port data.
		x	I	TTL	External memory interface, data bit 1 input.
	PSP1	x	O	DIG	PSP read data output (LATD<1>). Takes priority over port data.
		x	I	TTL	PSP write data input.
RD2/AD2/PSP2	RD2	0	O	DIG	LATD<2> data output.
		1	I	ST	PORTD<2> data input.
	AD2 ⁽¹⁾	x	O	DIG	External memory interface, address/data bit 2 output. Takes priority over PSP and port data.
		x	I	TTL	External memory interface, data bit 2 input.
	PSP2	x	O	DIG	PSP read data output (LATD<2>). Takes priority over port data.
		x	I	TTL	PSP write data input.
RD3/AD3/PSP3	RD3	0	O	DIG	LATD<3> data output.
		1	I	ST	PORTD<3> data input.
	AD3 ⁽¹⁾	x	O	DIG	External memory interface, address/data bit 3 output. Takes priority over PSP and port data.
		x	I	TTL	External memory interface, data bit 3 input.
	PSP3	x	O	DIG	PSP read data output (LATD<3>). Takes priority over port data.
		x	I	TTL	PSP write data input.
RD4/AD4/ PSP4/SDO2	RD4	0	O	DIG	LATD<4> data output.
		1	I	ST	PORTD<4> data input.
	AD4 ⁽¹⁾	x	O	DIG	External memory interface, address/data bit 4 output. Takes priority over PSP, MSSP and port data.
		x	I	TTL	External memory interface, data bit 4 input.
	PSP4	x	O	DIG	PSP read data output (LATD<4>). Takes priority over port and PSP data.
		x	I	TTL	PSP write data input.
	SDO2	0	O	DIG	SPI data output (MSSP2 module). Takes priority over PSP and port data.

Legend: PWR = Power Supply, O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: Implemented on 80-pin devices only.

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TABLE 11-14: SUMMARY OF REGISTERS ASSOCIATED WITH PORTG

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTG	—	—	RG5 ⁽¹⁾	RG4	RG3	RG2	RG1	RG0	60
LATG	—	—	LATG5 ⁽¹⁾	LATG4	LATG3	LATG2	LATG1	LATG0	60
TRISG	—	—	—	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0	60

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTG.

Note 1: RG5 and LATG5 are only available when MCLR is disabled (MCLRE Configuration bit = 0; otherwise, RG5 and LATG5 read as '0'.

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19.4.3.2 Reception

When the $\overline{R/W}$ bit of the address byte is clear and an address match occurs, the $\overline{R/W}$ bit of the SSPxSTAT register is cleared. The received address is loaded into the SSPxBUF register and the SDAx line is held low ($\overline{ACK}$).

When the address byte overflow condition exists, then the no Acknowledge ($\overline{ACK}$) pulse is given. An overflow condition is defined as either bit BF (SSPxSTAT<0>) is set, or bit SSPOV (SSPxCON1<6>) is set.

An MSSP interrupt is generated for each data transfer byte. The interrupt flag bit, SSPxIF, must be cleared in software. The SSPxSTAT register is used to determine the status of the byte.

If SEN is enabled (SSPxCON2<0> = 1), SCLx will be held low (clock stretch) following each data transfer. The clock must be released by setting bit, CKP (SSPxCON1<4>). See **Section 19.4.4 “Clock Stretching”** for more detail.

19.4.3.3 Transmission

When the $\overline{R/W}$ bit of the incoming address byte is set and an address match occurs, the $\overline{R/W}$ bit of the SSPxSTAT register is set. The received address is loaded into the SSPxBUF register. The $\overline{ACK}$ pulse will be sent on the ninth bit and pin SCLx is held low regardless of SEN (see **Section 19.4.4 “Clock Stretching”** for more detail). By stretching the clock, the master will be unable to assert another clock pulse until the slave is done preparing the transmit data. The transmit data must be loaded into the SSPxBUF register which also loads the SSPxSR register. Then pin SCLx should be enabled by setting bit, CKP (SSPxCON1<4>). The eight data bits are shifted out on the falling edge of the SCLx input. This ensures that the SDAx signal is valid during the SCLx high time (Figure 19-9).

The $\overline{ACK}$ pulse from the master-receiver is latched on the rising edge of the ninth SCLx input pulse. If the SDAx line is high (not $\overline{ACK}$), then the data transfer is complete. In this case, when the $\overline{ACK}$ is latched by the slave, the slave logic is reset (resets SSPxSTAT register) and the slave monitors for another occurrence of the Start bit. If the SDAx line was low ($\overline{ACK}$), the next transmit data must be loaded into the SSPxBUF register. Again, pin SCLx must be enabled by setting bit CKP.

An MSSP interrupt is generated for each data transfer byte. The SSPxIF bit must be cleared in software and the SSPxSTAT register is used to determine the status of the byte. The SSPxIF bit is set on the falling edge of the ninth clock pulse.

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REGISTER 25-5: CONFIG3H: CONFIGURATION REGISTER 3 HIGH (BYTE ADDRESS 300005h)

R/P-1	U-0	U-0	U-0	U-0	R/P-0	R/P-1	R/P-1
MCLRE	—	—	—	—	LPT1OSC	ECCPMX ⁽¹⁾	CCP2MX
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **MCLRE:** MCLR Pin Enable bit

1 = MCLR pin enabled; RG5 input pin disabled

0 = RG5 input pin enabled; MCLR disabled

bit 6-3 **Unimplemented:** Read as '0'

bit 2 **LPT1OSC:** Low-Power Timer1 Oscillator Enable bit

1 = Timer1 configured for low-power operation

0 = Timer1 configured for higher power operation

bit 1 **ECCPMX:** ECCP MUX bit⁽¹⁾

1 = ECCP1/3 (P1B/P1C/P3B/P3C) are multiplexed onto RE6, RE5, RE4 and RE3 respectively

0 = ECCP1/3 (P1B/P1C/P3B/P3C) are multiplexed onto RH7, RH6, RH5 and RH4 respectively

bit 0 **CCP2MX:** CCP2 MUX bit

1 = ECCP2 input/output is multiplexed with RC1

0 = ECCP2 input/output is multiplexed with RB3 in Extended Microcontroller, Microprocessor or Microprocessor with Boot Block mode⁽¹⁾. ECCP2 is multiplexed with RE7 in Microcontroller mode.

Note 1: This feature is only available on PIC18F8527/8622/8627/8722 devices.

PIC18F8722 FAMILY

28.2 DC Characteristics: Power-Down and Supply Current PIC18F6X27/6X22/8X27/8X22 (Industrial, Extended) PIC18LF6X27/6X22/8X27/8X22 (Industrial) (Continued)

PIC18LF6X27/6X22/8X27/8X22 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F6X27/6X22/8X27/8X22 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (IDD) ⁽²⁾						
	All devices	9.0	13	mA	-40°C	VDD = 4.2V	Fosc = 4 MHz, 16 MHz internal (PRI_RUN HS+PLL)
		9.0	13	mA	+25°C		
		9.0	13	mA	+85°C		
	Extended devices only	9.6	15	mA	+125°C		
	All devices	12	15	mA	-40°C	VDD = 5.0V	Fosc = 4 MHz, 16 MHz internal (PRI_RUN HS+PLL)
		12	15	mA	+25°C		
		12	15	mA	+85°C		
	Extended devices only	12	17	mA	+125°C		
	All devices	18	23.5	mA	-40°C	VDD = 4.2V	Fosc = 10 MHz, 40 MHz internal (PRI_RUN HS+PLL)
		19	23.5	mA	+25°C		
		19	23.5	mA	+85°C		
	All devices	25	29	mA	-40°C	VDD = 5.0V	Fosc = 10 MHz, 40 MHz internal (PRI_RUN HS+PLL)
		25	29	mA	+25°C		
25		29	mA	+85°C			

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
 OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} or V_{SS} ;
 $\text{MCLR} = V_{DD}$; WDT enabled/disabled as specified.
- 3:** When operation below -10°C is expected, use T1OSC High-Power mode, where LPT1OSC (CONFIG3H<2>) = 0. When operation will always be above -10°C , then the low-power Timer1 oscillator may be selected.
- 4:** BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

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28.2 DC Characteristics: Power-Down and Supply Current PIC18F6X27/6X22/8X27/8X22 (Industrial, Extended) PIC18LF6X27/6X22/8X27/8X22 (Industrial) (Continued)

PIC18LF6X27/6X22/8X27/8X22 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F6X27/6X22/8X27/8X22 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device	Typ	Max	Units	Conditions		
D026 (ΔIAD)	A/D Converter	0.2	1	μA	-40°C to +85°C	VDD = 2.0V	A/D on, not converting, Sleep mode
		0.2	1	μA	-40°C to +85°C	VDD = 3.0V	
		0.2	1	μA	-40°C to +85°C	VDD = 5.0V	
		0.5	4	μA	-40°C to +125°C		

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
 OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} or V_{SS} ;
 $\text{MCLR} = V_{DD}$; WDT enabled/disabled as specified.
- 3:** When operation below -10°C is expected, use T1OSC High-Power mode, where LPT1OSC (CONFIG3H<2>) = 0. When operation will always be above -10°C , then the low-power Timer1 oscillator may be selected.
- 4:** BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

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28.3 DC Characteristics: PIC18F8722 (Industrial, Extended) PIC18LF6X27/6X22/8X27/8X22 (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial			
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
D030 D030A D031 D032 D033 D033A D033B D034	V_{IL}	Input Low Voltage I/O Ports: with TTL Buffer with Schmitt Trigger Buffer $\overline{\text{MCLR}}$ OSC1 OSC1 OSC1 T13CKI	V_{SS} — V_{SS} V_{SS} V_{SS} V_{SS} V_{SS} V_{SS}	$0.15 V_{DD}$ 0.8 $0.2 V_{DD}$ $0.2 V_{DD}$ $0.3 V_{DD}$ $0.2 V_{DD}$ 0.3 0.3	V V V V V V V V	$V_{DD} < 4.5\text{V}$ $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ HS, HSPLL modes RC, EC modes ⁽¹⁾ XT, LP modes
D040 D040A D041 D042 D043 D043A D043B D043C D044	V_{IH}	Input High Voltage I/O Ports: with TTL Buffer with Schmitt Trigger Buffer $\overline{\text{MCLR}}$ OSC1 OSC1 OSC1 OSC1 T13CKI	$0.25 V_{DD} + 0.8\text{V}$ 2.0 $0.8 V_{DD}$ $0.8 V_{DD}$ $0.7 V_{DD}$ $0.8 V_{DD}$ $0.9 V_{DD}$ 1.6 1.6	V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD}	V V V V V V V V V	$V_{DD} < 4.5\text{V}$ $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ HS, HSPLL modes EC mode RC mode ⁽¹⁾ XT, LP modes
D060 D061 D063	I_{IL}	Input Leakage Current^(2,3) I/O Ports $\overline{\text{MCLR}}$ OSC1	— — — —	± 200 ± 50 ± 1 ± 1	nA nA μA μA	$V_{DD} < 5.5\text{V}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at high-impedance $V_{DD} < 3\text{V}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at high-impedance $V_{SS} \leq V_{PIN} \leq V_{DD}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$
D070	IPU IPURB	Weak Pull-up Current PORTB Weak Pull-up Current	50	400	μA	$V_{DD} = 5\text{V}$, $V_{PIN} = V_{SS}$

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC® device be driven with an external clock while in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

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TABLE 28-7: PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 4.2V TO 5.5V)

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
F10	FOSC	Oscillator Frequency Range	4	—	10	MHz	HS mode only
F11	FSYS	On-Chip VCO System Frequency	16	—	40	MHz	HS mode only
F12	t _{rc}	PLL Start-up Time (Lock Time)	—	—	2	ms	
F13	ΔCLK	CLKO Stability (Jitter)	-2	—	+2	%	

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 28-8: AC CHARACTERISTICS: INTERNAL RC ACCURACY

PIC18F6X27/6X22/8X27/8X22 (INDUSTRIAL, EXTENDED)

PIC18LF6X27/6X22/8X27/8X22 (INDUSTRIAL)

PIC18LF6X27/6X22/8X27/8X22 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F6X27/6X22/8X27/8X22 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device	Min	Typ	Max	Units	Conditions	
	INTOSC Accuracy @ Freq = 8 MHz, 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz ⁽¹⁾						
	PIC18LF6X27/6X22/8X27/8X22	-2	+/-1	2	%	+25°C	VDD = 2.7-3.3V
		-5	+/-1	5	%	-40°C to +85°C	VDD = 2.7-3.3V
	PIC18F6X27/6X22/8X27/8X22	-2	+/-1	2	%	+25°C	VDD = 4.5-5.5V
		-5	+/-1	5	%	-40°C to +85°C	VDD = 4.5-5.5V
	INTRC Accuracy @ Freq = 31 kHz						
	PIC18LF6X27/6X22/8X27/8X22	26.562	—	35.938	kHz	-40°C to +85°C	VDD = 2.7-3.3V
	PIC18F6X27/6X22/8X27/8X22	26.562	+/-8	35.938	kHz	-40°C to +85°C	VDD = 4.5-5.5V

Legend: Shading of rows is to assist in readability of the table.

Note 1: Frequency calibrated at 25°C. OSCUNE register can be used to compensate for temperature drift.

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FIGURE 28-16: EXAMPLE SPI MASTER MODE TIMING (CKE = 1)

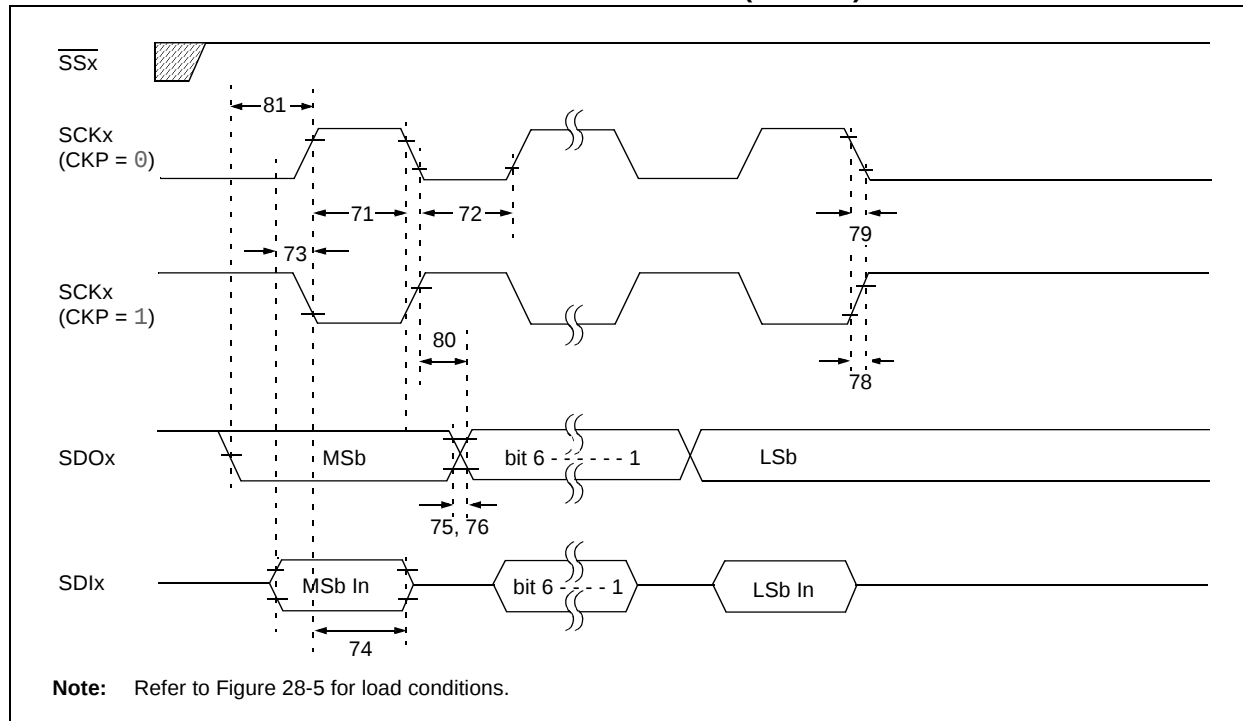


TABLE 28-17: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
71	Tsch	SCKx Input High Time (Slave mode)	Continuous	1.25 Tcy + 30	—	ns	
71A			Single Byte	40	—	ns	(Note 1)
72	Tscl	SCKx Input Low Time (Slave mode)	Continuous	1.25 Tcy + 30	—	ns	
72A			Single Byte	40	—	ns	(Note 1)
73	TdIV2sch, TdIV2scl	Setup Time of SDIx Data Input to SCKx Edge		20	—	ns	
73A	Tb2B	Last Clock Edge of Byte 1 to the 1st Clock Edge of Byte 2		1.5 Tcy + 40	—	ns	(Note 2)
74	Tsch2dIL, TscL2dIL	Hold Time of SDIx Data Input to SCKx Edge		40	—	ns	
75	TdoR	SDOx Data Output Rise Time	PIC18FXXXXX	—	25	ns	
			PIC18LFXXXXX	—	45	ns	VDD = 2.0V
76	TdoF	SDOx Data Output Fall Time		—	25	ns	
78	TscR	SCKx Output Rise Time (Master mode)	PIC18FXXXXX	—	25	ns	
			PIC18LFXXXXX	—	45	ns	VDD = 2.0V
79	TscF	SCKx Output Fall Time (Master mode)		—	25	ns	
80	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	PIC18FXXXXX	—	50	ns	
			PIC18LFXXXXX	—	100	ns	VDD = 2.0V
81	TdoV2sch, TdoV2scl	SDOx Data Output Setup to SCKx Edge		Tcy	—	ns	

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.

FIGURE 28-19: I²C™ BUS START/STOP BITS TIMING

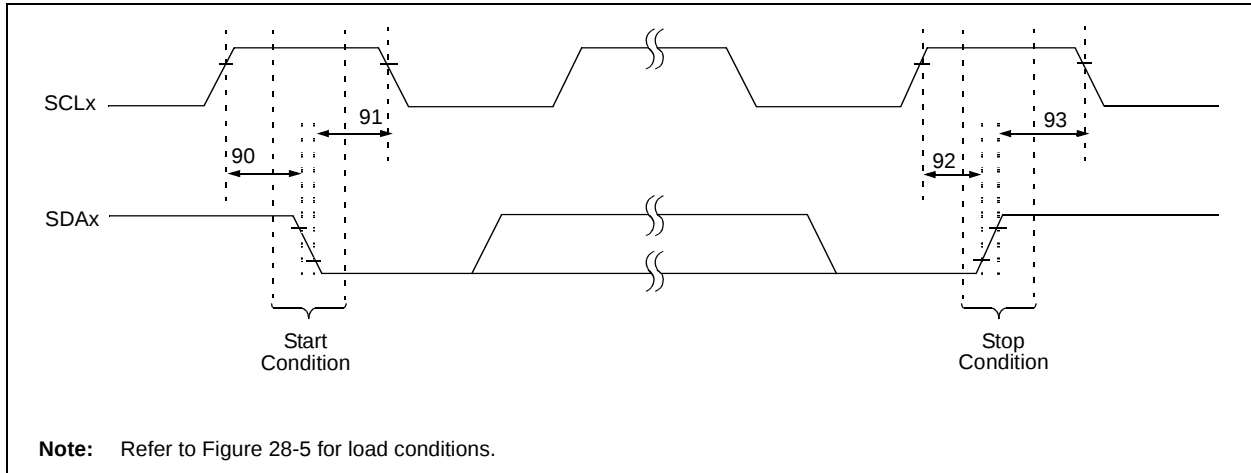
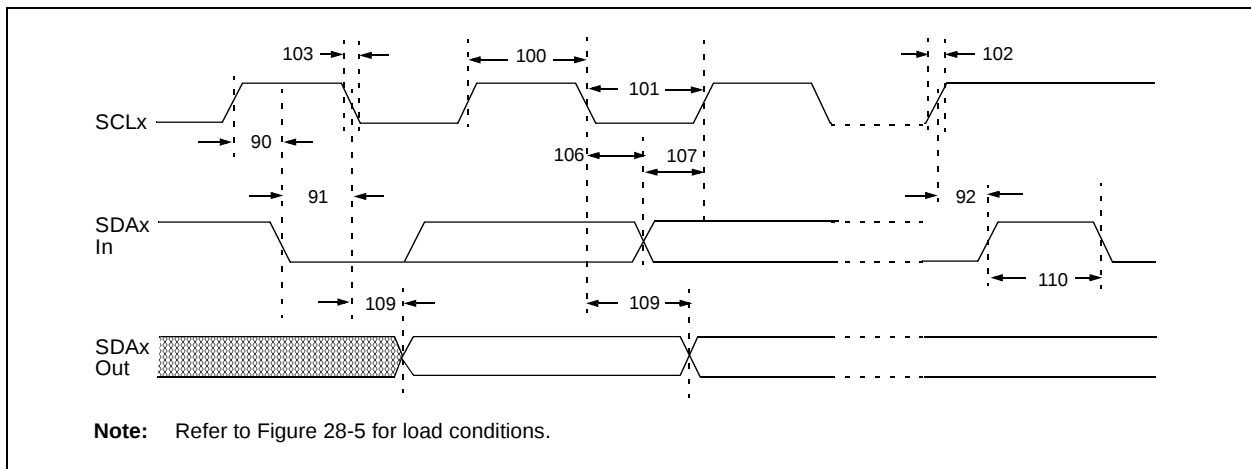


TABLE 28-20: I²C™ BUS START/STOP BITS REQUIREMENTS (SLAVE MODE)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
90	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—		
91	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—		
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	4700	—	ns	
			400 kHz mode	600	—		
93	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—		

FIGURE 28-20: I²C™ BUS DATA TIMING



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RH7/AN15/P1B	29
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RJ1/OE	30
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RJ3/WRH	30
RJ4/BA0	30
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