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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	70
Program Memory Size	96KB (48K × 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf8627t-i-pt

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Pin Name	Pin Number	Pin	Buffer	Description		
	TQFP	Туре	Туре	Description		
				PORTC is a bidirectional I/O port.		
RC0/T1OSO/T13CKI RC0 T1OSO T13CKI	30	I/O O I	ST — ST	Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.		
RC1/T1OSI/ECCP2/P2A RC1 T1OSI ECCP2 ⁽¹⁾	29	I/O I I/O	ST CMOS ST	Digital I/O. Timer1 oscillator input. Enhanced Capture 2 input/Compare 2 output/ PWM 2 output.		
P2A ⁽¹⁾		0	—	ECCP2 PWM output A.		
RC2/ECCP1/P1A RC2 ECCP1	33	I/O I/O	ST ST	Digital I/O. Enhanced Capture 1 input/Compare 1 output/ PWM 1 output		
P1A		0	_	ECCP1 PWM output A.		
RC3/SCK1/SCL1 RC3 SCK1 SCL1	34	I/O I/O I/O	ST ST ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C™ mode.		
RC4/SDI1/SDA1 RC4 SDI1 SDA1	35	I/O I I/O	ST ST ST	Digital I/O. SPI data in. I ² C data I/O.		
RC5/SDO1 RC5 SDO1	36	I/O O	ST —	Digital I/O. SPI data out.		
RC6/TX1/CK1 RC6 TX1 CK1	31	I/O O I/O	ST — ST	Digital I/O. EUSART1 asynchronous transmit. EUSART1 synchronous clock (see related RX1/DT1).		
RC7/RX1/DT1 RC7 RX1 DT1	32	I/O I I/O	ST ST ST	Digital I/O. EUSART1 asynchronous receive. EUSART1 synchronous data (see related TX1/CK1).		
Legend: TTL = TTL co	mpatible input		S DS lovele	= CMOS compatible input or output		
SI = Schmitt Trigger input with CMOS levels Analog = Analog input I = Input O = Output P = Power l^2C^{TM} = $l^2C/SMBus$ input buffer Note 1: Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.						

TABLE 1-3: PIC18F6527/6622/6627/6722 PINOUT I/O DESCRIPTIONS (CONTINUED)

2: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

Din Nome	Pin Number	Pin	Buffer	Description		
Pin Name	TQFP	Туре	Туре	Description		
				PORTG is a bidirectional I/O port.		
RG0/ECCP3/P3A RG0 ECCP3	5	I/O I/O	ST ST	Digital I/O. Enhanced Capture 3 input/Compare 3 output/ PW/M 3 output		
P3A		0	—	ECCP3 PWM output A.		
RG1/TX2/CK2 RG1 TX2 CK2	6	I/O O I/O	ST — ST	Digital I/O. EUSART2 asynchronous transmit. EUSART2 synchronous clock (see related RX2/DT2).		
RG2/RX2/DT2 RG2 RX2 DT2	7	I/O I I/O	ST ST ST	Digital I/O. EUSART2 asynchronous receive. EUSART2 synchronous data (see related TX2/CK2).		
RG3/CCP4/P3D RG3 CCP4 P3D	8	I/O I/O O	ST ST —	Digital I/O. Capture 4 input/Compare 4 output/PWM 4 output. ECCP3 PWM output D.		
RG4/CCP5/P1D RG4 CCP5 P1D	10	I/O I/O O	ST ST —	Digital I/O. Capture 5 input/Compare 5 output/PWM 5 output. ECCP1 PWM output D.		
RG5				See RG5/MCLR/VPP pin.		
Legend: TTL = TTL co ST = Schmi I = Input P = Power	ompatible input tt Trigger input	npatible input CMOS = CMOS compatible input or output Trigger input with CMOS levels Analog = Analog input O = Output ¹² OCTM/CMP				
Note 1: Alternate assi Microcontrolle	 Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode). 					

TABLE 1-4: PIC18F8527/8622/8627/8722 PINOUT I/O DESCRIPTIONS (CONTINUED)

2: Default assignment for ECCP2 in all operating modes (CCP2MX is set).

3: Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

4: Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

5: Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

Din Nome	Pin Number	Pin	Buffer	Description			
Pin Name	TQFP	Туре	Туре	Description			
				PORTJ is a bidirectional I/O port.			
RJ0/ALE RJ0 ALE	62	I/O O	ST —	Digital I/O. External memory address latch enable.			
RJ1/OE RJ1 OE	61	I/O O	ST —	Digital I/O. External memory output enable.			
RJ2/WRL RJ2 WRL	60	I/O O	ST —	Digital I/O. External memory write low control.			
RJ3/WRH RJ3 WRH	59	I/O O	ST —	Digital I/O. External memory write high control.			
RJ4/BA0 RJ4 BA0	39	I/O O	ST —	Digital I/O. External memory byte address 0 control.			
RJ5/CE RJ4 CE	40	I/O O	ST —	Digital I/O External memory chip enable control.			
RJ6/LB RJ6 LB	41	I/O O	ST —	Digital I/O. External memory low byte control.			
RJ7/UB RJ7 UB	42	I/O O	ST —	Digital I/O. External memory high byte control.			
Vss	11, 31, 51, 70	Р	—	Ground reference for logic and I/O pins.			
Vdd	12, 32, 48, 71	Р	—	Positive supply for logic and I/O pins.			
AVss	26	Р		Ground reference for analog modules.			
AVDD	25	Р		Positive supply for analog modules.			
Legend: TTL = TTL co	ompatible input	Р СМС)S	= CMOS compatible input or output			

TABLE 1-4: PIC18F8527/8622/8627/8722 PINOUT I/O DESCRIPTIONS (CONTINUED)

ST = Schmitt Trigger input with CMOS levels Analog= Analog input = Output

= Input Т Ο = Power Ρ

I²C[™]/SMB = I²C/SMBus input buffer

Note 1: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

2: Default assignment for ECCP2 in all operating modes (CCP2MX is set).

3: Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

4: Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

5: Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

Register	Applicable Devices		Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt		
TOSU	6X27	6X22	8X27	8X22	0 0000	0 0000	0 uuuu (3)
TOSH	6X27	6X22	8X27	8X22	0000 0000	0000 0000	uuuu uuuu ⁽³⁾
TOSL	6X27	6X22	8X27	8X22	0000 0000	0000 0000	uuuu uuuu (3)
STKPTR	6X27	6X22	8X27	8X22	00-0 0000	uu-u uuuu	uu-u uuuu (3)
PCLATU	6X27	6X22	8X27	8X22	0 0000	0 0000	u uuuu
PCLATH	6X27	6X22	8X27	8X22	0000 0000	0000 0000	uuuu uuuu
PCL	6X27	6X22	8X27	8X22	0000 0000	0000 0000	PC + 2 ⁽²⁾
TBLPTRU	6X27	6X22	8X27	8X22	00 0000	00 0000	uu uuuu
TBLPTRH	6X27	6X22	8X27	8X22	0000 0000	0000 0000	uuuu uuuu
TBLPTRL	6X27	6X22	8X27	8X22	0000 0000	0000 0000	uuuu uuuu
TABLAT	6X27	6X22	8X27	8X22	0000 0000	0000 0000	uuuu uuuu
PRODH	6X27	6X22	8X27	8X22	xxxx xxxx	uuuu uuuu	uuuu uuuu
PRODL	6X27	6X22	8X27	8X22	xxxx xxxx	սսսս սսսս	uuuu uuuu
INTCON	6X27	6X22	8X27	8X22	0000 000x	0000 000u	uuuu uuuu (1)
INTCON2	6X27	6X22	8X27	8X22	1111 1111	1111 1111	uuuu uuuu ⁽¹⁾
INTCON3	6X27	6X22	8X27	8X22	1100 0000	1100 0000	uuuu uuuu (1)
INDF0	6X27	6X22	8X27	8X22	N/A	N/A	N/A
POSTINC0	6X27	6X22	8X27	8X22	N/A	N/A	N/A
POSTDEC0	6X27	6X22	8X27	8X22	N/A	N/A	N/A
PREINC0	6X27	6X22	8X27	8X22	N/A	N/A	N/A
PLUSW0	6X27	6X22	8X27	8X22	N/A	N/A	N/A
FSR0H	6X27	6X22	8X27	8X22	0000	0000	uuuu
FSR0L	6X27	6X22	8X27	8X22	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	6X27	6X22	8X27	8X22	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF1	6X27	6X22	8X27	8X22	N/A	N/A	N/A
POSTINC1	6X27	6X22	8X27	8X22	N/A	N/A	N/A
POSTDEC1	6X27	6X22	8X27	8X22	N/A	N/A	N/A
PREINC1	6X27	6X22	8X27	8X22	N/A	N/A	N/A
PLUSW1	6X27	6X22	8X27	8X22	N/A	N/A	N/A

TABLE 4-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

4: See Table 4-3 for Reset value for specific condition.

5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled, depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

The PLUSW register can be used to implement a form of Indexed Addressing in the data memory space. By manipulating the value in the W register, users can reach addresses that are fixed offsets from pointer addresses. In some applications, this can be used to implement some powerful program control structure, such as software stacks, inside of data memory.

5.4.3.3 Operations by FSRs on FSRs

Indirect Addressing operations that target other FSRs or virtual registers represent special cases. For example, using an FSR to point to one of the virtual registers will not result in successful operations. As a specific case, assume that FSR0H:FSR0L contains FE7h, the address of INDF1. Attempts to read the value of the INDF1 using INDF0 as an operand will return 00h. Attempts to write to INDF1 using INDF0 as the operand will result in a NOP.

On the other hand, using the virtual registers to write to an FSR pair may not occur as planned. In these cases, the value will be written to the FSR pair but without any incrementing or decrementing. Thus, writing to INDF2 or POSTDEC2 will write the same value to the FSR2H:FSR2L.

Since the FSRs are physical registers mapped in the SFR space, they can be manipulated through all direct operations. Users should proceed cautiously when working on these registers, particularly if their code uses Indirect Addressing.

Similarly, operations by Indirect Addressing are generally permitted on all other SFRs. Users should exercise the appropriate caution that they do not inadvertently change settings that might affect the operation of the device.

5.5 Data Memory and the Extended Instruction Set

Enabling the PIC18 extended instruction set (XINST Configuration bit = 1) significantly changes certain aspects of data memory and its addressing. Specifically, the use of the Access Bank for many of the core PIC18 instructions is different; this is due to the introduction of a new addressing mode for the data memory space.

What does not change is just as important. The size of the data memory space is unchanged, as well as its linear addressing. The SFR map remains the same. Core PIC18 instructions can still operate in both Direct and Indirect Addressing mode; inherent and literal instructions do not change at all. Indirect Addressing with FSR0 and FSR1 also remain unchanged.

5.5.1 INDEXED ADDRESSING WITH LITERAL OFFSET

Enabling the PIC18 extended instruction set changes the behavior of Indirect Addressing using the FSR2 register pair within Access RAM. Under the proper conditions, instructions that use the Access Bank – that is, most bit-oriented and byte-oriented instructions – can invoke a form of Indexed Addressing using an offset specified in the instruction. This special addressing mode is known as Indexed Addressing with Literal Offset, or Indexed Literal Offset mode.

When using the extended instruction set, this addressing mode requires the following:

- The use of the Access Bank is forced ('a' = 0) and
- The file address argument is less than or equal to 5Fh.

Under these conditions, the file address of the instruction is not interpreted as the lower byte of an address (used with the BSR in Direct Addressing), or as an 8-bit address in the Access Bank. Instead, the value is interpreted as an offset value to an address pointer, specified by FSR2. The offset and the contents of FSR2 are added to obtain the target address of the operation.

5.5.2 INSTRUCTIONS AFFECTED BY INDEXED LITERAL OFFSET MODE

Any of the core PIC18 instructions that can use Direct Addressing are potentially affected by the Indexed Literal Offset Addressing mode. This includes all byte-oriented and bit-oriented instructions, or almost one-half of the standard PIC18 instruction set. Instructions that only use Inherent or Literal Addressing modes are unaffected.

Additionally, byte-oriented and bit-oriented instructions are not affected if they do not use the Access Bank (Access RAM bit is '1'), or include a file address of 60h or above. Instructions meeting these criteria will continue to execute as before. A comparison of the different possible addressing modes when the extended instruction set is enabled in shown in Figure 5-9.

Those who desire to use byte-oriented or bit-oriented instructions in the Indexed Literal Offset mode should note the changes to assembler syntax for this mode. This is described in more detail in **Section 26.2.1** "Extended Instruction Syntax".

FIGURE 6-2: TABLE WRITE OPERATION



6.2 Control Registers

Several control registers are used in conjunction with the TBLRD and TBLWT instructions. These include the:

- EECON1 register
- EECON2 register
- TABLAT register
- TBLPTR registers

6.2.1 EECON1 AND EECON2 REGISTERS

The EECON1 register (Register 6-1) is the control register for memory accesses. The EECON2 register is not a physical register; it is used exclusively in the memory write and erase sequences. Reading EECON2 will read all '0's.

The EEPGD control bit determines if the access will be a program or data EEPROM memory access. When clear, any subsequent operations will operate on the data EEPROM memory. When set, any subsequent operations will operate on the program memory.

The CFGS control bit determines if the access will be to the Configuration/Calibration registers or to program memory/data EEPROM memory. When set, subsequent operations will operate on Configuration registers regardless of EEPGD (see **Section 25.0** "**Special Features of the CPU**"). When clear, memory selection access is determined by EEPGD.

The FREE bit, when set, will allow a program memory erase operation. When FREE is set, the erase operation is initiated on the next WR command. When FREE is clear, only writes are enabled.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set in hardware when the WR bit is set and cleared when the internal programming timer expires and the write operation is complete.

Note:	During normal operation, the WRERR is								
	read as '1'. This can indicate that a write								
	operation was prematurely terminated by								
	a Reset, or a write operation was								
	attempted improperly.								

The WR control bit initiates write operations. The bit cannot be cleared, only set, in software; it is cleared in hardware at the completion of the write operation.

Note: The EEIF interrupt flag bit (PIR2<4>) is set when the write is complete. It must be cleared in software.

NOTES:

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1		
RBPU	INTEDG0	INTEDG1	INTEDG2	INTEDG3	TMR0IP	INT3IP	RBIP		
bit 7							bit 0		
Legend:									
R = Reada	able bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'			
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	x = Bit is unknown		
bit 7	RBPU: PORT	B Pull-up Enal	ble bit						
	1 = All PORT	B pull-ups are	disabled						
hit C		ouii-ups are ena	abled by Indiv	idual port latch	values				
DILO	1 - Interrupt	on rising edge	l o Euge Sele						
	0 = Interrupt	on falling edge							
bit 5	INTEDG1: Ex	ternal Interrupt	t 1 Edge Sele	ct bit					
	1 = Interrupt	on rising edge	-						
	0 = Interrupt	on falling edge							
bit 4	INTEDG2: Ex	ternal Interrupt	t 2 Edge Sele	ct bit					
	1 = Interrupt	on rising edge							
hit 3		ternal Interrunt	3 Edge Sele	et hit					
bit 5	1 = Interrupt	on rising edge	U Luge Delet						
	0 = Interrupt	on falling edge							
bit 2	TMROIP: TMF	R0 Overflow Int	terrupt Priority	/ bit					
	1 = High prio	rity							
	0 = Low prior	rity							
bit 1	INT3IP: IN13	External Interr	upt Priority bit	I					
	$\perp = Hign prior0 = Low prior$	rity itv							
bit 0	RBIP: RB Po	rt Change Inter	rupt Prioritv b	it					
	1 = High priority								
	0 = Low prior	ity							
Note:	Interrupt flag bits a	are set when a	n interrunt co	ndition occurs	regardless of t	he state of its	corresponding		
1010.	enable bit or the global interrupt enable bit. User software should ensure the appropriate interrupt flag bits								
	are clear prior to e	nabling an inte	rrupt. This fea	ature allows for	software polling	g.			

REGISTER 10-2: INTCON2: INTERRUPT CONTROL REGISTER 2

11.5 PORTE, TRISE and LATE Registers

PORTE is an 8-bit wide, bidirectional port. The corresponding Data Direction register is TRISE. Setting a TRISE bit (= 1) will make the corresponding PORTE pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISE bit (= 0) will make the corresponding PORTE pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATE) is also memory mapped. Read-modify-write operations on the LATE register read and write the latched output value for PORTE.

All pins on PORTE are implemented with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

Note:	On a Power	-on Reset,	these	pins	are
	configured as	digital input	s.		

When the device is operating in Microcontroller mode, pin RE7 can be configured as the alternate peripheral pin for the ECCP2 module. This is done by clearing the CCP2MX Configuration bit.

In 80-pin devices, PORTE is multiplexed with the system bus as part of the external memory interface. I/O port and other functions are only available when the interface is disabled by setting the EBDIS bit (MEMCON<7>). When the interface is enabled (80-pin devices only), PORTE is the high-order byte of the multiplexed address/data bus (AD<15:8>). The TRISE bits are also overridden.

When the Parallel Slave Port is active on PORTD, three of the PORTE pins (RE0/AD8/RD/P2D, RE1/AD9/WR/P2C and RE2/AD10/CS/P2B) are configured as digital control inputs for the port. The control functions are summarized in Table 11-9. The reconfiguration occurs automatically when the PSPMODE control bit (PSPCON<4>) is set. Users must still make certain the corresponding TRISE bits are set to configure these pins as digital inputs.

	LE II-3	
CLRF	PORTE	; Initialize PORTE by
		; clearing output
		; data latches
CLRF	LATE	; Alternate method
		; to clear output
		; data latches
MOVLW	03h	; Value used to
		; initialize data
		; direction
MOVWF	TRISE	; Set RE<1:0> as inputs
		; RE<7:2> as outputs

EXAMPLE 11-5: INITIALIZING PORTE

REGISTER 19-2: SSPxCON1: MSSPx CONTROL REGISTER 1 (SPI MODE)

					•	•			
R/W-0	0 R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
WCO	L SSPOV ⁽¹⁾	SSPEN ⁽²⁾	CKP	SSPM3 ⁽³⁾	SSPM2 ⁽³⁾	SSPM1 ⁽³⁾	SSPM0 ⁽³⁾		
bit 7							bit 0		
Legend:									
R = Read	able bit	W = Writable I	bit	U = Unimpler	nented bit, read	d as '0'			
-n = Value	e at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown		
bit 7	WCOL: Write	Collision Deter	ct bit s written whil	e it is still transr	mitting the prev	ious word			
	(must be 0 = No collisi	 (must be cleared in software) 0 = No collision 							
bit 6	SSPOV: Rec	eive Overflow Ir	ndicator bit ⁽¹⁾						
	SPI Slave mo	ode:							
	1 = A new by overflow, the SSP>	/te is received v the data in SSF (BUF, even if or	while the SSI PxSR is lost. nly transmitti	PxBUF register Overflow can or ng data, to avo	is still holding nly occur in Sla id setting over	the previous da ve mode. The ι flow (must be α	ata. In case of iser must read leared in soft-		
	ware).			0	Ũ	,			
	0 = No overfl	ow							
bit 5	SSPEN: Syne	chronous Serial	Port Enable	bit ⁽²⁾					
	1 = Enables s 0 = Disables	serial port and c serial port and (configures SC configures the	CKx, SDOx, SD ese pins as I/O	Ix and SSx as s port pins	serial port pins			
bit 4	CKP: Clock F	Polarity Select b	it						
	1 = Idle state 0 = Idle state	for clock is a hi for clock is a lo	gh level w level						
bit 3-0	SSPM<3:0>:	Synchronous S	Serial Port Mo	ode Select bits ⁽³	3)				
	0101 = SPI S 0100 = SPI S 0011 = SPI N 0010 = SPI N 0001 = SPI N	Slave mode, clo Slave mode, clo Aaster mode, clo Aaster mode, clo Aaster mode, clo Aaster mode, clo	ck = SCKx pi ck = SCKx pi ock = TMR2 ock = FOSC/6 ock = FOSC/1 ock = FOSC/4	n, <u>SSx</u> pin cont n, SSx pin cont output/2 4 6	trol disabled, Si trol enabled	Sx can be used	as I/O pin		
Note 1:	In Master mode, th writing to the SSP:	ne overflow bit i xBUF register.	s not set sinc	e each new rec	ception (and tra	insmission) is ir	nitiated by		
2:	When enabled, the	ese pins must b	e properly co	onfigured as inp	ut or output.				

3: Bit combinations not specifically listed here are either reserved or implemented in I^2C^{TM} mode only.

19.3.3 ENABLING SPI I/O

To enable the serial port, SSP Enable bit, SSPEN (SSPxCON1<5>), must be set. To reset or reconfigure SPI mode, clear the SSPEN bit, reinitialize the SSPxCON registers and then set the SSPEN bit. This configures the SDIx, SDOx, SCKx and SSx pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed as follows:

- SDIx is automatically controlled by the SPI module
- SDOx must have the TRISC<5> or TRISD<4> bit cleared
- SCKx (Master mode) must have the TRISC<3> or TRISD<6>bit cleared
- SCKx (Slave mode) must have the TRISC<3> or TRISD<6> bit set
- SSx must have the TRISF<7> or TRISD<7> bit set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

19.3.4 TYPICAL CONNECTION

Figure 19-2 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCKx signal. Data is shifted out of both shift registers on their programmed clock edge and latched on the opposite edge of the clock. Both processors should be programmed to the same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data Slave sends dummy data
- Master sends data Slave sends data
- Master sends dummy data Slave sends data

FIGURE 19-2: SPI MASTER/SLAVE CONNECTION



U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
	_		BORV1 ⁽¹⁾	BORV0 ⁽¹⁾	BOREN1 ⁽²⁾	BOREN0 ⁽²⁾	PWRTEN ⁽²⁾
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 7-5	Unimplemen	ted: Read as '	0'				
bit 4-3	BORV<1:0>:	Brown-out Res	set Voltage bits	_S (1)			
	11 = Minimun	n setting					
	•						
	•						
	00 = Maximur	m setting					
bit 2-1	BOREN<1:0>	Brown-out R	eset Enable bi	its ⁽²⁾			
	11 = Brown-	out Reset enat	oled in hardwa	re only (SBOF	REN is disabled))	
	10 = Brown	out Reset enab	oled in hardwa	re only and dis	sabled in Sleep	mode (SBORE	N is disabled)
	01 = Brown	out Reset enab	bled and contro	olled by softwa	are (SBOREN is	enabled)	
hit 0			Enable bit(2)	are and soilwa			
	1 – PWRT die	sabled					
	0 = PWRT en	abled					
	0	"DO OL			· · · ·		
Note 1: See	e Section 28.1	"DC Characte	ristics: Supp	iy voltage" to	r specifications.		

REGISTER 25-2: CONFIG2L: CONFIGURATION REGISTER 2 LOW (BYTE ADDRESS 300002h)

2: The Power-up Timer is decoupled from Brown-out Reset, allowing these features to be independently controlled.

ADD W to f

 $\begin{array}{l} 0 \leq f \leq 255 \\ d \, \in \, [0,1] \end{array}$

 $a \in [0,1]$

ADDWF f {,d {,a}}

26.1.1 STANDARD INSTRUCTION SET

ADDLW	ADD Litera	al to W			ADDWF
Syntax:	ADDLW	k	Syntax:		
Operands:	$0 \le k \le 255$		Operands:		
Operation:	$(W) + k \rightarrow V$	W			
Status Affected:	N, OV, C, D	0C, Z			Operation
Encoding:	0000	1111 k	kkk	kkkk	Operation.
Description:	The conten 8-bit literal W.	ts of W are a 'k' and the re	Encoding: Description:		
Words:	1				
Cycles:	1				
Q Cycle Activity:					
Q1	Q2	Q3		Q4	
Decode	Read literal 'k'	Process Data	V	Vrite to W	
Example: Before Instruct W =	ADDLW] ction 10h	.5h			
W =	25h				
					vvords:
					Cycles:
					Q Cycle Activity:
					Decode
					Example:
					Before Instructi
					W REG
					After Instruction

Operation:	(W) + (f) →	dest								
Status Affected:	N, OV, C, I	N, OV, C, DC, Z								
Encoding:	0010	01da	ffff	ffff						
Description: Add W to register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default).										
	If 'a' is '0', If 'a' is '1', GPR bank	If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).								
	If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 26.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details									
Words:	1									
Cycles:	1									
Q Cycle Activity:										
Q1	Q2	Q3	}	Q4						
Decode	Read register 'f'	Proce Data	ess a c	Write to destination						
Example:	ADDWF	REG,	0, 0							
Before Instruc W REG After Instructio W	tion = 17h = 0C2h on = 0D9h									
REG	= 0C2h									

Note: All PIC18 instructions may take an optional label argument preceding the instruction mnemonic for use in symbolic addressing. If a label is used, the instruction format then becomes: {label} instruction argument(s).

INCFSZ Increment f, Skip if 0								
Syntax:	INCFSZ f	{,d {,a}}						
Operands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$							
Operation:	(f) + 1 \rightarrow de skip if resul	est, t = 0						
Status Affected:	None							
Encoding:	0011	0011 11da ffff ffff						
Description:	The content incrementer placed in W placed back	ts of register 'f d. If 'd' is '0', tł /. If 'd' is '1', th < in register 'f'.	' are ne result is e result is (default)					
	If the result which is alro and a NOP i it a two-cyc	is '0', the next eady fetched is s executed ins le instruction.	t instruction s discarded stead, making					
	If 'a' is '0', ti If 'a' is '1', ti GPR bank (he Access Bar he BSR is use (default).	nk is selected. d to select the					
	If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 26.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed							
Words:	1							
Cycles:	1(2) Note: 3 c by	cycles if skip a a 2-word instr	nd followed uction.					
Q Cycle Activity:								
Q1	Q2	Q3	Q4					
Decode	Read register 'f'	Process Data	destination					
lf skip:								
Q1	Q2	Q3	Q4					
No	No	No	No					
operation	operation	operation	operation					
If skip and followe	a by 2-word in:		04					
No	No	No	No					
operation	operation	operation	operation					
No	No	No	No					
operation	operation	operation	operation					
Example:	HERE NZERO ZERO	INCFSZ CN	T, 1, 0					
Before Instruc PC	tion = Address	(HERE)						
After Instruction CNT If CNT PC If CNT PC	on = CNT + ´ = 0; = Address ≠ 0; = Address	(ZERO) (NZERO)						

INFS	NFSNZ Increment f, Skip if not 0									
Synta	ax:	INFSNZ f	{,d {,a}}							
Oper	ands:	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$	$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$							
Oper	ation:	(f) + 1 \rightarrow dest, skip if result \neq 0								
Statu	is Affected:	None	None							
Enco	oding:	0100	10da ff:	ff ffff						
Desc	ription:	The conten incremente placed in W placed bacl	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default).							
		If the result instruction discarded a instead, ma instruction.	is not '0', the which is alread and a NOP is e aking it a two-c	next dy fetched is xecuted sycle						
		If 'a' is '0', t If 'a' is '1', t GPR bank	he Access Bai he BSR is use (default).	nk is selected. d to select the						
	If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 26.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed									
Word	ls:	1								
Cycle	Cycles: 1(2) Note: 3 cycles if skip and followed by a 2-word instruction.									
QC	ycle Activity:									
	Q1	Q2	Q3	Q4						
	Decode	Read register 'f'	Process Data	Write to destination						
lf sk	ip:									
	Q1	Q2	Q3	Q4						
	N0 operation	N0 operation	N0 operation	N0 operation						
lf sk	ip and followe	d by 2-word in	struction:	operation						
	Q1	Q2	Q3	Q4						
	No	No	No	No						
	operation	operation	operation	operation						
	No	No	No	No						
<u>Exan</u>	nple:	HERE ZERO NZERO	OPERATION	operation						
	Before Instruc PC	tion = Address	6 (HERE)							
	After Instruction	on E = 5								
	REG If REG	= REG + ≠ 0;	1 (NZEDO)							

PC = Address (NZERO) If REG = 0; PC = Address (ZERO)

DC CH	ARACTE	ERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C \leq TA \leq +85°C for industrial					
Param No.	Sym	Characteristic	Min	Тур†	Max Units Conditions			
		Data EEPROM Memory						
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C to +85°C	
D121	Vdrw	VDD for Read/Write	VMIN	_	5.5	V	Using EECON to read/write VMIN = Minimum operating voltage	
D122	TDEW	Erase/Write Cycle Time	—	4	—	ms		
D123	Tretd	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated	
D124	Tref	Number of Total Erase/Write Cycles before Refresh ⁽¹⁾	1M	10M	—	E/W	-40°C to +85°C	
D125	IDDP	Supply Current during Programming	—	10	—	mA		
		Program Flash Memory						
D130	Eр	Cell Endurance	10K	100K	—	E/W	-40°C to +85°C	
D131	Vpr	VDD for Read	Vmin	—	5.5	V	VMIN = Minimum operating voltage	
D132B	Vpew	VDD for Self-Timed Write and Row Erase	Vmin	—	5.5	V	VMIN = Minimum operating voltage	
D133A	Tiw	Self-Timed Write Cycle Time	_	2	_	ms		
D134	Tretd	Characteristic Retention	40	100	_	Year	Provided no other specifications are violated	
D135	IDDP	Supply Current during Programming	—	10	—	mA		

TABLE 28-1:	MEMORY PROGRAMMING REQUIREMENTS
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† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Refer to Section 8.8 "Using the Data EEPROM" for a more detailed discussion on data EEPROM endurance.



FIGURE 28-15: EXAMPLE SPI MASTER MODE TIMING (CKE = 0)

TABLE 28-16: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 0)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \downarrow or SCKx \uparrow Input		Тсү		ns	
71	TscH	SCKx Input High Time	Continuous	1.25 TCY + 30	—	ns	
71A		(Slave mode)	Single Byte	40	_	ns	(Note 1)
72	TscL	SCKx Input Low Time	Continuous	1.25 Tcy + 30		ns	
72A		(Slave mode)	Single Byte	40		ns	(Note 1)
73	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input	20	_	ns		
73A	Тв2в	Last Clock Edge of Byte 1 to th of Byte 2	1.5 Tcy + 40	_	ns	(Note 2)	
74	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge		40		ns	
75	TDOR	SDOx Data Output Rise Time	DOx Data Output Rise Time PIC18FXXXX		25	ns	
			PIC18LFXXXX	—	45	ns	VDD = 2.0V
76	TDOF	SDOx Data Output Fall Time		—	25	ns	
78	TscR	SCKx Output Rise Time	PIC18FXXXX	—	25	ns	
		(Master mode)	PIC18LFXXXX	—	45	ns	VDD = 2.0V
79	TscF	SCKx Output Fall Time (Master mode)			25	ns	
80	TscH2doV,	SDOx Data Output Valid after	PIC18FXXXX	_	50	ns	
	TscL2doV	SCKx Edge	PIC18LFXXXX		100	ns	VDD = 2.0V

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.

Param. No.	Symbol	Characteris	tic	Min	Мах	Units	Conditions
100	Тнідн	Clock High Time	100 kHz mode	4.0	—	μs	PIC18FXXXX must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μS	PIC18FXXXX must operate at a minimum of 10 MHz
			SSP Module	1.5 TCY	—		
101	TLOW	Clock Low Time	100 kHz mode	4.7	—	μS	PIC18FXXXX must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μS	PIC18FXXXX must operate at a minimum of 10 MHz
			SSP Module	1.5 TCY	—		
102	TR	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1 Св	300	ns	CB is specified to be from 10 to 400 pF
103	TF	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1 Св	300	ns	CB is specified to be from 10 to 400 pF
90	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	μs	Only relevant for Repeated
			400 kHz mode	0.6	—	μs	Start condition
91	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	μS	After this period, the first clock
			400 kHz mode	0.6	—	μS	pulse is generated
106	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μS	
107	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	(Note 2)
			400 kHz mode	100	—	ns	
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	μs	_
			400 kHz mode	0.6	—	μS	
109	ΤΑΑ	Output Valid from Clock	100 kHz mode		3500	ns	(Note 1)
			400 kHz mode		—	ns	
110	TBUF	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free
			400 kHz mode	1.3	—	μS	before a new transmission can start
D102	Св	Bus Capacitive Loading		—	400	pF	

TABLE 28-21: I²C[™] BUS DATA REQUIREMENTS (SLAVE MODE)

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCLx to avoid unintended generation of Start or Stop conditions.

2: A Fast mode I²C[™] bus device can be used in a Standard mode I²C bus system, but the requirement, Tsu:DAT ≥ 250 ns, must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLx signal. If such a device does stretch the LOW period of the SCLx signal, it must output the next data bit to the SDAx line, TR max. + Tsu:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCLx line is released.

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