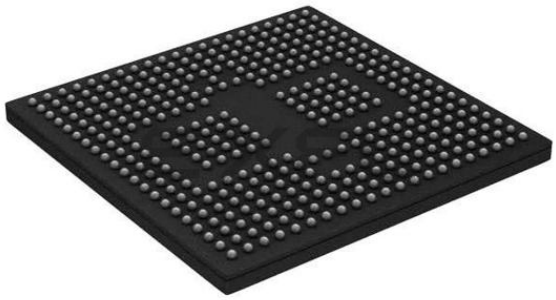

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	XCore
Core Size	32-Bit 24-Core
Speed	4000MIPS
Connectivity	USB
Peripherals	-
Number of I/O	176
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	0.95V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	374-LFBGA
Supplier Device Package	374-FBGA (18x18)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xu224-1024-fb374-c40

1 xCORE Multicore Microcontrollers

The xCORE-200 Series is a comprehensive range of 32-bit multicore microcontrollers that brings the low latency and timing determinism of the xCORE architecture to mainstream embedded applications. Unlike conventional microcontrollers, xCORE multicore microcontrollers execute multiple real-time tasks simultaneously and communicate between tasks using a high speed network. Because xCORE multicore microcontrollers are completely deterministic, you can write software to implement functions that traditionally require dedicated hardware.

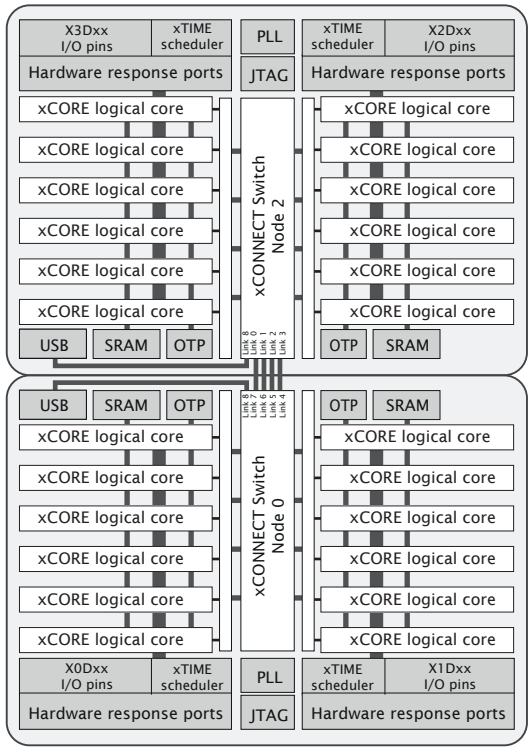

Figure 1: XU224-1024-FB374 block diagram

Key features of the XU224-1024-FB374 include:

- **Tiles**: Devices consist of one or more xCORE tiles. Each tile contains between five and eight 32-bit xCOREs with highly integrated I/O and on-chip memory.
- **Logical cores** Each logical core can execute tasks such as computational code, DSP code, control software (including logic decisions and executing a state machine) or software that handles I/O. Section 6.1
- **xTIME scheduler** The xTIME scheduler performs functions similar to an RTOS, in hardware. It services and synchronizes events in a core, so there is no requirement for interrupt handler routines. The xTIME scheduler triggers cores

Signal	Function					Type	Properties
X1D17	$X_0L3^0_{in}$		4D[1]	8B[3]	16A[11]	I/O	IO, PD
X1D18	$X_0L3^0_{out}$		4D[2]	8B[4]	16A[12]	I/O	IO, PD
X1D19	$X_0L3^1_{out}$		4D[3]	8B[5]	16A[13]	I/O	IO, PD
X1D20			4C[2]	8B[6]	16A[14]	32A[30]	I/O	IO, PD
X1D21			4C[3]	8B[7]	16A[15]	32A[31]	I/O	IO, PD
X1D22	$X_0L3^4_{out}$	1G[0]					I/O	IO, PD
X1D23		1H[0]					I/O	IO, PD
X1D24		1I[0]					I/O	IO, PD
X1D25		1J[0]					I/O	IO, PD
X1D26			4E[0]	8C[0]	16B[0]		I/O	IOT, PD
X1D27			4E[1]	8C[1]	16B[1]		I/O	IOT, PD
X1D28			4F[0]	8C[2]	16B[2]		I/O	IOT, PD
X1D29			4F[1]	8C[3]	16B[3]		I/O	IOT, PD
X1D30			4F[2]	8C[4]	16B[4]		I/O	IOT, PD
X1D31			4F[3]	8C[5]	16B[5]		I/O	IOT, PD
X1D32			4E[2]	8C[6]	16B[6]		I/O	IOT, PD
X1D33			4E[3]	8C[7]	16B[7]		I/O	IOT, PD
X1D34	$X_0L0^2_{out}$	1K[0]					I/O	IO, PD
X1D35	$X_0L0^3_{out}$	1L[0]					I/O	IO, PD
X1D36	$X_0L0^4_{out}$	1M[0]		8D[0]	16B[8]		I/O	IO, PD
X1D37	$X_0L3^4_{in}$	1N[0]		8D[1]	16B[9]		I/O	IO, PD
X1D38	$X_0L3^3_{in}$	1O[0]		8D[2]	16B[10]		I/O	IO, PD
X1D39	$X_0L3^2_{in}$	1P[0]		8D[3]	16B[11]		I/O	IO, PD
X1D40				8D[4]	16B[12]		I/O	IOT, PD
X1D41				8D[5]	16B[13]		I/O	IOT, PD
X1D42				8D[6]	16B[14]		I/O	IOT, PD
X1D43				8D[7]	16B[15]		I/O	IOT, PD
X1D49	$X_0L1^4_{in}$					32A[0]	I/O	IO, PD
X1D50	$X_0L1^3_{in}$					32A[1]	I/O	IO, PD
X1D51	$X_0L1^2_{in}$					32A[2]	I/O	IO, PD
X1D52	$X_0L1^1_{in}$					32A[3]	I/O	IO, PD
X1D53	$X_0L1^0_{in}$					32A[4]	I/O	IO, PD
X1D54	$X_0L1^0_{out}$					32A[5]	I/O	IO, PD
X1D55	$X_0L1^1_{out}$					32A[6]	I/O	IO, PD
X1D56	$X_0L1^2_{out}$					32A[7]	I/O	IO, PD
X1D57	$X_0L1^3_{out}$					32A[8]	I/O	IO, PD
X1D58	$X_0L1^4_{out}$					32A[9]	I/O	IO, PD
X1D61	$X_0L2^4_{in}$					32A[10]	I/O	IO, PD
X1D62	$X_0L2^3_{in}$					32A[11]	I/O	IO, PD
X1D63	$X_0L2^2_{in}$					32A[12]	I/O	IO, PD
X1D64	$X_0L2^1_{in}$					32A[13]	I/O	IO, PD
X1D65	$X_0L2^0_{in}$					32A[14]	I/O	IO, PD
X1D66	$X_0L2^0_{out}$					32A[15]	I/O	IO, PD

(continued)

Signal	Function					Type	Properties
X2D53	$X_2L5^0_{in}$				$32A^4$	I/O	IO, PD
X2D54	$X_2L5^0_{out}$				$32A^5$	I/O	IO, PD
X2D55	$X_2L5^1_{out}$				$32A^6$	I/O	IO, PD
X2D56	$X_2L5^2_{out}$				$32A^7$	I/O	IO, PD
X2D57	$X_2L5^3_{out}$				$32A^8$	I/O	IO, PD
X2D58	$X_2L5^4_{out}$				$32A^9$	I/O	IO, PD
X2D61	$X_2L6^4_{in}$				$32A^{10}$	I/O	IO, PD
X2D62	$X_2L6^3_{in}$				$32A^{11}$	I/O	IO, PD
X2D63	$X_2L6^2_{in}$				$32A^{12}$	I/O	IO, PD
X2D64	$X_2L6^1_{in}$				$32A^{13}$	I/O	IO, PD
X2D65	$X_2L6^0_{in}$				$32A^{14}$	I/O	IO, PD
X2D66	$X_2L6^0_{out}$				$32A^{15}$	I/O	IO, PD
X2D67	$X_2L6^1_{out}$				$32A^{16}$	I/O	IO, PD
X2D68	$X_2L6^2_{out}$				$32A^{17}$	I/O	IO, PD
X2D69	$X_2L6^3_{out}$				$32A^{18}$	I/O	IO, PD
X2D70	$X_2L6^4_{out}$				$32A^{19}$	I/O	IO, PD
X3D00	$X_2L7^2_{in}$	$1A^0$				I/O	IO, PD
X3D01	$X_2L7^1_{in}$	$1B^0$				I/O	IO, PD
X3D02	$X_2L4^0_{in}$		$4A^0$	$8A^0$	$16A^0$ $32A^{20}$	I/O	IO, PD
X3D03	$X_2L4^0_{out}$		$4A^1$	$8A^1$	$16A^1$ $32A^{21}$	I/O	IO, PD
X3D04	$X_2L4^1_{out}$		$4B^0$	$8A^2$	$16A^2$ $32A^{22}$	I/O	IO, PD
X3D05	$X_2L4^2_{out}$		$4B^1$	$8A^3$	$16A^3$ $32A^{23}$	I/O	IO, PD
X3D06	$X_2L4^3_{out}$		$4B^2$	$8A^4$	$16A^4$ $32A^{24}$	I/O	IO, PD
X3D07	$X_2L4^4_{out}$		$4B^3$	$8A^5$	$16A^5$ $32A^{25}$	I/O	IO, PD
X3D08	$X_2L7^4_{in}$		$4A^2$	$8A^6$	$16A^6$ $32A^{26}$	I/O	IO, PD
X3D09	$X_2L7^3_{in}$		$4A^3$	$8A^7$	$16A^7$ $32A^{27}$	I/O	IO, PD
X3D10		$1C^0$				I/O	IOT, PD
X3D11		$1D^0$				I/O	IOT, PD
X3D12		$1E^0$				I/O	IO, PD
X3D13		$1F^0$				I/O	IO, PD
X3D14			$4C^0$	$8B^0$	$16A^8$ $32A^{28}$	I/O	IO, PD
X3D15			$4C^1$	$8B^1$	$16A^9$ $32A^{29}$	I/O	IO, PD
X3D20			$4C^2$	$8B^6$	$16A^{14}$ $32A^{30}$	I/O	IO, PD
X3D21			$4C^3$	$8B^7$	$16A^{15}$ $32A^{31}$	I/O	IO, PD
X3D23		$1H^0$				I/O	IO, PD
X3D24		$1I^0$				I/O	IO, PD
X3D25		$1J^0$				I/O	IO, PD
X3D26			$4E^0$	$8C^0$	$16B^0$	I/O	IOT, PD
X3D27			$4E^1$	$8C^1$	$16B^1$	I/O	IOT, PD
X3D28			$4F^0$	$8C^2$	$16B^2$	I/O	IOT, PD
X3D29			$4F^1$	$8C^3$	$16B^3$	I/O	IOT, PD
X3D30			$4F^2$	$8C^4$	$16B^4$	I/O	IOT, PD
X3D31			$4F^3$	$8C^5$	$16B^5$	I/O	IOT, PD

(continued)

ports are available. All pins of a port provide either output or input. Signals in different directions cannot be mapped onto the same port.

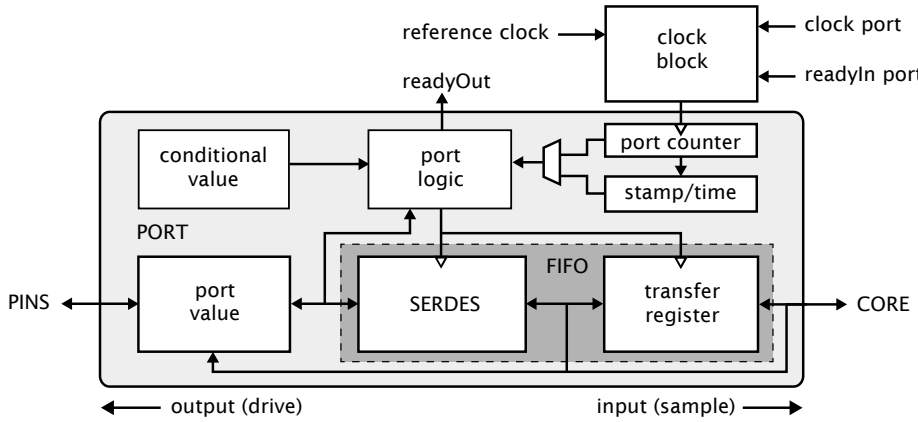

Figure 4: Port block diagram

The port logic can drive its pins high or low, or it can sample the value on its pins, optionally waiting for a particular condition. Ports are accessed using dedicated instructions that are executed in a single processor cycle. xCORE-200 IO pins can be used as *open collector* outputs, where signals are driven low if a zero is output, but left high impedance if a one is output. This option is set on a per-port basis.

Data is transferred between the pins and core using a FIFO that comprises a SERDES and transfer register, providing options for serialization and buffered data.

Each port has a 16-bit counter that can be used to control the time at which data is transferred between the port value and transfer register. The counter values can be obtained at any time to find out when data was obtained, or used to delay I/O until some time in the future. The port counter value is automatically saved as a timestamp, that can be used to provide precise control of response times.

The ports and xCONNECT links are multiplexed onto the physical pins. If an xConnect Link is enabled, the pins of the underlying ports are disabled. If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled. Ports always operate at their specified width, even if they share pins with another port.

6.4 Clock blocks

xCORE devices include a set of programmable clocks called clock blocks that can be used to govern the rate at which ports execute. Each xCORE tile has six clock blocks: the first clock block provides the tile reference clock and runs at a default frequency of 100MHz; the remaining clock blocks can be set to run at different frequencies.

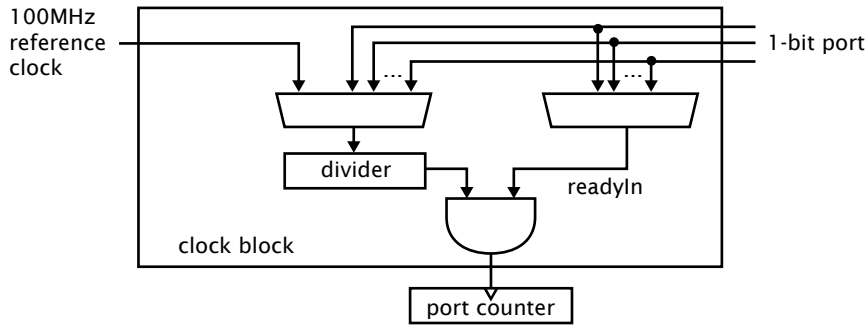

Figure 5: Clock block diagram

A clock block can use a 1-bit port as its clock source allowing external application clocks to be used to drive the input and output interfaces. xCORE-200 clock blocks optionally divide the clock input from a 1-bit port.

In many cases I/O signals are accompanied by strobing signals. The xCORE ports can input and interpret strobe (known as readyIn and readyOut) signals generated by external sources, and ports can generate strobe signals to accompany output data.

On reset, each port is connected to clock block 0, which runs from the xCORE Tile reference clock.

6.5 Channels and Channel Ends

Logical cores communicate using point-to-point connections, formed between two channel ends. A channel-end is a resource on an xCORE tile, that is allocated by the program. Each channel-end has a unique system-wide identifier that comprises a unique number and their tile identifier. Data is transmitted to a channel-end by an output-instruction; and the other side executes an input-instruction. Data can be passed synchronously or asynchronously between the channel ends.

6.6 xCONNECT Switch and Links

XMOS devices provide a scalable architecture, where multiple xCORE devices can be connected together to form one system. Each xCORE device has an xCONNECT interconnect that provides a communication infrastructure for all tasks that run on the various xCORE tiles on the system.

The interconnect relies on a collection of switches and XMOS links. Each xCORE device has an on-chip switch that can set up circuits or route data. The switches are connected by xConnect Links. An XMOS link provides a physical connection between two switches. The switch has a routing algorithm that supports many different topologies, including lines, meshes, trees, and hypercubes.

The links operate in either 2 wires per direction or 5 wires per direction mode, depending on the amount of bandwidth required. Circuit switched, streaming

The pins used for QSPI boot are hardcoded in the boot ROM and cannot be changed. If required, an QSPI boot program can be burned into OTP that uses different pins.

8.2 Boot from SPI master

If set to boot from SPI master, the processor enables the four pins specified in Figure 11, and drives the SPI clock at 2.5 MHz (assuming a 400 MHz core clock). A READ command is issued with a 24-bit address 0x000000. The clock polarity and phase are 0 / 0.

Figure 11: SPI master pins

Pin	Signal	Description
X0D00	MISO	Master In Slave Out (Data)
X0D01	SS	Slave Select
X0D10	SCLK	Clock
X0D11	MOSI	Master Out Slave In (Data)

The xCORE Tile expects each byte to be transferred with the *least-significant bit first*. Programmers who write bytes into an SPI interface using the most significant bit first may have to reverse the bits in each byte of the image stored in the SPI device.

If a large boot image is to be read in, it is faster to first load a small boot-loader that reads the large image using a faster SPI clock, for example 50 MHz or as fast as the flash device supports.

The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. If required, an SPI boot program can be burned into OTP that uses different pins.

8.3 Boot from SPI slave

If set to boot from SPI slave, the processor enables the three pins specified in Figure 12 and expects a boot image to be clocked in. The supported clock polarity and phase are 0/0 and 1/1.

Figure 12: SPI slave pins

Pin	Signal	Description
X0D00	SS	Slave Select
X0D10	SCLK	Clock
X0D11	MOSI	Master Out Slave In (Data)

The xCORE Tile expects each byte to be transferred with the *least-significant bit first*. The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. If required, an SPI boot program can be burned into OTP that uses different pins.

8.4 Boot from xConnect Link

If set to boot from an xConnect Link, the processor enables its link(s) around 2 us after the boot process starts. Enabling the Link switches off the pull-down

resistors on the link, drives all the TX wires low (the initial state for the Link), and monitors the RX pins for boot-traffic; they must be low at this stage. If the internal pull-down is too weak to drain any residual charge, external pull-downs of 10K may be required on those pins.

The boot-rom on the core will then:

1. Allocate channel-end 0.
2. Input a word on channel-end 0. It will use this word as a channel to acknowledge the boot. Provide the null-channel-end 0x0000FF02 if no acknowledgment is required.
3. Input the boot image specified above, including the CRC.
4. Input an END control token.
5. Output an END control token to the channel-end received in step 2.
6. Free channel-end 0.
7. Jump to the loaded code.

8.5 Boot from OTP

If an xCORE tile is set to use secure boot (see Figure 8), the boot image is read from address 0 of the OTP memory in the tile's security module.

This feature can be used to implement a secure bootloader which loads an encrypted image from external flash, decrypts and CRC checks it with the processor, and discontinues the boot process if the decryption or CRC check fails. XMOS provides a default secure bootloader that can be written to the OTP along with secret decryption keys.

Each tile has its own individual OTP memory, and hence some tiles can be booted from OTP while others are booted from SPI or the channel interface. This enables systems to be partially programmed, dedicating one or more tiles to perform a particular function, leaving the other tiles user-programmable.

8.6 Security register

The security register enables security features on the xCORE tile. The features shown in Figure 13 provide a strong level of protection and are sufficient for providing strong IP security.

9 Memory

9.1 OTP

Each xCORE Tile integrates 8 KB one-time programmable (OTP) memory along with a security register that configures system wide security features. The OTP holds

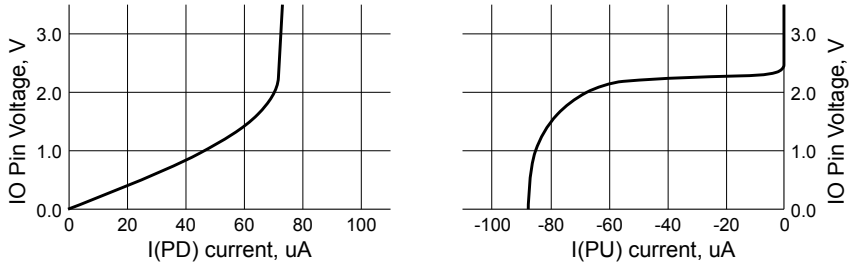

Figure 22: Typical internal pull-down and pull-up currents

13.3 ESD Stress Voltage

Figure 23: ESD stress voltage

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
HBM	Human body model	-2.00		2.00	KV	
CDM	Charged Device Model	-500		500	V	

13.4 Reset Timing

Figure 24: Reset timing

Symbol	Parameters	MIN	TYP	MAX	UNITS	Notes
T(RST)	Reset pulse width	5			µs	
T(INIT)	Initialization time			150	µs	A

A Shows the time taken to start booting after RST_N has gone high.

13.5 Power Consumption

Figure 25: xCORE Tile currents

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
I(DDCQ)	Quiescent VDD current		90		mA	A, B, C
PD	Tile power dissipation		325		µW/MIPS	A, D, E, F
IDD	Active VDD current		1140	1400	mA	A, G
I(ADDPLL)	PLL_AVDD current		5	7	mA	H
I(VDD33)	VDD33 current		53.4		mA	I
I(USB_VDD)	USB_VDD current		16.6		mA	J

A Use for budgetary purposes only.

B Assumes typical tile and I/O voltages with no switching activity.

C Includes PLL current.

D Assumes typical tile and I/O voltages with nominal switching activity.

E Assumes 1 MHz = 1 MIPS.

F PD(TYP) value is the usage power consumption under typical operating conditions.

G Measurement conditions: VDD = 1.0 V, VDDIO = 3.3 V, 25 °C, 500 MHz, average device resource usage.

H PLL_AVDD = 1.0 V

I HS mode transmitting while driving all 0's data (constant JKJK on DP/DM). Loading of 10 pF. Transfers do not include any interpacket delay.

J HS receive mode; no traffic.

The tile power consumption of the device is highly application dependent and should be used for budgetary purposes only.

More detailed power analysis can be found in the XS1-U Power Consumption document,

13.6 Clock

Figure 26: Clock

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f	Frequency	3.25	24	100	MHz	
SR	Slew rate	0.10			V/ns	
TJ(LT)	Long term jitter (pk-pk)			2	%	A
f(MAX)	Processor clock frequency			500	MHz	B

A Percentage of CLK period.

B Assumes typical tile and I/O voltages with nominal activity.

Further details can be found in the XS1-U Clock Frequency Control document,

14.1 Part Marking

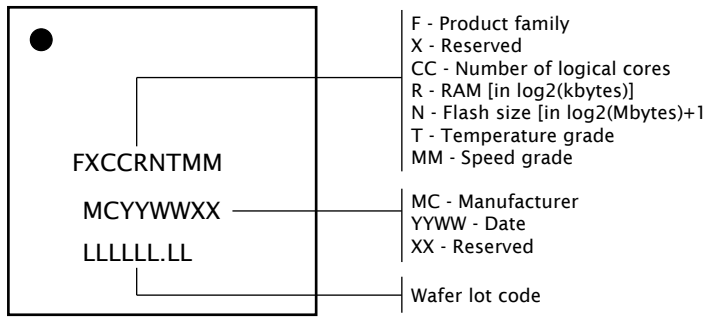

Figure 30: Part marking scheme

15 Ordering Information

Figure 31: Orderable part numbers

Product Code	Marking	Qualification	Speed Grade
XU224-1024-FB374-C40	U124A0C40	Commercial	2000 MIPS
XU224-1024-FB374-I40	U124A0I40	Industrial	2000 MIPS

Appendices

A Configuration of the XU224-1024-FB374

The device is configured through banks of registers, as shown in Figure 32.

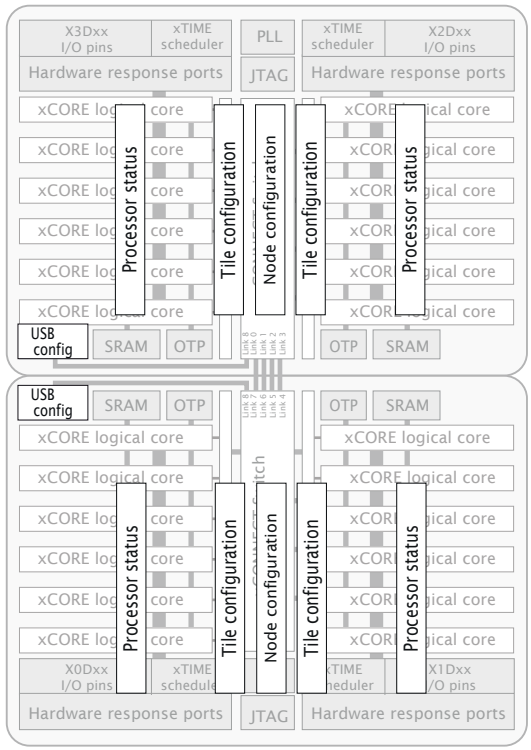

Figure 32: Registers

The following communication sequences specify how to access those registers. Any messages transmitted contain the most significant 24 bits of the channel-end to which a response is to be sent. This comprises the node-identifier and the channel number within the node. if no response is required on a write operation, supply 24-bits with the last 8-bits set, which suppresses the reply message. Any multi-byte data is sent most significant byte first.

A.1 Accessing a processor status register

The processor status registers are accessed directly from the processor instruction set. The instructions GETPS and SETPS read and write a word. The register number should be translated into a processor-status resource identifier by shifting the register number left 8 places, and ORing it with 0x0B. Alternatively, the functions `getps(reg)` and `setps(reg,value)` can be used from XC.

Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:18	RW	0	RGMII TX data delay value (in PLL output cycle increments)
17:9	RW	0	RGMII TX clock divider value. TX clk rises when counter (clocked by PLL output) reaches this value and falls when counter reaches (value»1). Value programmed into this field should be actual divide value required minus 1
8	RW	0	Enable RGMII interface periph ports
7:6	RO	-	Reserved
5	RW	0	Select the dynamic mode (1) for the clock divider when the clock divider is enabled. In dynamic mode the clock divider is only activated when all active threads are paused. In static mode the clock divider is always enabled.
4	RW	0	Enable the clock divider. This divides the output of the PLL to facilitate one of the low power modes.
3	RO	-	Reserved
2	RW		Select between UTMI (1) and ULPI (0) mode.
1	RW		Enable the ULPI Hardware support module
0	RO	-	Reserved

0x02: xCORE Tile control

B.4 xCORE Tile boot status: 0x03

This read-only register describes the boot status of the xCORE tile.

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	RO		Processor number.
15:9	RO	-	Reserved
8	RO		Overwrite BOOT_MODE.
7:6	RO	-	Reserved
5	RO		Indicates if core1 has been powered off
4	RO		Cause the ROM to not poll the OTP for correct read levels
3	RO		Boot ROM boots from RAM
2	RO		Boot ROM boots from JTAG
1:0	RO		The boot PLL mode pin value.

0x03: xCORE Tile boot status

0x9C .. 0x9F: Resources breakpoint control register

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	DRW	0	A bit for each thread in the machine allowing the breakpoint to be enabled individually for each thread.
15:2	RO	-	Reserved
1	DRW	0	When 0 break when condition A is met. When 1 = break when condition B is met.
0	DRW	0	When 1 the instruction breakpoint is enabled.

C Tile Configuration

The xCORE Tile control registers can be accessed using configuration reads and writes (use `write_tile_config_reg(tileref, ...)` and `read_tile_config_reg(tileref, ...)` for reads and writes).

Number	Perm	Description
0x00	CRO	Device identification
0x01	CRO	xCORE Tile description 1
0x02	CRO	xCORE Tile description 2
0x04	CRW	Control PSwitch permissions to debug registers
0x05	CRW	Cause debug interrupts
0x06	CRW	xCORE Tile clock divider
0x07	CRO	Security configuration
0x20 .. 0x27	CRW	Debug scratch
0x40	CRO	PC of logical core 0
0x41	CRO	PC of logical core 1
0x42	CRO	PC of logical core 2
0x43	CRO	PC of logical core 3
0x44	CRO	PC of logical core 4
0x45	CRO	PC of logical core 5
0x46	CRO	PC of logical core 6
0x47	CRO	PC of logical core 7
0x60	CRO	SR of logical core 0
0x61	CRO	SR of logical core 1
0x62	CRO	SR of logical core 2
0x63	CRO	SR of logical core 3
0x64	CRO	SR of logical core 4
0x65	CRO	SR of logical core 5
0x66	CRO	SR of logical core 6
0x67	CRO	SR of logical core 7

Figure 34: Summary

C.1 Device identification: 0x00

This register identifies the xCORE Tile

0x07: Security configuration

Bits	Perm	Init	Description
31	CRO		Disables write permission on this register
30:15	RO	-	Reserved
14	CRO		Disable access to XCore's global debug
13	RO	-	Reserved
12	CRO		lock all OTP sectors
11:8	CRO		lock bit for each OTP sector
7	CRO		Enable OTP reduanacy
6	RO	-	Reserved
5	CRO		Override boot mode and read boot image from OTP
4	CRO		Disable JTAG access to the PLL/BOOT configuration registers
3:1	RO	-	Reserved
0	CRO		Disable access to XCore's JTAG debug TAP

C.8 Debug scratch: 0x20 .. 0x27

A set of registers used by the debug ROM to communicate with an external debugger, for example over the switch. This is the same set of registers as the Debug Scratch registers in the processor status.

0x20 .. 0x27: Debug scratch

Bits	Perm	Init	Description
31:0	CRW		Value.

C.9 PC of logical core 0: 0x40

Value of the PC of logical core 0.

0x40: PC of logical core 0

Bits	Perm	Init	Description
31:0	CRO		Value.

C.10 PC of logical core 1: 0x41

Value of the PC of logical core 1.

0x41: PC of logical core 1

Bits	Perm	Init	Description
31:0	CRO		Value.

C.11 PC of logical core 2: 0x42

Value of the PC of logical core 2.

0x42: PC of logical core 2

Bits	Perm	Init	Description
31:0	CRO		Value.

C.12 PC of logical core 3: 0x43

Value of the PC of logical core 3.

0x43: PC of logical core 3

Bits	Perm	Init	Description
31:0	CRO		Value.

C.13 PC of logical core 4: 0x44

Value of the PC of logical core 4.

0x44: PC of logical core 4

Bits	Perm	Init	Description
31:0	CRO		Value.

C.14 PC of logical core 5: 0x45

Value of the PC of logical core 5.

0x45: PC of logical core 5

Bits	Perm	Init	Description
31:0	CRO		Value.

D Node Configuration

The digital node control registers can be accessed using configuration reads and writes (use `write_node_config_reg(device, ...)` and `read_node_config_reg(device, ...)` for reads and writes).

Number	Perm	Description
0x00	RO	Device identification
0x01	RO	System switch description
0x04	RW	Switch configuration
0x05	RW	Switch node identifier
0x06	RW	PLL settings
0x07	RW	System switch clock divider
0x08	RW	Reference clock
0x09	R	System JTAG device ID register
0x0A	R	System USERCODE register
0x0C	RW	Directions 0-7
0x0D	RW	Directions 8-15
0x10	RW	DEBUG_N configuration, tile 0
0x11	RW	DEBUG_N configuration, tile 1
0x1F	RO	Debug source
0x20 .. 0x28	RW	Link status, direction, and network
0x40 .. 0x47	RO	PLink status and network
0x80 .. 0x88	RW	Link configuration and initialization
0xA0 .. 0xA7	RW	Static link configuration

Figure 35: Summary

D.1 Device identification: 0x00

This register contains version and revision identifiers and the mode-pins as sampled at boot-time.

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	RO		Sampled values of BootCtl pins on Power On Reset.
15:8	RO		SSwitch revision.
7:0	RO		SSwitch version.

0x00: Device identification

0x0D: Directions 8-15

Bits	Perm	Init	Description
31:28	RW	0	The direction for packets whose dimension is F.
27:24	RW	0	The direction for packets whose dimension is E.
23:20	RW	0	The direction for packets whose dimension is D.
19:16	RW	0	The direction for packets whose dimension is C.
15:12	RW	0	The direction for packets whose dimension is B.
11:8	RW	0	The direction for packets whose dimension is A.
7:4	RW	0	The direction for packets whose dimension is 9.
3:0	RW	0	The direction for packets whose dimension is 8.

D.12 DEBUG_N configuration, tile 0: 0x10

Configures the behavior of the DEBUG_N pin.

0x10: DEBUG_N configuration, tile 0

Bits	Perm	Init	Description
31:2	RO	-	Reserved
1	RW	0	Set 1 to enable GlobalDebug to generate debug request to XCore.
0	RW	0	Set 1 to enable inDebug bit to drive GlobalDebug.

D.13 DEBUG_N configuration, tile 1: 0x11

Configures the behavior of the DEBUG_N pin.

0x11: DEBUG_N configuration, tile 1

Bits	Perm	Init	Description
31:2	RO	-	Reserved
1	RW	0	Set 1 to enable GlobalDebug to generate debug request to XCore.
0	RW	0	Set 1 to enable inDebug bit to drive GlobalDebug.

D.14 Debug source: 0x1F

Contains the source of the most recent debug event.

0x04: UIFM IFM control

Bits	Perm	Init	Description
31:8	RO	-	Reserved
7	RW	0	Set to 1 to enable XEVACKMODE mode.
6	RW	0	Set to 1 to enable SOFISTOKEN mode.
5	RW	0	Set to 1 to enable UIFM power signalling mode.
4	RW	0	Set to 1 to enable IF timing mode.
3	RO	-	Reserved
2	RW	0	Set to 1 to enable UIFM linestate decoder.
1	RW	0	Set to 1 to enable UIFM CHECKTOKENS mode.
0	RW	0	Set to 1 to enable UIFM DOTOKENS mode.

F.3 UIFM Device Address: 0x08

The device address whose packets should be received. 0 until enumeration, it should be set to the assigned value after enumeration.

0x08: UIFM Device Address

Bits	Perm	Init	Description
31:7	RO	-	Reserved
6:0	RW	0	The enumerated USB device address must be stored here. Only packets to this address are passed on.

F.4 UIFM functional control: 0x0C

0x0C: UIFM functional control

Bits	Perm	Init	Description
31:5	RO	-	Reserved
4:2	RW	1	Set to 0 to disable UIFM to UTMI+ OPMODE mode.
1	RW	1	Set to 1 to switch UIFM to UTMI+ TERMSELECT mode.
0	RW	1	Set to 1 to switch UIFM to UTMI+ XCVRSELECT mode.

F.5 UIFM on-the-go control: 0x10

This register is used to negotiate an on-the-go connection.

0x10: UIFM on-the-go control

Bits	Perm	Init	Description
31:8	RO	-	Reserved
7	RW	0	Set to 1 to switch UIFM to EXTVBUSIND mode.
6	RW	0	Set to 1 to switch UIFM to DRVVBUSEXT mode.
5	RO	-	Reserved
4	RW	0	Set to 1 to switch UIFM to UTMI+ CHRGVBUS mode.
3	RW	0	Set to 1 to switch UIFM to UTMI+ DISCHRGVBUS mode.
2	RW	0	Set to 1 to switch UIFM to UTMI+ DMPULLDOWN mode.
1	RW	0	Set to 1 to switch UIFM to UTMI+ DPPULLDOWN mode.
0	RW	0	Set to 1 to switch UIFM to IDPULLUP mode.

F.6 UIFM on-the-go flags: 0x14

Status flags used for on-the-go negotiation

0x14: UIFM on-the-go flags

Bits	Perm	Init	Description
31:6	RO	-	Reserved
5	RO	0	Value of UTMI+ Bvalid flag.
4	RO	0	Value of UTMI+ IDGND flag.
3	RO	0	Value of UTMI+ HOSTDIS flag.
2	RO	0	Value of UTMI+ VBUSVLD flag.
1	RO	0	Value of UTMI+ SESSVLD flag.
0	RO	0	Value of UTMI+ SESSEND flag.