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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I <sup>2</sup> C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	24
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 23x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f930-g-gqr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 1.4. C8051F921 Block Diagram





Figure 3.4. QFN-32 Package Marking Diagram





Figure 3.10. Typical QFN-24 Landing Diagram





Figure 4.1. Active Mode Current (External CMOS Clock)



#### 5.2.3. Burst Mode

Burst Mode is a power saving feature that allows ADC0 to remain in a low power state between conversions. When Burst Mode is enabled, ADC0 wakes from a low power state, accumulates 1, 4, 8, 16, 32, or 64 using an internal burst mode clock (approximately 25 MHz), then re-enters a low power state. Since the burst mode clock is independent of the system clock, ADC0 can perform multiple conversions then enter a low power state within a single system clock cycle, even if the system clock is slow (e.g., 32.768 kHz), or suspended.

Burst Mode is enabled by setting BURSTEN to logic 1. When in burst mode, AD0EN controls the ADC0 idle power state (i.e. the state ADC0 enters when not tracking or performing conversions). If AD0EN is set to logic 0, ADC0 is powered down after each burst. If AD0EN is set to logic 1, ADC0 remains enabled after each burst. On each convert start signal, ADC0 is awakened from its Idle Power State. If ADC0 is powered down, it will automatically power up and wait the programmable Power-Up Time controlled by the AD0PWR bits. Otherwise, ADC0 will start tracking and converting immediately. Figure 5.3 shows an example of Burst Mode Operation with a slow system clock and a repeat count of 4.

When burst mode is enabled, a single convert start will initiate a number of conversions equal to the repeat count. When burst mode is disabled, a convert start is required to initiate each conversion. In both modes, the ADC0 End of Conversion Interrupt Flag (AD0INT) will be set after "repeat count" conversions have been accumulated. Similarly, the Window Comparator will not compare the result to the greater-than and less-than registers until "repeat count" conversions have been accumulated.

In Burst Mode, tracking is determined by the settings in AD0PWR and AD0TK. The default settings for these registers will work in most applications without modification; however, settling time requirements may need adjustment in some applications. Refer to "5.2.4. Settling Time Requirements" on page 73 for more details.

Notes:

- Setting AD0TM to 1 will insert an additional 3 SAR clocks of tracking before each conversion, regardless of the settings of AD0PWR and AD0TK.
- When using Burst Mode, care must be taken to issue a convert start signal no faster than once every four SYSCLK periods. This includes external convert start signals.
- A rising edge of external start-of-conversion (CNVSTR) will cause only one ADC conversion in Burst Mode, regardless of the value of the Repeat Count field. The end-of-conversion interrupt will occur after the number of conversions specified in Repeat Count have completed. In other words, if Repeat Count is set to 4, four pulses on CNVSTR will cause an ADC end-of-conversion interrupt. Refer to the bottom portion of Figure 5.3, "Burst Mode Tracking Example with Repeat Count Set to 4," on page 72 for an example.
- To start multiple conversions in Burst Mode with one external start-of-conversion signal, the external interrupts (/INT0 or /INT1) or Port Match can be used to trigger an ISR that writes to AD0BUSY. External interrupts are configurable to be active low or active high, edge or level sensitive, but is only available on a limited number of pins. Port Match is only level sensitive, but is available on more port pins than the external interrupts. Refer to Section "12.6. External Interrupts INT0 and INT1" on page 146 for details on external interrupts and Section "21.4. Port Match" on page 227 for details on Port Match.



## 6. Programmable Current Reference (IREF0)

C8051F93x-C8051F92x devices include an on-chip programmable current reference (source or sink) with two output current settings: Low Power Mode and High Current Mode. The maximum current output in Low Power Mode is 63  $\mu$ A (1  $\mu$ A steps) and the maximum current output in High Current Mode is 504  $\mu$ A (8  $\mu$ A steps).

The current source/sink is controlled though the IREF0CN special function register. It is enabled by setting the desired output current to a non-zero value. It is disabled by writing 0x00 to IREF0CN. The port I/O pin associated with ISRC0 should be configured as an analog input and skipped in the Crossbar. See Section "21. Port Input/Output" on page 216 for more details.

#### SFR Definition 6.1. IREF0CN: Current Reference Control

Bit	7	6	5	4	3	2	1	0
Name	SINK	MODE	IREF0DAT					
Туре	R/W	R/W	R/W					
Reset	0	0	0	0	0	0	0	0

#### SFR Page = 0x0; SFR Address = 0xB9

Bit	Name	Function
7	SINK	IREF0 Current Sink Enable.
		Selects if IREF0 is a current source or a current sink. 0: IREF0 is a current source. 1: IREF0 is a current sink.
6	MDSEL	IREF0 Output Mode Select.
		Selects Low Power or High Current Mode.
		0: Low Power Mode is selected (step size = 1 $\mu$ A).
		1: High Current Mode is selected (step size = 8 μA).
5:0	IREF0DAT[5:0]	IREF0 Data Word.
		Specifies the number of steps required to achieve the desired output current. Output current = direction x step size x IREF0DAT. IREF0 is in a low power state when IREF0DAT is set to 0x00.

#### 6.1. IREF0 Specifications

See Table 4.12 on page 63 for a detailed listing of IREF0 specifications.



### 7. Comparators

C8051F93x-C8051F92x devices include two on-chip programmable voltage comparators: Comparator 0 (CPT0) is shown in Figure 7.1; Comparator 1 (CPT1) is shown in Figure 7.2. The two comparators operate identically, but may differ in their ability to be used as reset or wake-up sources. See the Reset Sources chapter and the Power Management chapter for details on reset sources and low power mode wake-up sources, respectively.

The Comparator offers programmable response time and hysteresis, an analog input multiplexer, and two outputs that are optionally available at the Port pins: a synchronous "latched" output (CP0, CP1), or an asynchronous "raw" output (CP0A, CP1A). The asynchronous CP0A signal is available even when the system clock is not active. This allows the Comparator to operate and generate an output when the device is in some low power modes.

#### 7.1. Comparator Inputs

Each Comparator performs an analog comparison of the voltage levels at its positive (CP0+ or CP1+) and negative (CP0- or CP1-) input. Both comparators support multiple port pin inputs multiplexed to their positive and negative comparator inputs using analog input multiplexers. The analog input multiplexers are completely under software control and configured using SFR registers. See Section "7.6. Comparator0 and Comparator1 Analog Multiplexers" on page 100 for details on how to select and configure Comparator inputs.

**Important Note About Comparator Inputs:** The Port pins selected as Comparator inputs should be configured as analog inputs and skipped by the Crossbar. See the Port I/O chapter for more details on how to configure Port I/O pins as Analog Inputs. The Comparator may also be used to compare the logic level of digital signals, however, Port I/O pins configured as digital inputs must be driven to a valid logic state (HIGH or LOW) to avoid increased power consumption.



Figure 7.1. Comparator 0 Functional Block Diagram



#### 7.5. Comparator Register Descriptions

The SFRs used to enable and configure the comparators are described in the following register descriptions. A Comparator must be enabled by setting the CPnEN bit to logic 1 before it can be used. From an enabled state, a comparator can be disabled and placed in a low power state by clearing the CPnEN bit to logic 0.

**Important Note About Comparator Settings:** False rising and falling edges can be detected by the Comparator while powering on or if changes are made to the hysteresis or response time control bits. Therefore, it is recommended that the rising-edge and falling-edge flags be explicitly cleared to logic 0 a short time after the comparator is enabled or its mode bits have been changed. The Comparator Power Up Time is specified in Section "Table 4.13. Comparator Electrical Characteristics" on page 64.

#### SFR Definition 7.1. CPT0CN: Comparator 0 Control

Bit	7	6	5	4	3	2	1	0
Name	CP0EN	CP0OUT	CP0RIF	CP0FIF	CP0H	YP[1:0]	CP0H	/N[1:0]
Туре	R/W	R	R/W	R/W	R/	W	R/	W
Reset	0	0	0	0	0	0	0	0

#### SFR Page= 0x0; SFR Address = 0x9B

Bit	Name	Function
7	CP0EN	Comparator0 Enable Bit.
		0: Comparator0 Disabled. 1: Comparator0 Enabled.
6	CP0OUT	Comparator0 Output State Flag.
		0: Voltage on CP0+ < CP0 1: Voltage on CP0+ > CP0
5	CP0RIF	Comparator0 Rising-Edge Flag. Must be cleared by software.
		<ul><li>0: No Comparator0 Rising Edge has occurred since this flag was last cleared.</li><li>1: Comparator0 Rising Edge has occurred.</li></ul>
4	CP0FIF	Comparator0 Falling-Edge Flag. Must be cleared by software.
		<ul><li>0: No Comparator0 Falling-Edge has occurred since this flag was last cleared.</li><li>1: Comparator0 Falling-Edge has occurred.</li></ul>
3-2	CP0HYP[1:0]	Comparator0 Positive Hysteresis Control Bits.
		00: Positive Hysteresis Disabled.
		01: Positive Hysteresis = 5 mV. 10: Positive Hysteresis = 10 mV
		11: Positive Hysteresis = 20 mV.
1-0	CP0HYN[1:0]	Comparator0 Negative Hysteresis Control Bits.
		00: Negative Hysteresis Disabled.
		01: Negative Hysteresis = 5 mV.
		11: Negative Hysteresis = 10 mV.



### 10.8. EMIF Timing Diagrams

### 10.8.1. Multiplexed 16-bit MOVX: EMI0CF[3:2] = 01, 10, or 11



Note: See the Port Input/Output chapter to determine which port pins are mapped to the ADDR[11:8], AD[7:0], ALE, /RD, and /WR signals.



Rev. 1.4



### 13. Flash Memory

On-chip, re-programmable Flash memory is included for program code and non-volatile data storage. The Flash memory can be programmed in-system through the C2 interface or by software using the MOVX write instruction. Once cleared to logic 0, a Flash bit must be erased to set it back to logic 1. Flash bytes would typically be erased (set to 0xFF) before being reprogrammed. The write and erase operations are automatically timed by hardware for proper execution; data polling to determine the end of the write/erase operations is not required. Code execution is stalled during Flash write/erase operations. Refer to Table 4.6 for complete Flash memory electrical characteristics.

#### 13.1. Programming The Flash Memory

The simplest means of programming the Flash memory is through the C2 interface using programming tools provided by Silicon Laboratories or a third party vendor. This is the only means for programming a non-initialized device. For details on the C2 commands to program Flash memory, see Section "27. C2 Interface" on page 324.

The Flash memory can be programmed by software using the MOVX write instruction with the address and data byte to be programmed provided as normal operands. Before programming Flash memory using MOVX, Flash programming operations must be enabled by: (1) setting the PSWE Program Store Write Enable bit (PSCTL.0) to logic 1 (this directs the MOVX writes to target Flash memory); and (2) Writing the Flash key codes in sequence to the Flash Lock register (FLKEY). The PSWE bit remains set until cleared by software. For detailed guidelines on programming Flash from firmware, please see Section "13.5. Flash Write and Erase Guidelines" on page 153.

To ensure the integrity of the Flash contents, the on-chip VDD Monitor must be enabled and enabled as a reset source in any system that includes code that writes and/or erases Flash memory from software. Furthermore, there should be no delay between enabling the  $V_{DD}$  Monitor and enabling the  $V_{DD}$  Monitor as a reset source. Any attempt to write or erase Flash memory while the  $V_{DD}$  Monitor is disabled, or not enabled as a reset source, will cause a Flash Error device reset.

#### 13.1.1. Flash Lock and Key Functions

Flash writes and erases by user software are protected with a lock and key function. The Flash Lock and Key Register (FLKEY) must be written with the correct key codes, in sequence, before Flash operations may be performed. The key codes are: 0xA5, 0xF1. The timing does not matter, but the codes must be written in order. If the key codes are written out of order, or the wrong codes are written, Flash writes and erases will be disabled until the next system reset. Flash writes and erases will also be disabled if a Flash write or erase is attempted before the key codes have been written properly. The Flash lock resets after each write or erase; the key codes must be written again before a following Flash operation can be performed. The FLKEY register is detailed in SFR Definition 13.2.



#### 15.2. 32-bit CRC Algorithm

The C8051F93x-C8051F92x CRC unit calculates the 32-bit CRC using a poly of 0x04C11DB7. The CRC-32 algorithm is "reflected", meaning that all of the input bytes and the final 32-bit output are bit-reversed in the processing engine. The following is a description of a simplified CRC algorithm that produces results identical to the hardware:

- Step 1. XOR the least-significant byte of the current CRC result with the input byte. If this is the first iteration of the CRC unit, the current CRC result will be the set initial value (0x00000000 or 0xFFFFFFF).
- Step 2. Right-shift the CRC result.
- Step 3. If the LSB of the CRC result is set, XOR the CRC result with the reflected polynomial (0xEDB88320).
- Step 4. Repeat at Step 2 for the number of input bits (8).

For example, the 32-bit 'F93x/92x CRC algorithm can be described by the following code:

```
unsigned long UpdateCRC (unsigned long CRC_acc, unsigned char CRC_input)
{
   unsigned char i; // loop counter
   #define POLY 0xEDB88320 // bit-reversed version of the poly 0x04C11DB7
   // Create the CRC "dividend" for polynomial arithmetic (binary arithmetic
   // with no carries)
   CRC_acc = CRC_acc ^ CRC_input;
   // "Divide" the poly into the dividend using CRC XOR subtraction
   // CRC acc holds the "remainder" of each divide
   11
   // Only complete this division for 8 bits since input is 1 byte
   for (i = 0; i < 8; i++)
   {
      // Check if the MSB is set (if MSB is 1, then the POLY can "divide"
      // into the "dividend")
      if ((CRC acc & 0x00000001) == 0x00000001)
      {
         // if so, shift the CRC value, and XOR "subtract" the poly
         CRC_acc = CRC_acc >> 1;
         CRC_acc ^= POLY;
      }
      else
      ł
         // if not, just shift the CRC value
         CRC_acc = CRC_acc >> 1;
      }
   }
   // Return the final remainder (CRC value)
   return CRC_acc;
}
```

The following table lists several input values and the associated outputs using the 32-bit 'F93x/92x CRC algorithm (an initial value of 0xFFFFFFF is used):



#### **19.1.** Programmable Precision Internal Oscillator

All C8051F93x-C8051F92x devices include a programmable precision internal oscillator that may be selected as the system clock. OSCICL is factory calibrated to obtain a 24.5 MHz frequency. See Section "4. Electrical Characteristics" on page 45 for complete oscillator specifications.

The precision oscillator supports a spread spectrum mode which modulates the output frequency in order to reduce the EMI generated by the system. When enabled (SSE = 1), the oscillator output frequency is modulated by a stepped triangle wave whose frequency is equal to the oscillator frequency divided by 384 (63.8 kHz using the factory calibration). The deviation from the nominal oscillator frequency is +0%, -1.6%, and the step size is typically 0.26% of the nominal frequency. When using this mode, the typical average oscillator frequency is lowered from 24.5 MHz to 24.3 MHz.

#### 19.2. Low Power Internal Oscillator

All C8051F93x-C8051F92x devices include a low power internal oscillator that defaults as the system clock after a system reset. The low power internal oscillator frequency is  $20 \text{ MHz} \pm 10\%$  and is automatically enabled when selected as the system clock and disabled when not in use. See Section "4. Electrical Characteristics" on page 45 for complete oscillator specifications.

#### **19.3. External Oscillator Drive Circuit**

All C8051F93x-C8051F92x devices include an external oscillator circuit that may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. Figure 19.1 shows a block diagram of the four external oscillator options. The external oscillator is enabled and configured using the OSCXCN register.

The external oscillator output may be selected as the system clock or used to clock some of the digital peripherals (e.g., timers, PCA, etc.). See the data sheet chapters for each digital peripheral for details. See Section "4. Electrical Characteristics" on page 45 for complete oscillator specifications.

#### 19.3.1. External Crystal Mode

If a crystal or ceramic resonator is used as the external oscillator, the crystal/resonator and a 10 M $\Omega$  resistor must be wired across the XTAL1 and XTAL2 pins as shown in Figure 19.1, Option 1. Appropriate loading capacitors should be added to XTAL1 and XTAL2, and both pins should be configured for analog I/O with the digital output drivers disabled.

Figure 19.2 shows the external oscillator circuit for a 20 MHz quartz crystal with a manufacturer recommended load capacitance of 12.5 pF. Loading capacitors are "in series" as seen by the crystal and "in parallel" with the stray capacitance of the XTAL1 and XTAL2 pins. The total value of the each loading capacitor and the stray capacitance of each XTAL pin should equal 12.5pF x 2 = 25 pF. With a stray capacitance of 10 pF per pin, the 15 pF capacitors yield an equivalent series capacitance of 12.5 pF across the crystal.

**Note:** The recommended load capacitance depends upon the crystal and the manufacturer. Refer to the crystal data sheet when completing these calculations.



Table 20.3 shows a summary of the oscillator bias settings. The SmaRTClock Bias Doubling feature allows the self-oscillation frequency to be increased (almost doubled) and allows a higher crystal drive strength in crystal mode. High crystal drive strength is recommended when the crystal is exposed to poor environmental conditions such as excessive moisture. SmaRTClock Bias Doubling is enabled by setting BIASX2 (RTC0XCN.5) to 1.

Mode	Setting	Power Consumption
Crystal	Bias Double Off, AGC On	Lowest 600 nA
	Bias Double Off, AGC Off	Low 800 nA
	Bias Double On, AGC On	High
	Bias Double On, AGC Off	Highest
Self-Oscillate	Bias Double Off	Low
	Bias Double On	High

 Table 20.3. SmaRTClock Bias Settings





Figure 21.4. Crossbar Priority Decoder with Crystal Pins Skipped

![](_page_14_Picture_3.jpeg)

### SFR Definition 21.13. P1: Port1

Bit	7	6	5	1	3	2	1	0
Dit		0	5	-	5	2	•	0
Name	P1[7:0]							
Туре	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Page = All Pages; SFR Address = 0x90; Bit-Addressable

Bit	Name	Description	Write	Read			
7:0	P1[7:0]	<b>Port 1 Data.</b> Sets the Port latch logic value or reads the Port pin logic state in Port cells con- figured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P1.n Port pin is logic LOW. 1: P1.n Port pin is logic HIGH.			
Note: F	Note: Pin P1.7 is only available in 32-pin devices.						

### SFR Definition 21.14. P1SKIP: Port1 Skip

Bit	7	6	5	4	3	2	1	0
Name	P1SKIP[7:0]							
Туре	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xD5

Bit	Name	Function			
7:0	P1SKIP[7:0]	Port 1 Crossbar Skip Enable Bits.			
		<ul> <li>These bits select Port 1 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar.</li> <li>0: Corresponding P1.n pin is not skipped by the Crossbar.</li> <li>1: Corresponding P1.n pin is skipped by the Crossbar.</li> </ul>			
Note:	Pin P1.7 is only available in 32-pin devices.				

![](_page_15_Picture_9.jpeg)

Setting the EXTHOLD bit extends the minimum setup and hold times for the SDA line. The minimum SDA setup time defines the absolute minimum time that SDA is stable before SCL transitions from low-to-high. The minimum SDA hold time defines the absolute minimum time that the current SDA value remains stable after SCL transitions from high-to-low. EXTHOLD should be set so that the minimum setup and hold times meet the SMBus Specification requirements of 250 ns and 300 ns, respectively. Table 22.2 shows the minimum setup and hold times for the two EXTHOLD settings. Setup and hold time extensions are typically necessary when SYSCLK is above 10 MHz.

EXTHOLD	Minimum SDA Setup Time	Minimum SDA Hold Time			
	T <sub>low</sub> – 4 system clocks				
0	or	3 system clocks			
	1 system clock + s/w delay*				
1	11 system clocks	12 system clocks			
*Note: Setup Time for ACK bit transmissions and the MSB of all data transfers. When using software acknowledgement, the s/w delay occurs between the time SMB0DAT or ACK is written and when SI is cleared. Note that if SI is cleared in the same write that defines the outgoing ACK value, s/w delay is zero.					

#### Table 22.2. Minimum SDA Setup and Hold Times

With the SMBTOE bit set, Timer 3 should be configured to overflow after 25 ms in order to detect SCL low timeouts (see Section "22.3.4. SCL Low Timeout" on page 241). The SMBus interface will force Timer 3 to reload while SCL is high, and allow Timer 3 to count when SCL is low. The Timer 3 interrupt service routine should be used to reset SMBus communication by disabling and re-enabling the SMBus.

SMBus Free Timeout detection can be enabled by setting the SMBFTE bit. When this bit is set, the bus will be considered free if SDA and SCL remain high for more than 10 SMBus clock source periods (see Figure 22.4).

![](_page_16_Picture_6.jpeg)

### 24.5. Serial Clock Phase and Polarity

Four combinations of serial clock phase and polarity can be selected using the clock control bits in the SPI Configuration Register (SPInCFG). The CKPHA bit (SPInCFG.5) selects one of two clock phases (edge used to latch the data). The CKPOL bit (SPInCFG.4) selects between an active-high or active-low clock. Both master and slave devices must be configured to use the same clock phase and polarity. SPI0 should be disabled (by clearing the SPIENn bit, SPInCN.0) when changing the clock phase or polarity. The clock and data line relationships for master mode are shown in Figure 24.5. For slave mode, the clock and data relationships are shown in Figure 24.6 and Figure 24.7. Note that CKPHA must be set to 0 on both the master and slave SPI when communicating between two of the following devices: C8051F04x, C8051F06x, C8051F12x, C8051F31x, C8051F32x, and C8051F33x.

The SPIn Clock Rate Register (SPInCKR) as shown in SFR Definition 24.3 controls the master mode serial clock frequency. This register is ignored when operating in slave mode. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency or 12.5 MHz, whichever is slower. When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS (in 4-wire slave mode), and the serial input data synchronously with the slave's system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the slave's system clock frequency.

![](_page_17_Figure_4.jpeg)

Figure 24.5. Master Mode Data/Clock Timing

![](_page_17_Picture_6.jpeg)

![](_page_18_Figure_1.jpeg)

\* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

![](_page_18_Figure_3.jpeg)

![](_page_18_Figure_4.jpeg)

\* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

![](_page_18_Figure_6.jpeg)

![](_page_18_Picture_7.jpeg)

![](_page_19_Figure_1.jpeg)

Figure 25.1. T0 Mode 0 Block Diagram

#### 25.1.2. Mode 1: 16-bit Counter/Timer

Mode 1 operation is the same as Mode 0, except that the counter/timer registers use all 16 bits. The counter/timers are enabled and configured in Mode 1 in the same manner as for Mode 0.

![](_page_19_Picture_5.jpeg)

#### 26.3.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.

![](_page_20_Figure_3.jpeg)

Figure 26.4. PCA Capture Mode Diagram

**Note:** The CEXn input signal must remain high or low for at least 2 system clock cycles to be recognized by the hardware.

![](_page_20_Picture_6.jpeg)