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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	716800
Number of I/O	222
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lae3-17ea-6fn484e

Table 2-5. DLL Signals

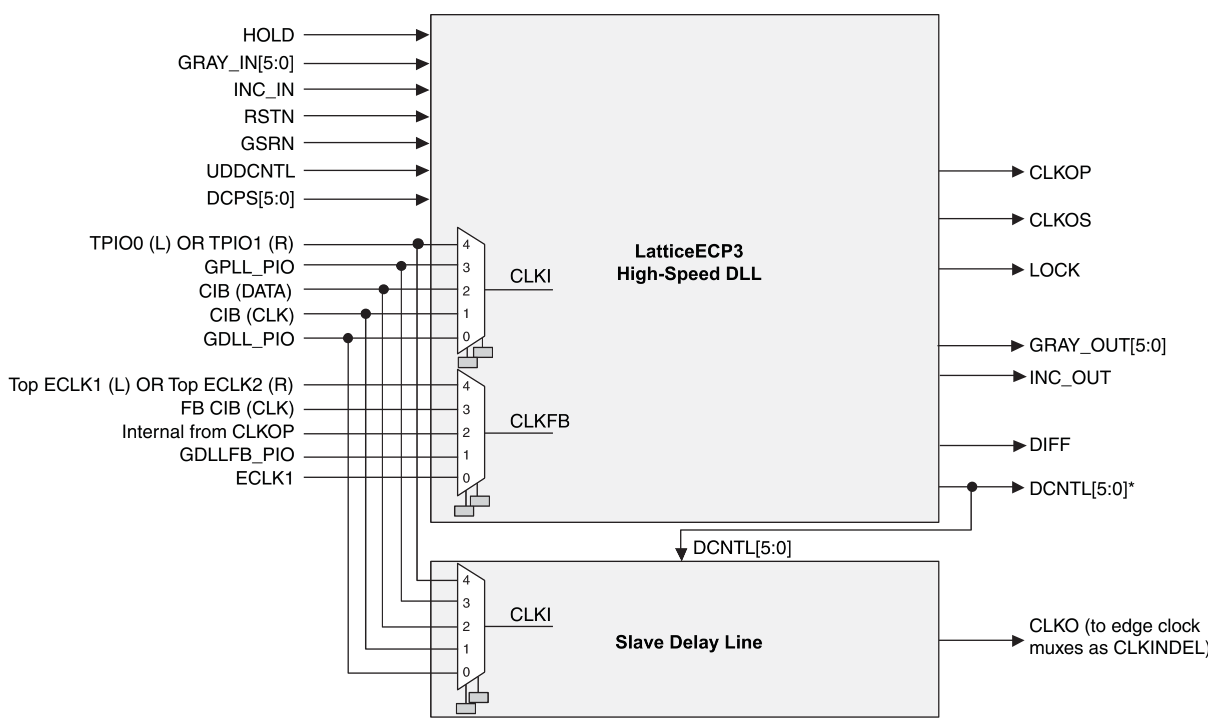
Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine delay shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator
INCI	I	Incremental indicator from another DLL via CIB.
GRAYI[5:0]	I	Gray-coded digital control bus from another DLL in time reference mode.
DIFF	O	Difference indicator when DCNTL is difference than the internal setting and update is needed.
INCO	O	Incremental indicator to other DLLs via CIB.
GRAYO[5:0]	O	Gray-coded digital control bus to other DLLs via CIB

LA-LatticeECP3 devices have two general DLLs and four Slave Delay lines, two per DLL. The DLLs are in the lowest EBR row and located adjacent to the EBR. Each DLL replaces one EBR block. One Slave Delay line is placed adjacent to the DLL and the duplicate Slave Delay line (in Figure 2-6) for the DLL is placed in the I/O ring between Banks 6 and 7 and Banks 2 and 3.

The outputs from the DLL and Slave Delay lines are fed to the clock distribution network.

For more information, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide.

Figure 2-6. Top-Level Block Diagram, High-Speed DLL and Slave Delay Line

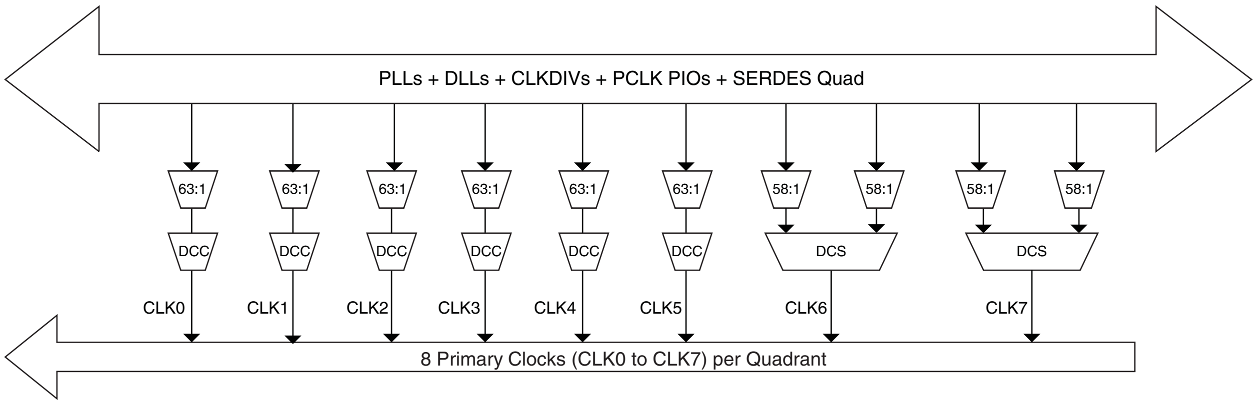


* This signal is not user accessible. It can only be used to feed the slave delay line.

Primary Clock Routing

The purpose of the primary clock routing is to distribute primary clock sources to the destination quadrants of the device. A global primary clock is a primary clock that is distributed to all quadrants. The clock routing structure in LA-LatticeECP3 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-11 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

Figure 2-11. Per Quadrant Primary Clock Selection



Dynamic Clock Control (DCC)

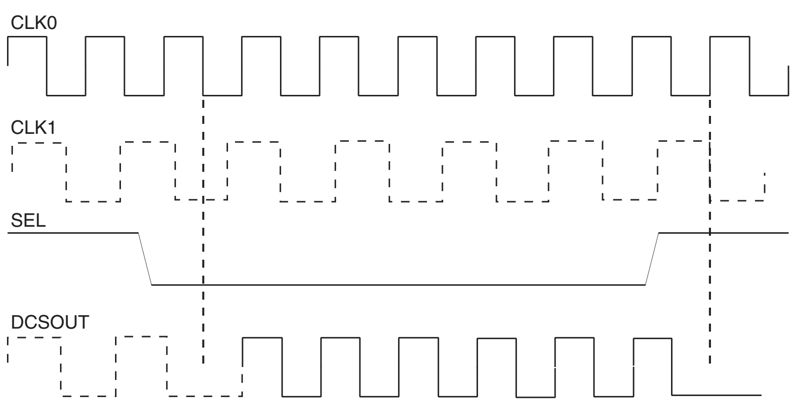
The DCC (Quadrant Clock Enable/Disable) feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, all the logic fed by that clock does not toggle, reducing the overall power consumption of the device.

Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-11).

Figure 2-12 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.

Figure 2-12. DCS Waveforms



Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

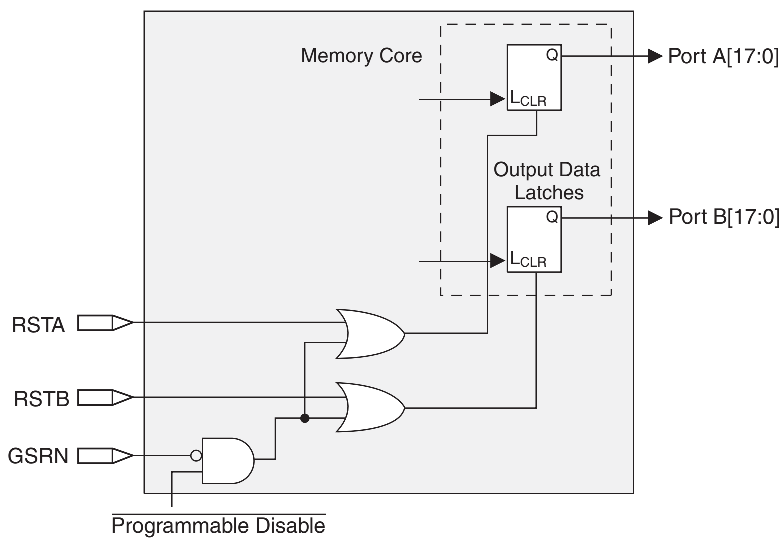
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-21.

Figure 2-21. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

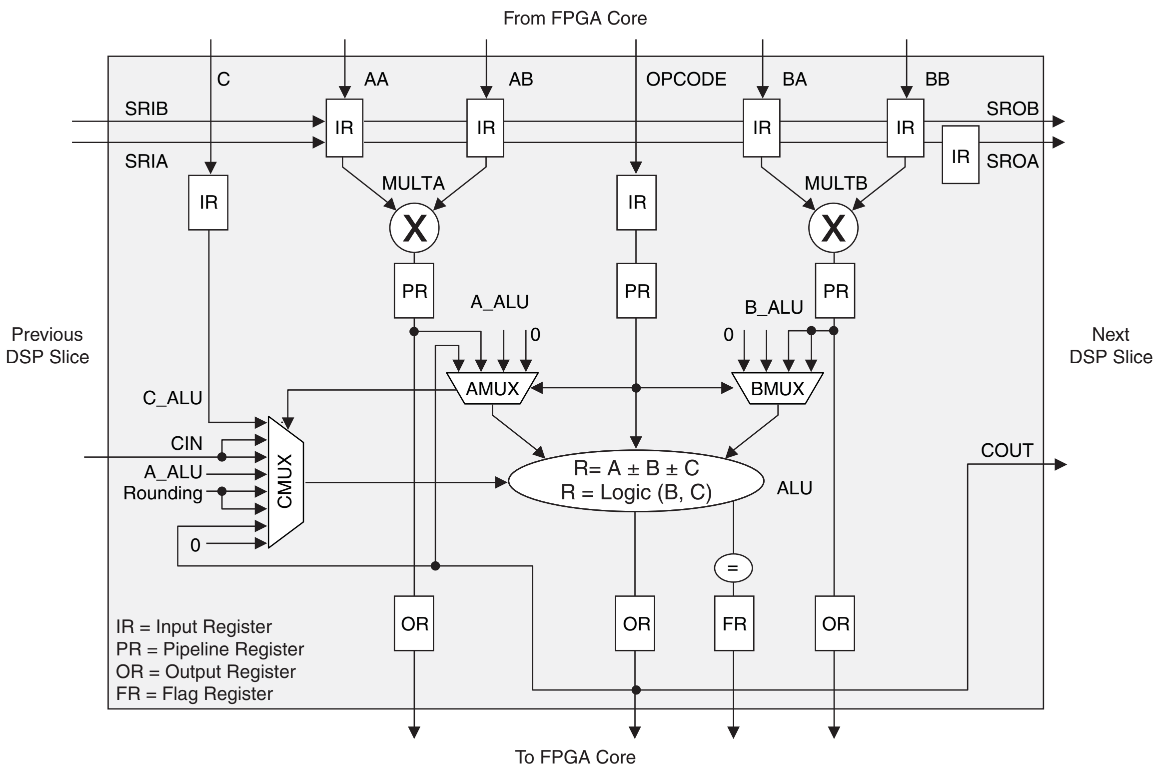
sysDSP™ Slice

The LA-LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LA-LatticeECP3, on the other hand, has many DSP slices that support different data

Figure 2-24. Detailed sysDSP Slice Diagram



Note: A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LA-LatticeECP3 slices versus the above functions.

Table 2-8. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1[1]	1/2	—

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

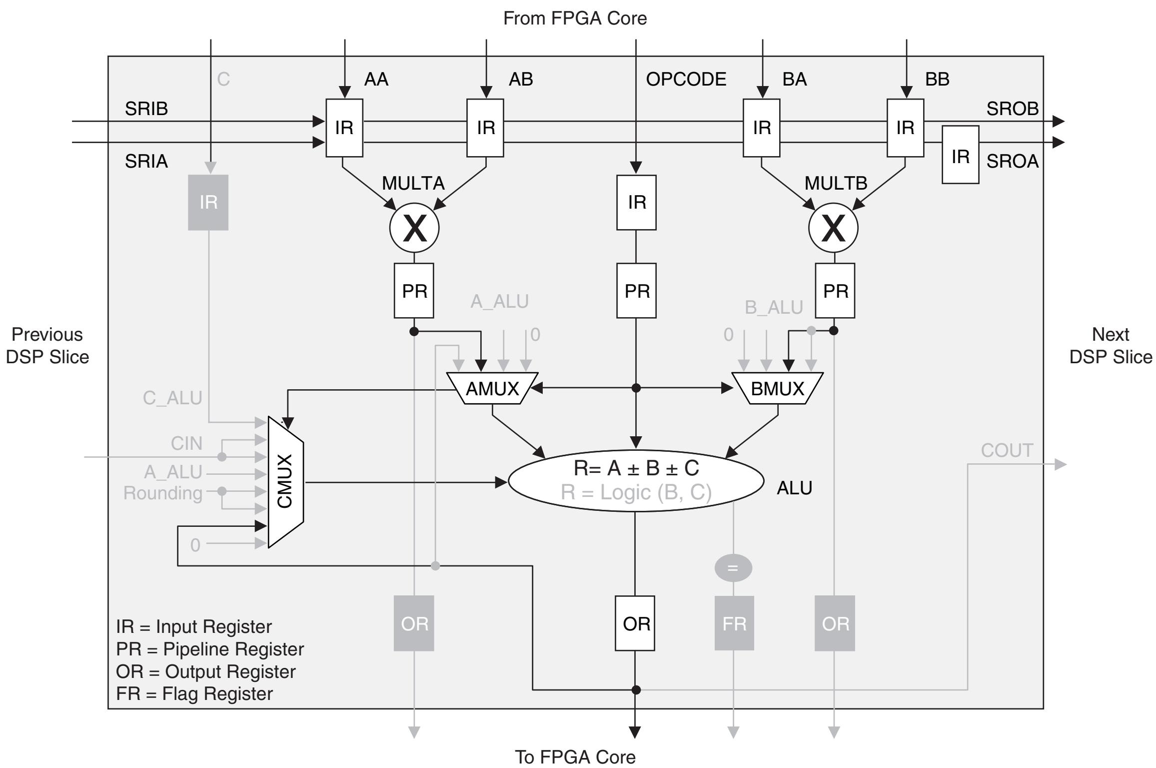
Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

MMAC DSP Element

The LA-LatticeECP3 supports a MAC with two multipliers. This is called Multiply Multiply Accumulate or MMAC. In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value and with the result of the multiplier operation of operands BA and BB. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-27 shows the MMAC sysDSP element.

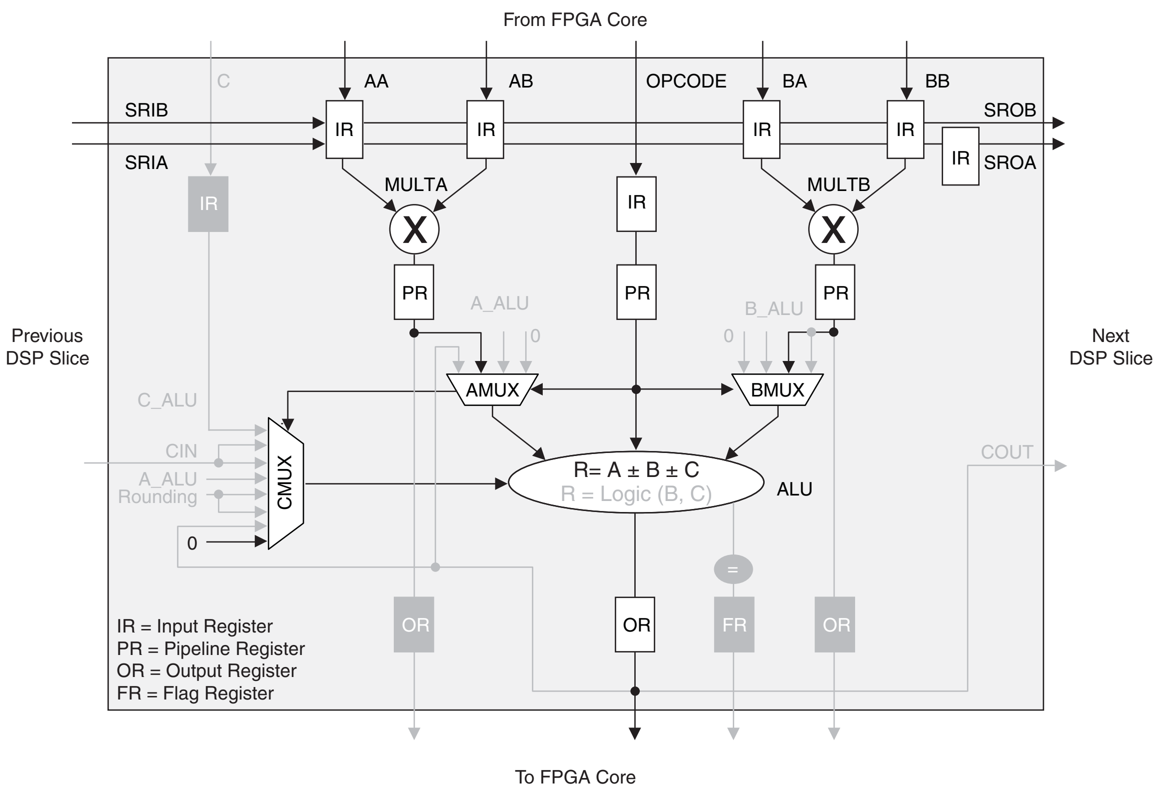
Figure 2-27. MMAC sysDSP Element



MULTADDSUB DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB. The user can enable the input, output and pipeline registers. Figure 2-28 shows the MULTADDSUB sysDSP element.

Figure 2-28. MULTADDSUB



Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In single data rate (SDR) the data is registered with the system clock by one of the registers in the single data rate sync register block.

In DDR mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (ECLKDQSR) in the DDR Memory mode or ECLK signal when using DDR Generic mode, creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

A gearbox function can be implemented in each of the input registers on the left and right sides. The gearbox function takes a double data rate signal applied to PIOA and converts it as four data streams, INA, IPA, INB and IPB. The two data streams from the first set of DDR registers are synchronized to the edge clock and then to the system clock before entering the core. Figure 2-29 provides further information on the use of the gearbox function.

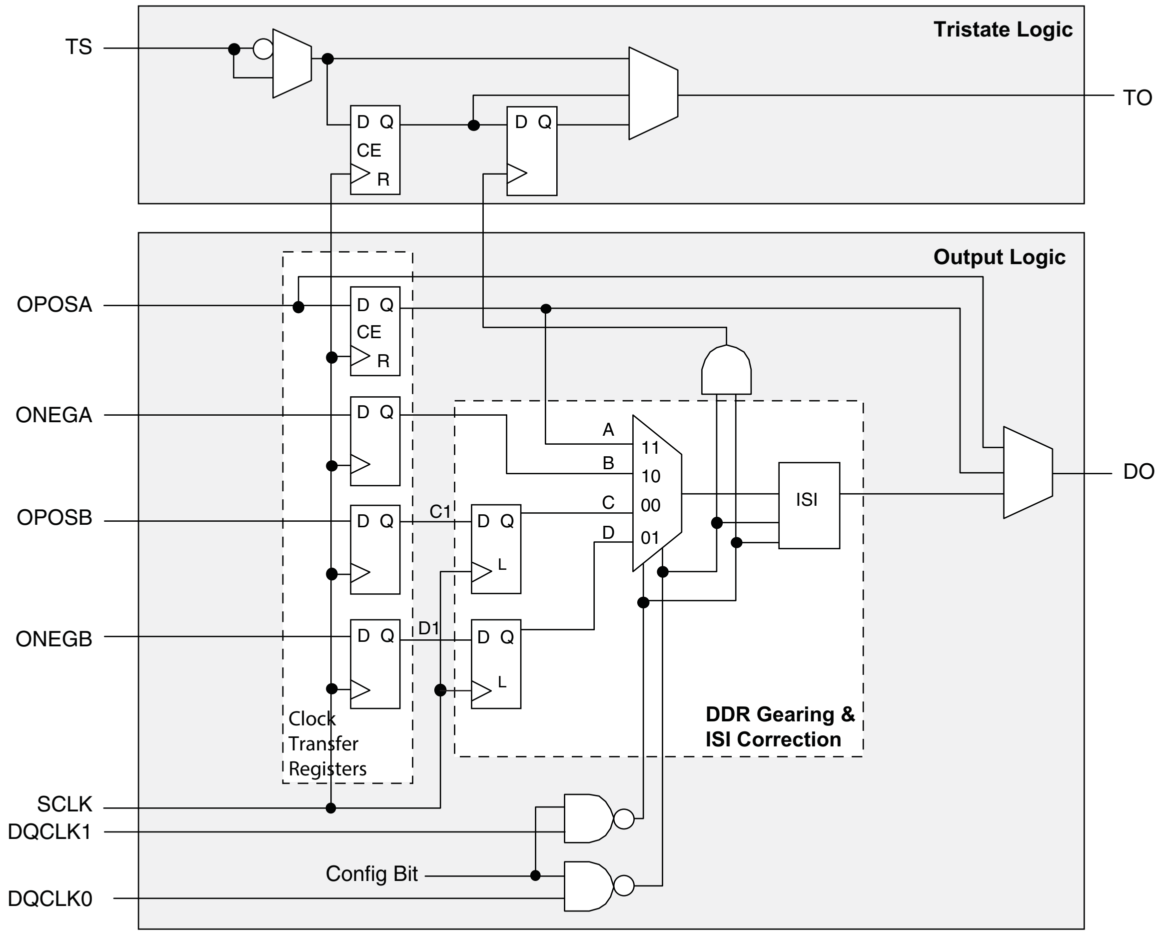
The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the ECLKDQSR (DDR Memory Interface mode) or ECLK (DDR Generic mode). The DDRLAT signal is used to ensure the data transfer from the synchronization registers to the clock transfer and gearbox registers.

The ECLKDQSR, DDRCLKPOL and DDRLAT signals are generated in the DQS Read Control Logic Block. See Figure 2-36 for an overview of the DQS read control logic.

Further discussion about using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Figure 2-33. Output and Tristate Block for Left and Right Edges



Tristate Register Block

The tristate register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional register for DDR operation.

In SDR and non-gearing DDR modes, TS input feeds one of the flip-flops that then feeds the output. In DDRX2 mode, the register TS input is fed into another register that is clocked using the DQCLK0 and DQCLK1 signals. The output of this register is used as a tristate control.

ISI Calibration

The setting for Inter-Symbol Interference (ISI) cancellation occurs in the output register block. ISI correction is only available in the DDRX2 modes. ISI calibration settings exist once per output register block, so each I/O in a DQS-12 group may have a different ISI calibration setting.

The ISI block extends output signals at certain times, as a function of recent signal history. So, if the output pattern consists of a long strings of 0's to long strings of 1's, there are no delays on output signals. However, if there are quick, successive transitions from 010, the block will stretch out the binary 1. This is because the long trail of 0's will cause these symbols to interfere with the logic 1. Likewise, if there are quick, successive transitions from 101, the block will stretch out the binary 0. This block is controlled by a 3-bit delay control that can be set in the DQS control logic block.

For more information about this topic, please see the list of technical documentation at the end of this data sheet.

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block.

DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high-speed source synchronous and DDR, DDR2 and DDR3 memory interfaces. The support varies by the edge of the device as detailed below.

Left and Right Edges

The left and right sides of the PIC have fully functional elements supporting DDR, DDR2, and DDR3 memory interfaces. One of every 12 PIOs supports the dedicated DQS pins with the DQS control logic block. Figure 2-34 shows the DQS bus spanning 11 I/O pins. Two of every 12 PIOs support the dedicated DQS and DQS# pins with the DQS control logic block.

Bottom Edge

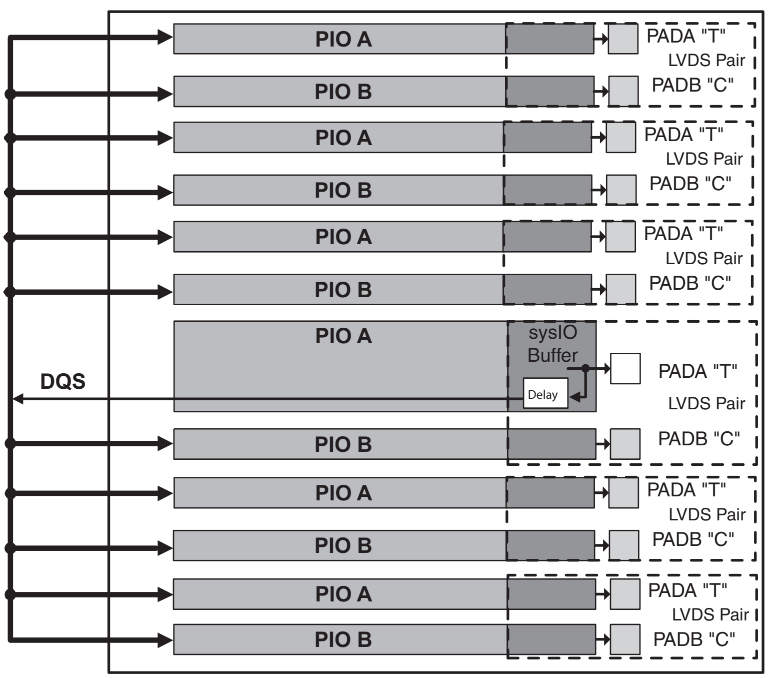
PICs on the bottom edge of the device do not support DDR memory and Generic DDR interfaces.

Top Edge

PICs on the top side are similar to the PIO elements on the left and right sides but do not support gearing on the output registers. Hence, the modes to support output/tristate DDR3 memory are removed on the top side.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left, right and top edges are designed for DDR memories that support 10 bits of data.

Figure 2-34. DQS Grouping on the Left, Right and Top Edges



DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces, a PLL is used for this adjustment. However, in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The delay required for the DQS signal is generated by two dedicated DLLs (DDR DLL) on opposite side of the device. Each DLL creates DQS delays in its half of the device as shown in Figure 2-36. The DDR DLL on the left side will generate delays for all the DQS Strobe pins on Banks 0, 7 and 6 and DDR DLL on the right will generate delays for all the DQS pins on Banks 1, 2 and 3. The DDR DLL loop compensates for temperature, voltage and process variations by using the system clock and DLL feedback loop. DDR DLL communicates the required delay to the DQS delay block using a 7-bit calibration bus (DCNTL[6:0])

The DQS signal (selected PIOs only, as shown in Figure 2-34) feeds from the PAD through a DQS control logic block to a dedicated DQS routing resource. The DQS control logic block consists of DQS Read Control logic block that generates control signals for the read side and DQS Write Control logic that generates the control signals required for the write side. A more detailed DQS control diagram is shown in Figure 2-36, which shows how the DQS control blocks interact with the data paths.

The DQS Read control logic receives the delay generated by the DDR DLL on its side and delays the incoming DQS signal by 90 degrees. This delayed ECLKDQSR is routed to 10 or 11 DQ pads covered by that DQS signal. This block also contains a polarity control logic that generates a DDRCLKPOL signal, which controls the polarity of the clock to the sync registers in the input register blocks. The DQS Read control logic also generates a DDRLAT signal that is in the input register block to transfer data from the first set of DDR register to the second set of DDR registers when using the DDRX2 gearbox mode for DDR3 memory interface.

The DQS Write control logic block generates the DQCLK0 and DQCLK1 clocks used to control the output gearing in the Output register block which generates the DDR data output and the DQS output. They are also used to control the generation of the DQS output through the DQS output register block. In addition to the DCNTL [6:0] input from the DDR DLL, the DQS Write control block also uses a Dynamic Delay DYN DEL [7:0] attribute which is used to further delay the DQS to accomplish the write leveling found in DDR3 memory. Write leveling is controlled by the DDR memory controller implementation. The DYN DELAY can set 128 possible delay step settings. In addition, the most significant bit will invert the clock for a 180-degree shift of the incoming clock. This will generate the DQSW signal used to generate the DQS output in the DQS output register block.

Figure 2-35 and Figure 2-36 show how the DQS transition signals that are routed to the PIOs.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

2. **Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**
   The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

   LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

3. **Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)**
   The sysI/O buffers in the Configuration Bank consist of ratioed single-ended output drivers and single-ended input buffers. This bank does not support PCI clamp like the other banks on the top, left, and right sides.

   The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on the top banks. PCI clamps are used primarily on inputs and bi-directional pads to reduce ringing on the receiving end.

Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LA-LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysI/O Standards

The LA-LatticeECP3 sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. For further information on utilizing the sysI/O buffer to support a variety of standards please see TN1177, LatticeECP3 sysIO Usage Guide.

transmit reference clock will cause a violation of the Gigabit Ethernet, Serial RapidIO and SGMII transmit jitter specifications.

For further information on SERDES, please see TN1176, LatticeECP3 SERDES/PCS Usage Guide.

IEEE 1149.1-Compliant Boundary Scan Testability

All LA-LatticeECP3 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more information, please see TN1169, LatticeECP3 sysCONFIG Usage Guide.

Device Configuration

All LA-LatticeECP3 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support dual-byte, byte and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In- System Configuration specification. The sysCONFIG port includes seven I/Os used as dedicated pins with the remaining pins used as dual-use pins. See TN1169, LatticeECP3 sysCONFIG Usage Guide for more information about using the dual-use pins as general purpose I/Os.

There are various ways to configure a LA-LatticeECP3 device:

1. JTAG
2. Standard Serial Peripheral Interface (SPI and SPIm modes) - interface to boot PROM memory
3. System microprocessor to drive a x8 CPU port (PCM mode)
4. System microprocessor to drive a serial slave SPI port (SSPI mode)
5. Generic byte wide flash with a MachXO™ device, providing control and addressing

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

LA-LatticeECP3 devices also support the Slave SPI Interface. In this mode, the FPGA behaves like a SPI Flash device (slave mode) with the SPI port of the FPGA to perform read-write operations.

Enhanced Configuration Options

LA-LatticeECP3 devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dual-boot image support.

1. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See TN1087, Minimizing System Interruption During Configuration Using TransFR Technology for details.
2. **Dual-Boot Image Support**
   Dual-boot images are supported for applications requiring reliable remote updates of configuration data for the

MLVDS25

The LA-LatticeECP3 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

Figure 3-5. MLVDS25 (Multipoint Low Voltage Differential Signaling)

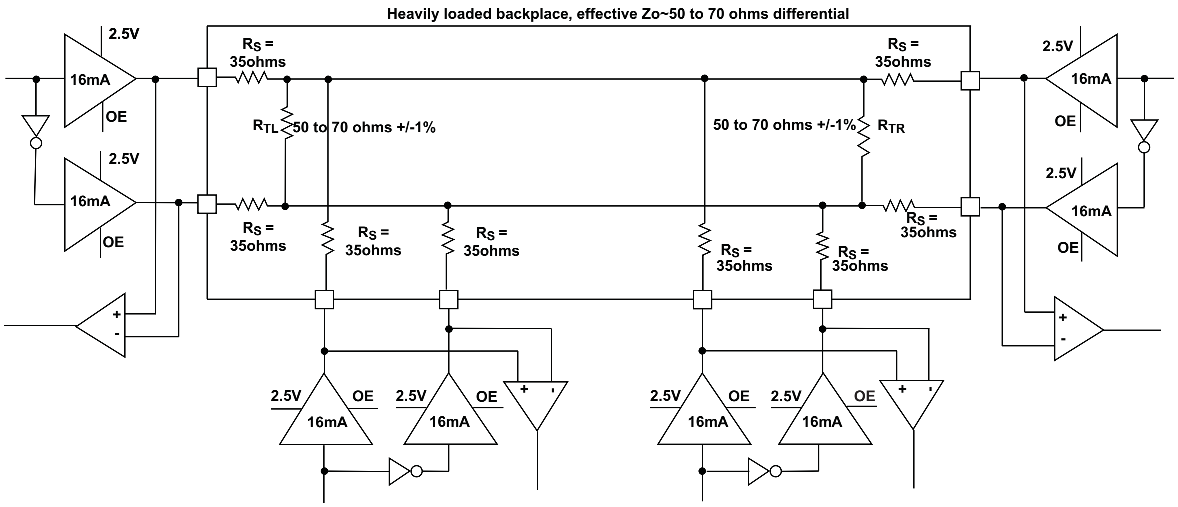


Table 3-7. MLVDS25 DC Conditions[1]

Parameter	Description	Typical		Units
		Zo=50Ω	Zo=70Ω	
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (+/-1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage	1.52	1.60	V
V_{OL}	Output Low Voltage	0.98	0.90	V
V_{OD}	Output Differential Voltage	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

Parameter	Description	Device	-6 / -6L		Units
			Min.	Max.	
General I/O Pin Parameters (using dedicated clock input Primary Clock with PLL with clock injection removal setting) [2]					
t_{COPLL}	Clock to Output - PIO Output Register	LAE3-35EA	-	2.72	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	LAE3-35EA	0.81	-	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	LAE3-35EA	0.37	-	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LAE3-35EA	1.82	-	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LAE3-35EA	0.00	-	ns
t_{COPLL}	Clock to Output - PIO Output Register	LAE3-17EA	-	2.49	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	LAE3-17EA	0.81	-	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	LAE3-17EA	0.37	-	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LAE3-17EA	1.82	-	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LAE3-17EA	0.00	-	ns
Generic DDR[12]					
Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_RX.SCLK.Centered) Using PCLK Pin for Clock Input					
t_{SUGDDR}	Data Setup Before CLK	All Devices	480	—	ps
t_{HOGDDR}	Data Hold After CLK	All Devices	480	—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	All Devices	—	250	MHz
Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX1_RX.SCLK.PLL.Aligned) Using PLLCLKIN Pin for Clock Input					
Data Left, Right, and Top Sides and Clock Left and Right Sides					
$t_{DVACLKGDDR}$	Data Setup Before CLK	All Devices	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	All Devices	0.775	—	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency	All Devices	—	250	MHz
Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX1_RX.SCLK.Aligned) Using DLL - CLKIN Pin for Clock Input					
Data Left, Right and Top Sides and Clock Left and Right Sides					
$t_{DVACLKGDDR}$	Data Setup Before CLK	All Devices	-	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	All Devices	0.775	-	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency	All Devices	-	250	MHz

LA-LatticeECP3 Internal Switching Characteristics[1]

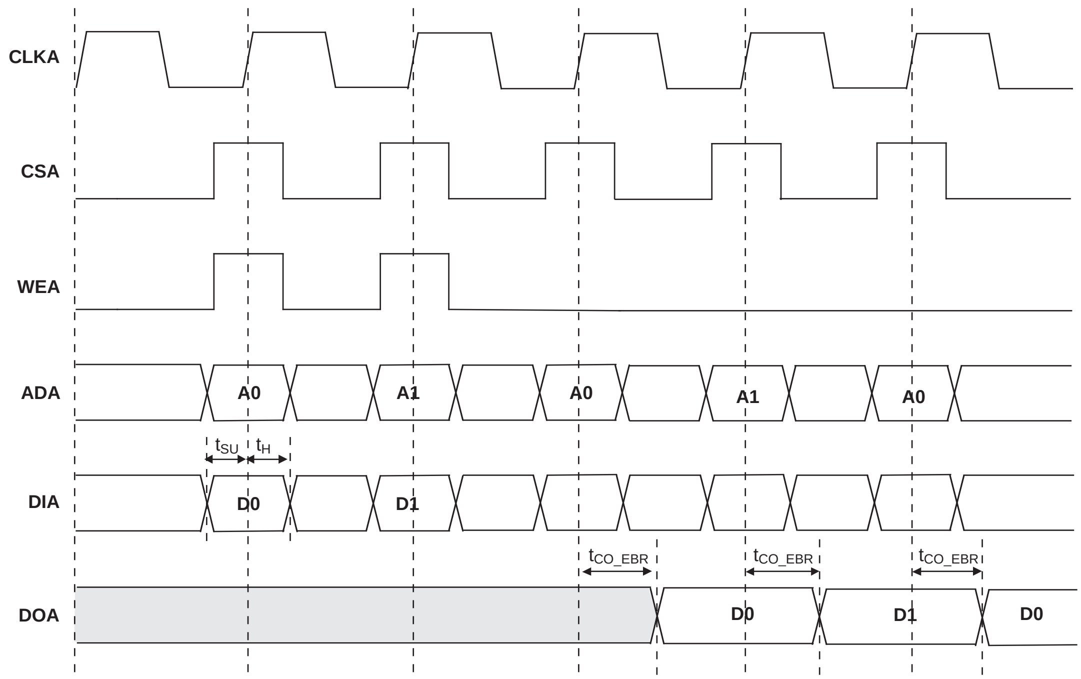
Over Recommended Operating Conditions

Parameter	Description	-6 / -6L		Units
		Min.	Max.	
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.080	-	ns
PLL Parameters				
t_{RSTREC_GPLL}	Reset Recovery to Rising Clock	1.00	—	ns
DSP Block Timing[2, 3]				
t_{SUI_DSP}	Input Register Setup Time	0.39	—	ns
t_{HI_DSP}	Input Register Hold Time	-0.21	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	2.39	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	-1.16	—	ns
t_{SUO_DSP}	Output Register Setup Time	3.37	—	ns
t_{HO_DSP}	Output Register Hold Time	-1.86	—	ns
t_{COI_DSP}	Input Register Clock to Output Time	—	3.77	ns
t_{COP_DSP}	Pipeline Register Clock to Output Time	—	1.66	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	0.63	ns
t_{SUOPT_DSP}	Opcode Register Setup Time	0.39	—	ns
t_{HOPT_DSP}	Opcode Register Hold Time	-0.27	—	ns
t_{SUDATA_DSP}	Cascade_data through ALU to Output Register Setup Time	2.16	—	ns
t_{HPDATA_DSP}	Cascade_data through ALU to Output Register Hold Time	-0.98	—	ns

1. Internal parameters are characterized but not tested on every device.
2. These parameters apply to LA-LatticeECP3 devices only.
3. DSP Block is configured in Multiply Add/Sub 18x18 Mode.

Timing Diagrams

Figure 3-9. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-10. Read/Write Mode with Input and Output Registers

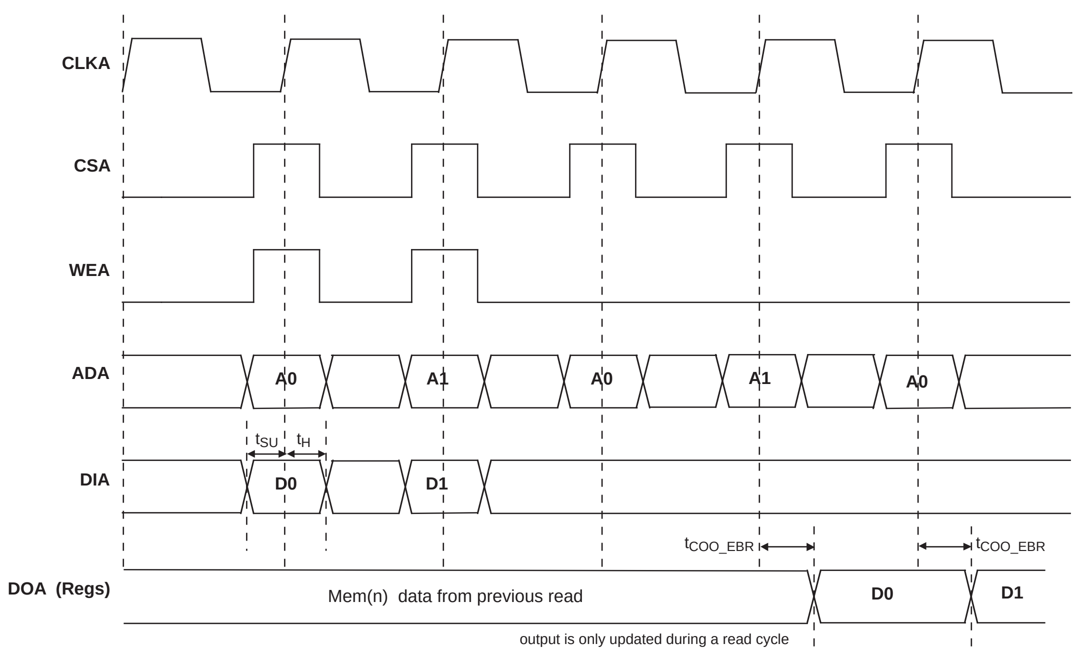
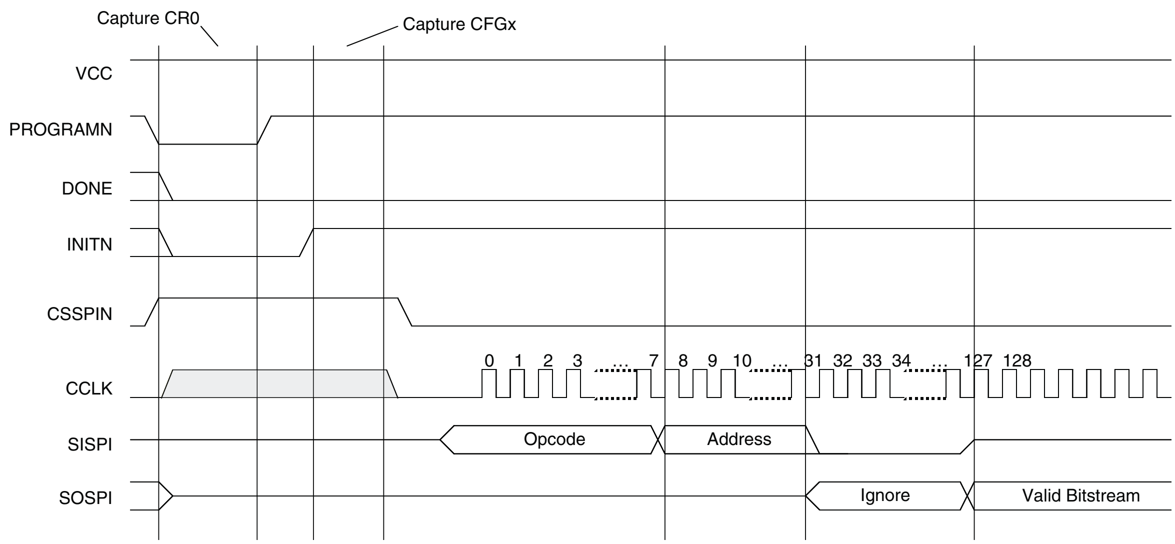


Table 3-25. Master SPI Configuration Waveforms



Signal Descriptions (Cont.)

Signal Name	I/O	Description
D7/SPID0	I/O	Parallel configuration I/O. SPI/SPIm data input. Open drain during configuration.
DI/CSSPI0N/CEN	I/O	Serial data input for slave serial mode. SPI/SPIm mode chip select.
Dedicated SERDES Signals[3]		
PCS[Index]_HDINNm	I	High-speed input, negative channel m
PCS[Index]_HDOUTNm	O	High-speed output, negative channel m
PCS[Index]_REFCLKN	I	Negative Reference Clock Input
PCS[Index]_HDINPm	I	High-speed input, positive channel m
PCS[Index]_HDOUTPm	O	High-speed output, positive channel m
PCS[Index]_REFCLKP	I	Positive Reference Clock Input
PCS[Index]_VCCOBm	—	Output buffer power supply, channel m (1.2V/1.5)
PCS[Index]_VCCIBm	—	Input buffer power supply, channel m (1.2V/1.5V)

1. When placing switching I/Os around these critical pins that are designed to supply the device with the proper reference or supply voltage, care must be given.
2. These pins are dedicated inputs or can be used as general purpose I/O.
3. m defines the associated channel in the quad.

LA-LatticeECP3 Devices, Green and Lead-Free Packaging

The following devices may have associated errata. Specific devices with associated errata will be notated with a footnote.

Part Number	Voltage	Grade	Package	Pins	Temp.	LUT (Ks)
LAE3-17EA-6FTN256E	1.2	6	Lead-Free ftBGA	256	Auto	17
LAE3-17EA-6LFTN256E	1.2	6L	Lead-Free ftBGA	256	Auto	17
LAE3-17EA-6MG328E	1.2	6	Green csBGA	328	Auto	17
LAE3-17EA-6LMG328E	1.2	6L	Green csBGA	328	Auto	17
LAE3-17EA-6FN484E	1.2	6	Lead-Free fpBGA	484	Auto	17
LAE3-17EA-6LFN484E	1.2	6L	Lead-Free fpBGA	484	Auto	17
LAE3-35EA-6LFTN256E	1.2	6L	Lead-Free ftBGA	256	Auto	35
LAE3-35EA-6FN484E	1.2	6	Lead-Free fpBGA	484	Auto	35
LAE3-35EA-6LFN484E	1.2	6L	Lead-Free fpBGA	484	Auto	35
LAE3-35EA-6FN672E	1.2	6	Lead-Free fpBGA	672	Auto	35
LAE3-35EA-6LFN672E	1.2	6L	Lead-Free fpBGA	672	Auto	35

For Further Information

A variety of technical notes for the LatticeECP3 family are available on the Lattice website.

- TN1169, LatticeECP3 sysCONFIG Usage Guide
- TN1176, LatticeECP3 SERDES/PCS Usage Guide
- TN1177, LatticeECP3 sysIO Usage Guide
- TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide
- TN1179, LatticeECP3 Memory Usage Guide
- TN1180, LatticeECP3 High-Speed I/O Interface
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- TN1182, LatticeECP3 sysDSP Usage Guide
- TN1184, LatticeECP3 Soft Error Detection (SED) Usage Guide
- TN1189, LatticeECP3 Hardware Checklist

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com