Lattice Semiconductor Corporation - LAE3-17EA-6FTN256E Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

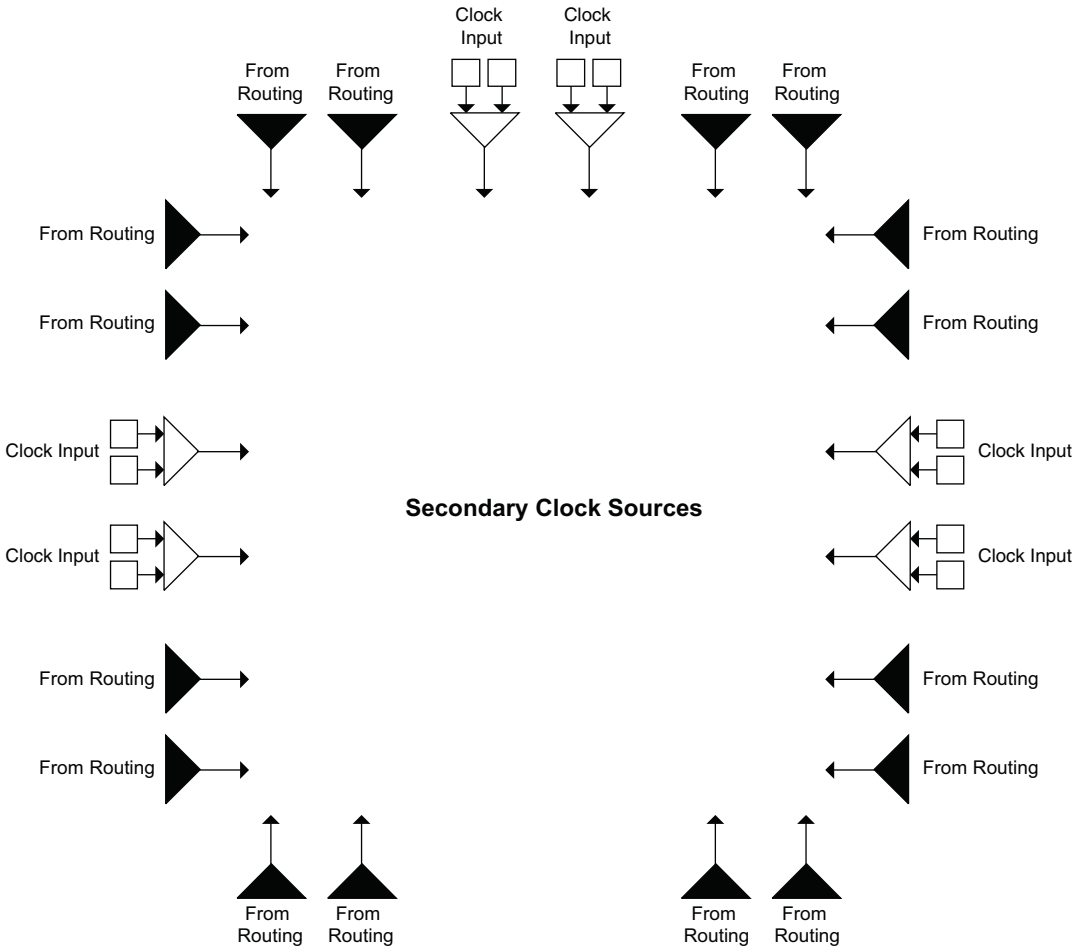
Details	
Product Status	Active
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	716800
Number of I/O	133
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lae3-17ea-6ftn256e

Secondary Clock/Control Sources

LA-LatticeECP3 devices derive eight secondary clock sources (SC0 through SC7) from six dedicated clock input pads and the rest from routing. Figure 2-13 shows the secondary clock sources. All eight secondary clock sources are defined as inputs to a per-region mux SC0-SC7. SC0-SC3 are primary for control signals (CE and/or LSR), and SC4-SC7 are for the clock.

In an actual implementation, there is some overlap to maximize routability. In addition to SC0-SC3, SC7 is also an input to the control signals (LSR or CE). SC0-SC2 are also inputs to clocks along with SC4-SC7.

Figure 2-13. Secondary Clock Sources

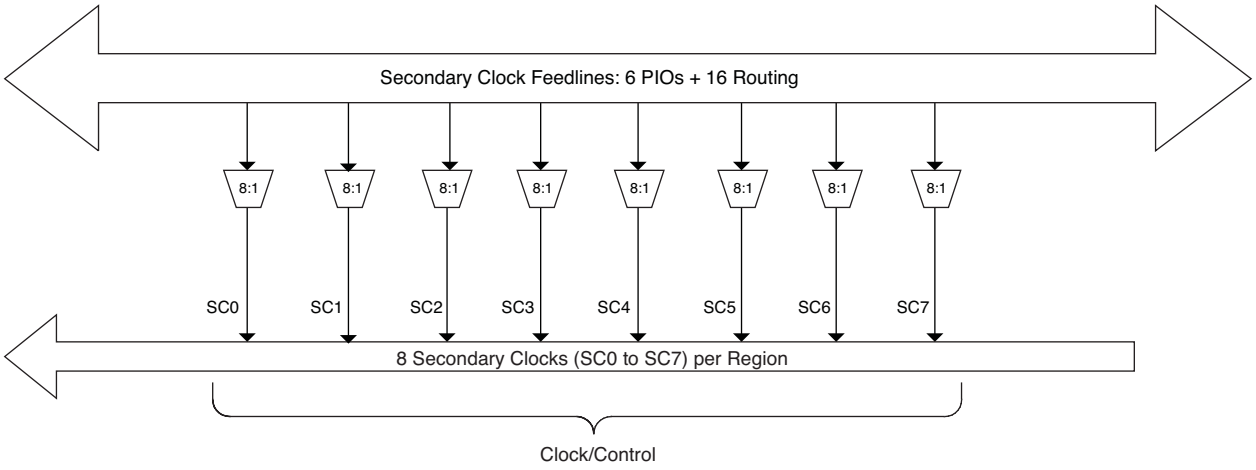


Note: Clock inputs can be configured in differential or single-ended mode.

Secondary Clock/Control Routing

Global secondary clock is a secondary clock that is distributed to all regions. The purpose of the secondary clock routing is to distribute the secondary clock sources to the secondary clock regions. Secondary clocks in the LA-LatticeECP3 devices are region-based resources. Certain EBR rows and special vertical routing channels bind the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP slice in the DSP row or the center of the DSP row. Figure 2-14 shows this special vertical routing channel and the 20 secondary clock regions for the LA-LatticeECP3 family of devices. All devices in the LA-LatticeECP3 family have eight secondary clock resources per region (SC0 to SC7). The same secondary clock routing can be used for control signals.

Figure 2-15. Per Region Secondary Clock Selection



Slice Clock Selection

Figure 2-16 shows the clock selections and Figure 2-17 shows the control selections for Slice0 through Slice2. All the primary clocks and seven secondary clocks are routed to this clock selection mux. Other signals can be used as a clock input to the slices via routing. Slice controls are generated from the secondary clocks/controls or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-16. Slice0 through Slice2 Clock Selection

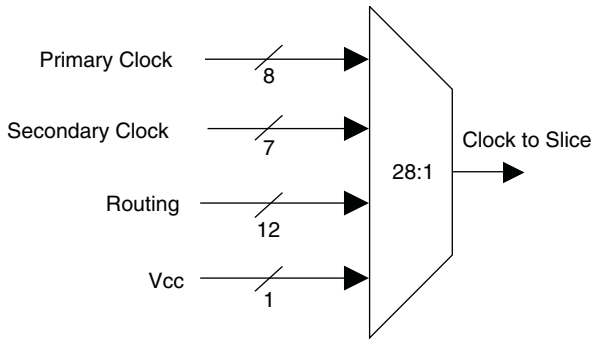
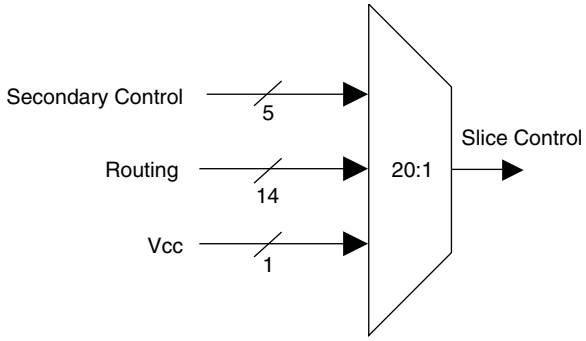


Figure 2-17. Slice0 through Slice2 Control Selection



Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

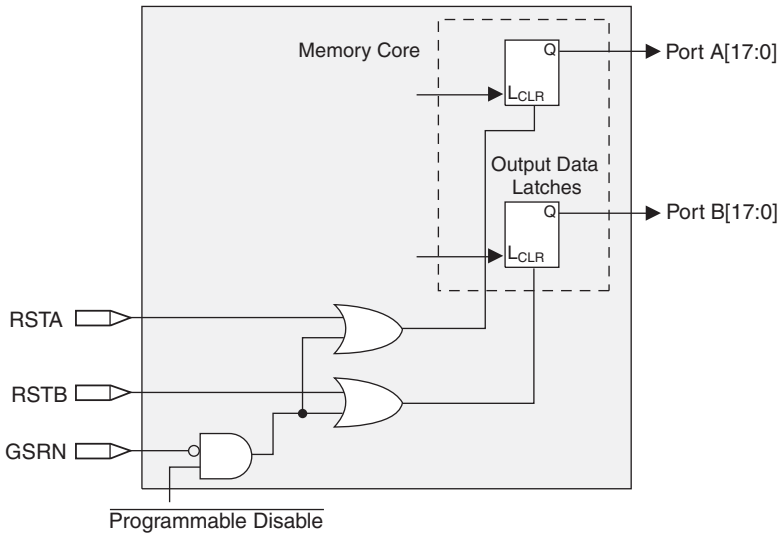
EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-21.

Figure 2-21. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

sysDSP™ Slice

The LA-LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LA-LatticeECP3, on the other hand, has many DSP slices that support different data

MMAC DSP Element

The LA-LatticeECP3 supports a MAC with two multipliers. This is called Multiply Multiply Accumulate or MMAC. In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value and with the result of the multiplier operation of operands BA and BB. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-27 shows the MMAC sysDSP element.

Figure 2-27. MMAC sysDSP Element

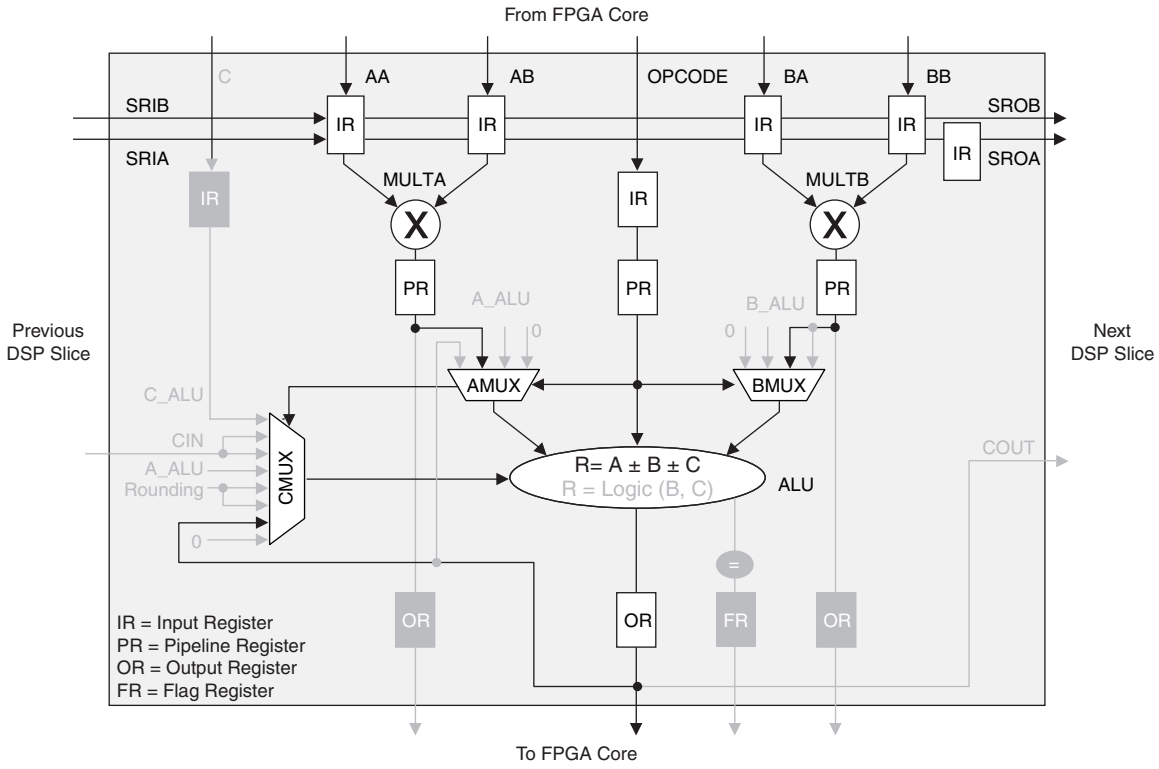
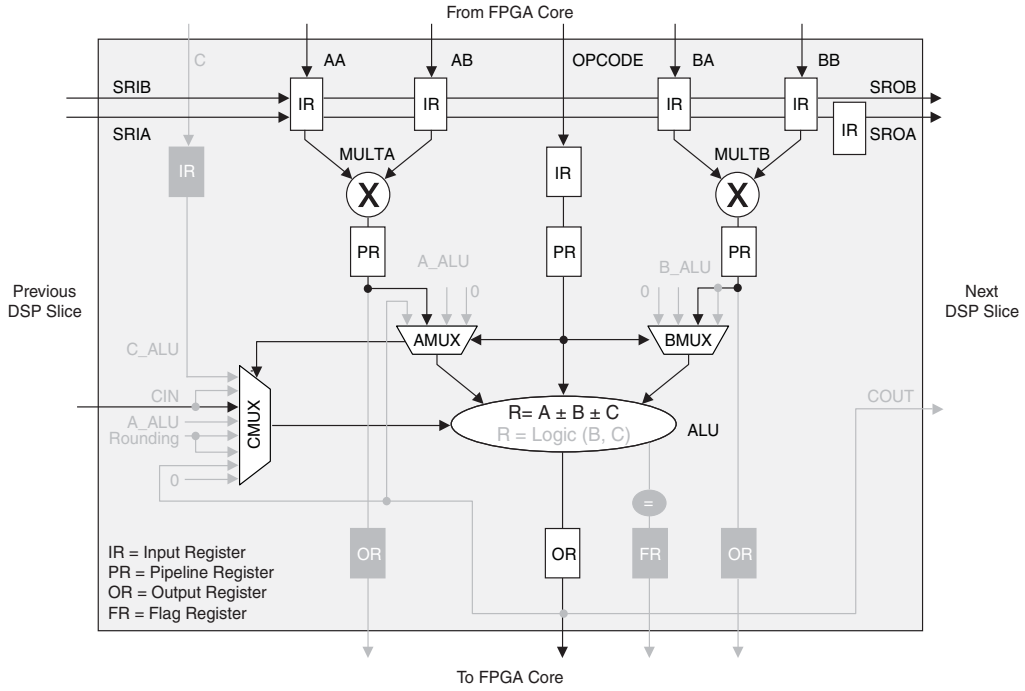


Figure 2-30. MULTADDSUBSUM Slice 1



Advanced sysDSP Slice Features

Cascading

The LA-LatticeECP3 sysDSP slice has been enhanced to allow cascading. Adder trees are implemented fully in sysDSP slices, improving the performance. Cascading of slices uses the signals CIN, COUT and C Mux of the slice.

Addition

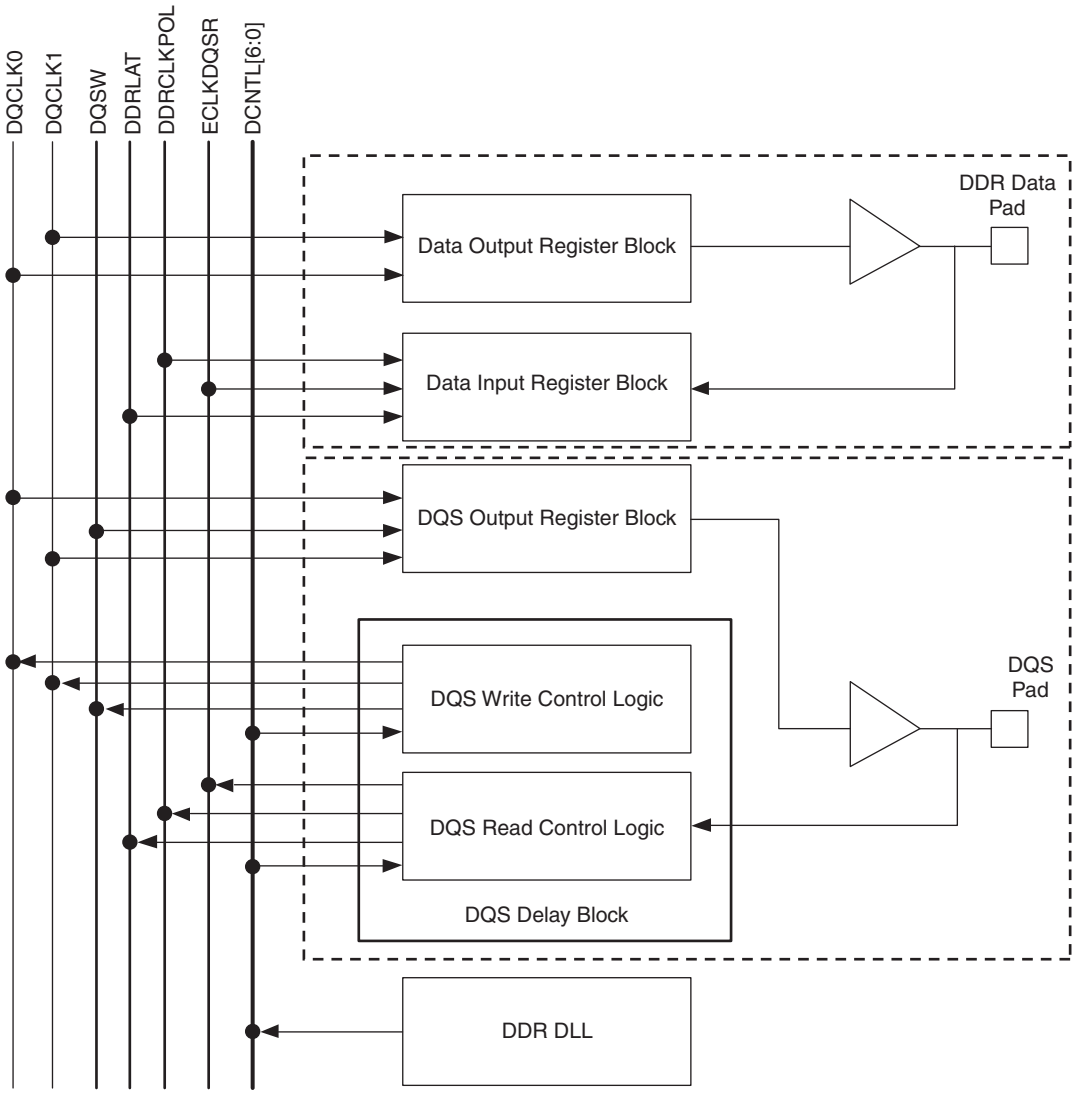
The LA-LatticeECP3 sysDSP slice allows for the bypassing of multipliers and cascading of adder logic. High performance adder functions are implemented without the use of LUTs. The maximum width adders that can be implemented are 54-bit.

Rounding

The rounding operation is implemented in the ALU and is done by adding a constant followed by a truncation operation. The rounding methods supported are:

- Rounding to zero (RTZ)
- Rounding to infinity (RTI)
- Dynamic rounding
- Random rounding
- Convergent rounding

Figure 2-36. DQS Local Bus



Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LA-LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

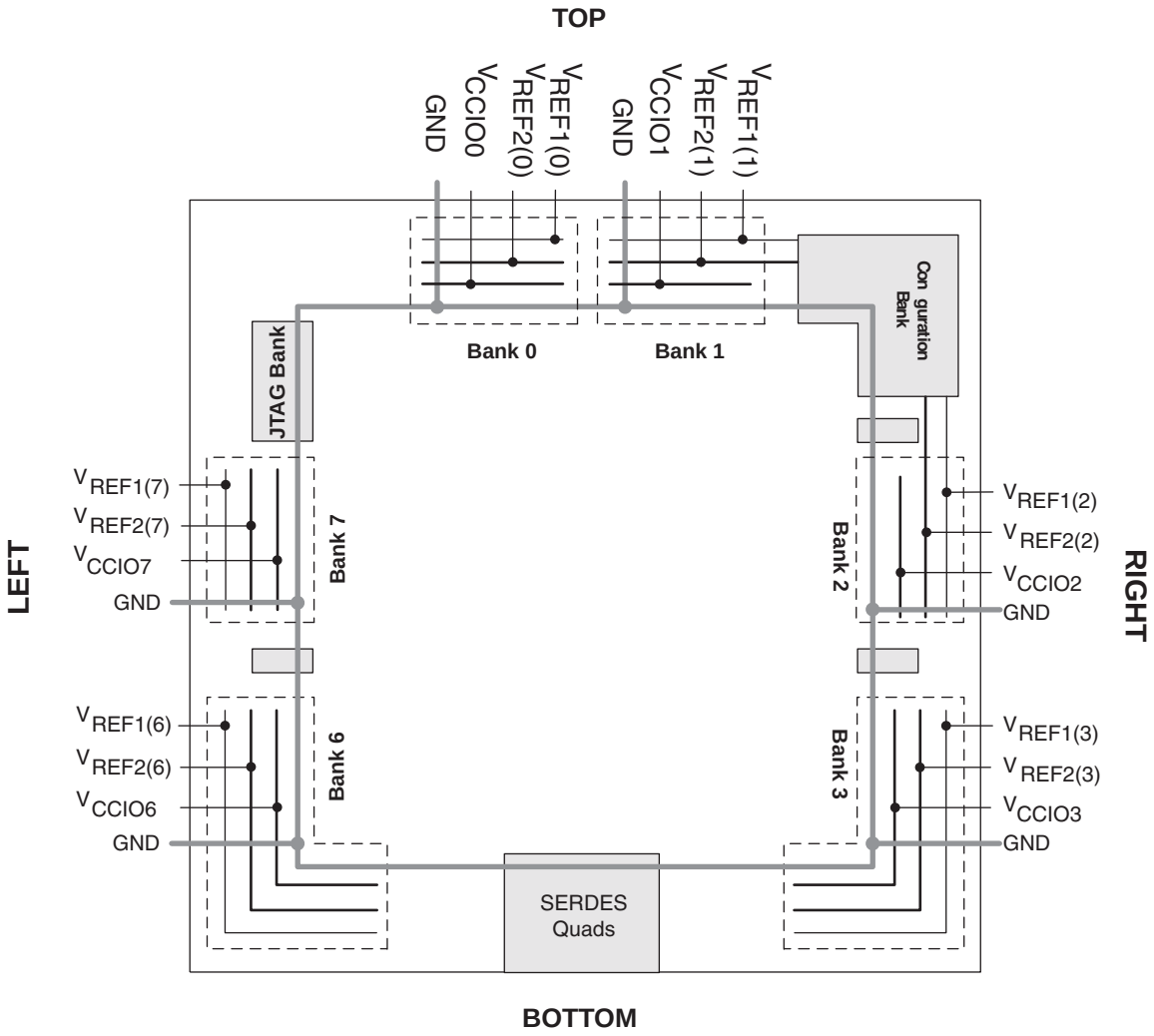
Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

DDR3 Memory Support

LA-LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.

Figure 2-37. LA-LatticeECP3 Banks



LA-LatticeECP3 devices contain two types of sysI/O buffer pairs.

1. **Top (Bank 0 and Bank 1) and Bottom sysIO Buffer Pairs (Single-Ended Outputs Only)**
   The sysI/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input. Only the top edge buffers have a programmable PCI clamp.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   The top and bottom sides are ideal for general purpose I/O, PCI, and inputs for LVDS (LVDS outputs are only allowed on the left and right sides). The top side can be used for the DDR3 ADDR/CMD signals.

   The I/O pins located on the top and bottom sides of the device (labeled PTxxA/B or PBxxA/B) are fully hot socketable. Note that the pads in Banks 3, 6 and 8 are wrapped around the corner of the device. In these banks, only the pads located on the top or bottom of the device are hot socketable. The top and bottom side pads can be identified by the Lattice Diamond tool.

2. **Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**
   The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   In addition, programmable on-chip input termination (parallel or differential, static or dynamic) is supported on these sides, which is required for DDR3 interface. However, there is no support for hot-socketing for the I/O pins located on the left and right side of the device as the PCI clamp is always enabled on these pins.

   LVDS, RSDS, PPLVDS and Mini-LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

3. **Configuration Bank sysI/O Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)**
   The sysI/O buffers in the Configuration Bank consist of ratioed single-ended output drivers and single-ended input buffers. This bank does not support PCI clamp like the other banks on the top, left, and right sides.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Programmable PCI clamps are only available on the top banks. PCI clamps are used primarily on inputs and bi-directional pads to reduce ringing on the receiving end.

Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in LA-LatticeECP3 devices, see the list of technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported sysI/O Standards

The LA-LatticeECP3 sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, slew rates, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, MLVDS, RSDS, Mini-LVDS, PPLVDS (point-to-point LVDS), TRLVDS (Transition Reduced LVDS), differential SSTL and differential HSTL. For further information on utilizing the sysI/O buffer to support a variety of standards please see TN1177, LatticeECP3 sysIO Usage Guide.

sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS18	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS15	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS12	-0.3	0.35 V_{CC}	0.65 V_{CC}	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL33	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI33	-0.3	0.3 V_{CCIO}	0.5 V_{CCIO}	3.6	0.1 V_{CCIO}	0.9 V_{CCIO}	1.5	-0.5
SSTL18_I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
SSTL18_II (DDR2 Memory)	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.28	V_{CCIO} - 0.28	8	-8
							11	-11
SSTL2_I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
							12	-12
SSTL2_II (DDR Memory)	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
							20	-20
SSTL3_I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3_II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL15 (DDR3 Memory)	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.3	V_{CCIO} - 0.3	7.5	-7.5
						V_{CCIO} * 0.8	9	-9
HSTL15_I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	4	-4
							8	-8
HSTL18_I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
							12	-12
HSTL18_II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16

1. For electromigration, the average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA, where n is the number of I/Os between bank GND connections or between the last VCCIO and GND in a bank and the end of a bank.

MLVDS25

The LA-LatticeECP3 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

Figure 3-5. MLVDS25 (Multipoint Low Voltage Differential Signaling)

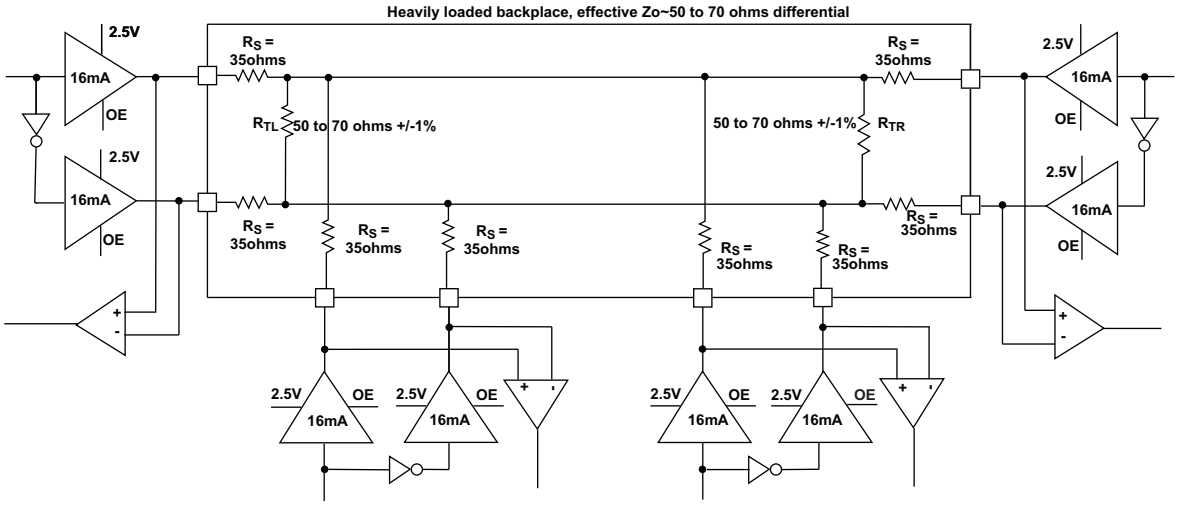


Table 3-7. MLVDS25 DC Conditions[1]

Parameter	Description	Typical		Units
		Zo=50Ω	Zo=70Ω	
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R_{TL}	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R_{TR}	Receiver Termination (+/-1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage	1.52	1.60	V
V_{OL}	Output Low Voltage	0.98	0.90	V
V_{OD}	Output Differential Voltage	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tool are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

LA-LatticeECP3 External Switching Characteristics[1, 2]

Over Recommended Operating Ranges

Parameter	Description	Device	-6 / -6L		Units
			Min.	Max.	
Clocks					
Primary Clock [6]					
f_{MAX_PRI}	Frequency for Primary Clock Tree	LAE3-35EA	—	375	MHz
t_{W_PRI}	Pulse Width for Primary Clock	LAE3-35EA	1	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	LAE3-35EA	—	360	ps
t_{SKEW_PRIB}	Primary Clock Skew Within a Bank	LAE3-35EA	—	300	ps
f_{MAX_PRI}	Frequency for Primary Clock Tree	LAE3-17EA	—	375	MHz
t_{W_PRI}	Pulse Width for Primary Clock	LAE3-17EA	1	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	LAE3-17EA	—	370	ps
t_{SKEW_PRIB}	Primary Clock Skew Within a Bank	LAE3-17EA	—	240	ps
Edge Clock [6]					
f_{MAX_EDGE}	Frequency for Edge Clock	LAE3-35EA	—	375	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	LAE3-35EA	1.2	—	ns
$t_{SKEW\_EDGE\_DQS}$	Edge Clock Skew Within an Edge of the Device	LAE3-35EA	—	220	ps
f_{MAX_EDGE}	Frequency for Edge Clock	LAE3-17EA	—	375	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	LAE3-17EA	1.2	—	ns
$t_{SKEW\_EDGE\_DQS}$	Edge Clock Skew Within an Edge of the Device	LAE3-17EA	—	220	ps
Generic SDR					
General I/O Pin Parameters (using dedicated clock input Primary Clock without PLL) [2]					
t_{CO}	Clock to Output - PIO Output Register	LAE3-35EA	-	4.54	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LAE3-35EA	0.00	-	ns
t_{H}	Clock to Data Hold - PIO Input Register	LAE3-35EA	1.62	-	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LAE3-35EA	1.48	-	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LAE3-35EA	0.00	-	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LAE3-35EA	-	375	Mhz
t_{CO}	Clock to Output - PIO Output Register	LAE3-17EA	-	4.34	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LAE3-17EA	0.00	-	ns
t_{H}	Clock to Data Hold - PIO Input Register	LAE3-17EA	1.62	-	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LAE3-17EA	1.48	-	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LAE3-17EA	0.00	-	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LAE3-17EA	-	375	Mhz

Parameter	Description	Device	-6 / -6L		Units
			Min.	Max.	
GenericDDRX2 Inputs with Clock and Data (>10bits wide) are Aligned at Pin (GDDRX2_RX.ECLK.Aligned) (No CLKDIV)					
Left and Right Sides Using DLLCLKPIN for Clock Input					
$t_{DVACLKGDDR}$	Data Setup Before CLK	LAE3-35EA	-	0.21	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	LAE3-35EA	0.79	-	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-35EA	-	311	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK (Left and Right Sides)	LAE3-17EA	-	0.21	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	LAE3-17EA	0.79	-	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-17EA	-	311	MHz
Top Side Using PCLK Pin for Clock Input					
$t_{DVACLKGDDR}$	Data Setup Before CLK	LAE3-35EA	-	0.21	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	LAE3-35EA	0.79	-	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-35EA	-	130	MHz
$t_{DVACLKGDDR}$	Data Setup Before CLK	LAE3-17EA	-	0.21	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	LAE3-17EA	0.79	-	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	LAE3-17EA	-	130	MHz
GenericDDRX2 Inputs with Clock and Data (<10 Bits Wide) Centered at Pin (GDDRX2_RX.DQS.Centered) Using DQS Pin for Clock Input					
Left and Right Sides					
t_{SUGDDR}	Data Setup Before CLK	All Devices	352	-	ps
t_{HOGDDR}	Data Hold After CLK	All Devices	352	-	ps
f_{MAX_GDDR}	DDRX2 Clock Frequency	All Devices	-	375	MHz
GenericDDRX2 Inputs with Clock and Data (<10 Bits Wide) Aligned at Pin (GDDRX2_RX.DQS.Aligned) Using DQS Pin for Clock Input					
Left and Right Sides					
$t_{DVACLKGDDR}$	Data Setup Before CLK	All Devices	-	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	All Devices	0.775 -	-	UI
f_{MAX_GDDR}	DDRX2 Clock Frequency	All Devices	-	375	MHz
GenericDDRX1 Output with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_TX.SCLK.Centered)10					
$t_{DVBGDDR}$	Data Valid Before CLK	LAE3-35EA	690	-	ps
$t_{DVAGDDR}$	Data Valid After CLK	LAE3-35EA	690	-	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	LAE3-35EA	-	250	MHz
$t_{DVBGDDR}$	Data Valid Before CLK	LAE3-17EA	690	-	ps
$t_{DVAGDDR}$	Data Valid After CLK	LAE3-17EA	690	-	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	LAE3-17EA	-	250	MHz

LA-LatticeECP3 Internal Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	-6 / -6L		Units
		Min.	Max.	
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.080	-	ns
PLL Parameters				
t_{RSTREC_GPLL}	Reset Recovery to Rising Clock	1.00	—	ns
DSP Block Timing[2, 3]				
t_{SUI_DSP}	Input Register Setup Time	0.39	—	ns
t_{HI_DSP}	Input Register Hold Time	-0.21	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	2.39	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	-1.16	—	ns
t_{SUO_DSP}	Output Register Setup Time	3.37	—	ns
t_{HO_DSP}	Output Register Hold Time	-1.86	—	ns
t_{COI_DSP}	Input Register Clock to Output Time	—	3.77	ns
t_{COP_DSP}	Pipeline Register Clock to Output Time	—	1.66	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	0.63	ns
t_{SUOPT_DSP}	Opcode Register Setup Time	0.39	—	ns
t_{HOPT_DSP}	Opcode Register Hold Time	-0.27	—	ns
t_{SUDATA_DSP}	Cascade_data through ALU to Output Register Setup Time	2.16	—	ns
t_{HPDATA_DSP}	Cascade_data through ALU to Output Register Hold Time	-0.98	—	ns

1. Internal parameters are characterized but not tested on every device.
2. These parameters apply to LA-LatticeECP3 devices only.
3. DSP Block is configured in Multiply Add/Sub 18x18 Mode.

SERDES/PCS Block Latency

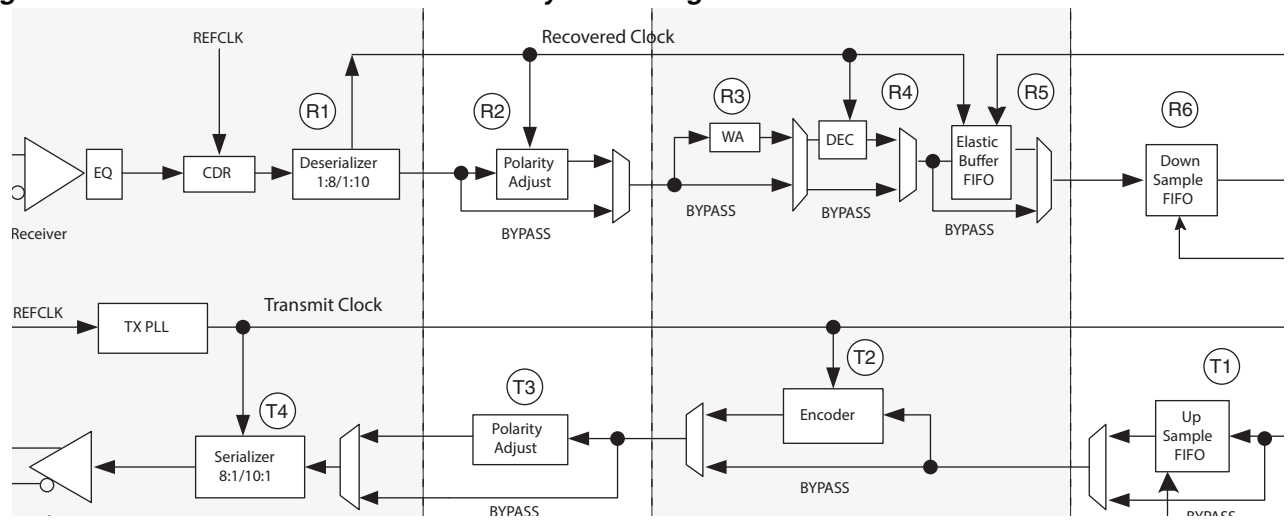
Table 3-10 describes the latency of each functional block in the transmitter and receiver. Latency is given in parallel clock cycles. Figure 3-12 shows the location of each block.

Table 3-10. SERDES/PCS Latency Breakdown

Item	Description	Min.	Avg.	Max.	Fixed	Bypass	Units
Transmit Data Latency[1]							
T1	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk
T2	8b10b Encoder	—	—	—	2	1	word clk
T3	SERDES Bridge transmit	—	—	—	2	1	word clk
T4	Serializer: 8-bit mode	—	—	—	15 + Δ1	—	UI + ps
	Serializer: 10-bit mode	—	—	—	18 + Δ1	—	UI + ps
T5	Pre-emphasis ON	—	—	—	1 + Δ2	—	UI + ps
	Pre-emphasis OFF	—	—	—	0 + Δ3	—	UI + ps
Receive Data Latency[2]							
R1	Equalization ON	—	—	—	Δ1	—	UI + ps
	Equalization OFF	—	—	—	Δ2	—	UI + ps
R2	Deserializer: 8-bit mode	—	—	—	10 + Δ3	—	UI + ps
	Deserializer: 10-bit mode	—	—	—	12 + Δ3	—	UI + ps
R3	SERDES Bridge receive	—	—	—	2	—	word clk
R4	Word alignment	3.1	—	4	—	—	word clk
R5	8b10b decoder	—	—	—	1	—	word clk
R6	Clock Tolerance Compensation	7	15	23	1	1	word clk
R7	FPGA Bridge - Gearing disabled with different clocks	1	3	5	—	1	word clk
	FPGA Bridge - Gearing disabled with same clocks	—	—	—	3	1	word clk
	FPGA Bridge - Gearing enabled	1	3	5	—	—	word clk

1. Δ1 = -245ps, Δ2 = +88ps, Δ3 = +112ps.
2. Δ1 = +118ps, Δ2 = +132ps, Δ3 = +700ps.

Figure 3-12. Transmitter and Receiver Latency Block Diagram



SERDES High Speed Data Receiver

Table 3-11. Serial Input Data Specifications

Symbol	Description		Min.	Typ.	Max.	Units
$RX\text{-}CID_S$	Stream of nontransitions[1] (CID = Consecutive Identical Digits) @ 10^{-12} BER	3.125G	—	—	136	Bits
		2.5G	—	—	144	
		1.485G	—	—	160	
		622M	—	—	204	
		270M	—	—	228	
		150M	—	—	296	
$V_{RX\text{-}DIFF\text{-}S}$	Differential input sensitivity		150	—	1760	mV, p-p
$V_{RX\text{-}IN}$	Input levels		0	—	V_{CCA} +0.5[4]	V
$V_{RX\text{-}CM\text{-}DC}$	Input common mode range (DC coupled)		0.6	—	V_{CCA}	V
$V_{RX\text{-}CM\text{-}AC}$	Input common mode range (AC coupled)[3]		0.1	—	V_{CCA} +0.2	V
$T_{RX\text{-}RELOCK}$	SCDR re-lock time[2]		—	1000	—	Bits
$Z_{RX\text{-}TERM}$	Input termination 50/75 Ohm/High Z		-20%	50/75/HiZ	+20%	Ohms
$RL_{RX\text{-}RL}$	Return loss (without package)		10	—	—	dB

1. This is the number of bits allowed without a transition on the incoming data stream when using DC coupling.
2. This is the typical number of bit times to re-lock to a new phase or frequency within +/- 300 ppm, assuming 8b10b encoded data.
3. AC coupling is used to interface to LVPECL and LVDS. LVDS interfaces are found in laser drivers and Fibre Channel equipment. LVDS interfaces are generally found in 622 Mbps SERDES devices.
4. Up to 1.76V.

Input Data Jitter Tolerance

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High speed serial interface standards have recognized the dependency on jitter type and have specifications to indicate tolerance levels for different jitter types as they relate to specific protocols. Sinusoidal jitter is considered to be a worst case jitter type.

Table 3-12. Receiver Total Jitter Tolerance Specification

Description	Frequency	Condition	Min.	Typ.	Max.	Units
Deterministic	3.125 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	2.5 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	1.25 Gbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p
Deterministic	622 Mbps	600 mV differential eye	—	—	0.47	UI, p-p
Random		600 mV differential eye	—	—	0.18	UI, p-p
Total		600 mV differential eye	—	—	0.65	UI, p-p

Note: Values are measured with CJPAT, all channels operating, FPGA Logic active, I/Os around SERDES pins quiet, voltages are nominal, room temperature.

XAUI/Serial Rapid I/O Type 3/CPRI LV E.30 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-15. Transmit

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance		80	100	120	Ohms
J_{TX_DDJ}[2, 3, 4]	Output data deterministic jitter		—	—	0.17	UI
J_{TX_TJ}[1, 2, 3, 4]	Total output data jitter		—	—	0.35	UI

1. Total jitter includes both deterministic jitter and random jitter.
2. Jitter values are measured with each CML output AC coupled into a 50-ohm impedance (100-ohm differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Values are measured at 2.5 Gbps.

Table 3-16. Receive and Jitter Tolerance

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 3.125 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 3.125 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J_{RX_DJ}[1, 2, 3]	Deterministic jitter tolerance (peak-to-peak)		—	—	0.37	UI
J_{RX_RJ}[1, 2, 3]	Random jitter tolerance (peak-to-peak)		—	—	0.18	UI
J_{RX_SJ}[1, 2, 3]	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.10	UI
J_{RX_TJ}[1, 2, 3]	Total jitter tolerance (peak-to-peak)		—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

Serial Rapid I/O Type 2/CPRI LV E.24 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-17. Transmit

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}[1]	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance		80	100	120	Ohms
J_{TX_DDJ}[3, 4, 5]	Output data deterministic jitter		—	—	0.17	UI
J_{TX_TJ}[2, 3, 4, 5]	Total output data jitter		—	—	0.35	UI

1. Rise and Fall times measured with board trace, connector and approximately 2.5pf load.
2. Total jitter includes both deterministic jitter and random jitter. The random jitter is the total jitter minus the actual deterministic jitter.
3. Jitter values are measured with each CML output AC coupled into a 50-ohm impedance (100-ohm differential impedance).
4. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
5. Values are measured at 2.5 Gbps.

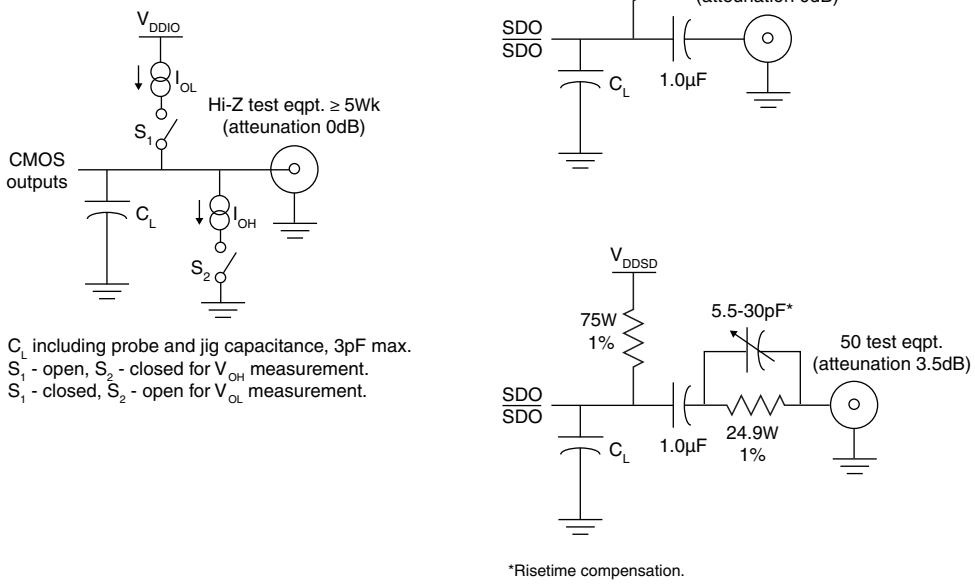
Table 3-18. Receive and Jitter Tolerance

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 2.5 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 2.5 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J_{RX_DJ}[2, 3, 4, 5]	Deterministic jitter tolerance (peak-to-peak)		—	—	0.37	UI
J_{RX_RJ}[2, 3, 4, 5]	Random jitter tolerance (peak-to-peak)		—	—	0.18	UI
J_{RX_SJ}[2, 3, 4, 5]	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.10	UI
J_{RX_TJ}[1, 2, 3, 4, 5]	Total jitter tolerance (peak-to-peak)		—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance, Differential Input Sensitivity and Receiver Eye Opening parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

Figure 3-19. Test Loads

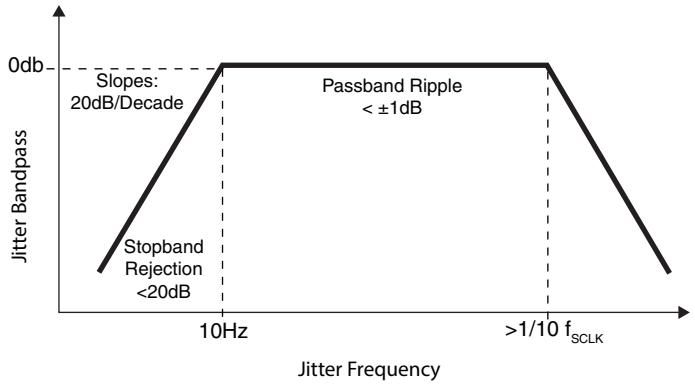
Test Loads



C_L including probe and jig capacitance, 3pF max.
S_1 - open, S_2 - closed for V_{OH} measurement.
S_1 - closed, S_2 - open for V_{OL} measurement.

*Risetime compensation.

Timing Jitter Bandpass



LA-LatticeECP3 sysCONFIG Port Timing Specifications (Continued)

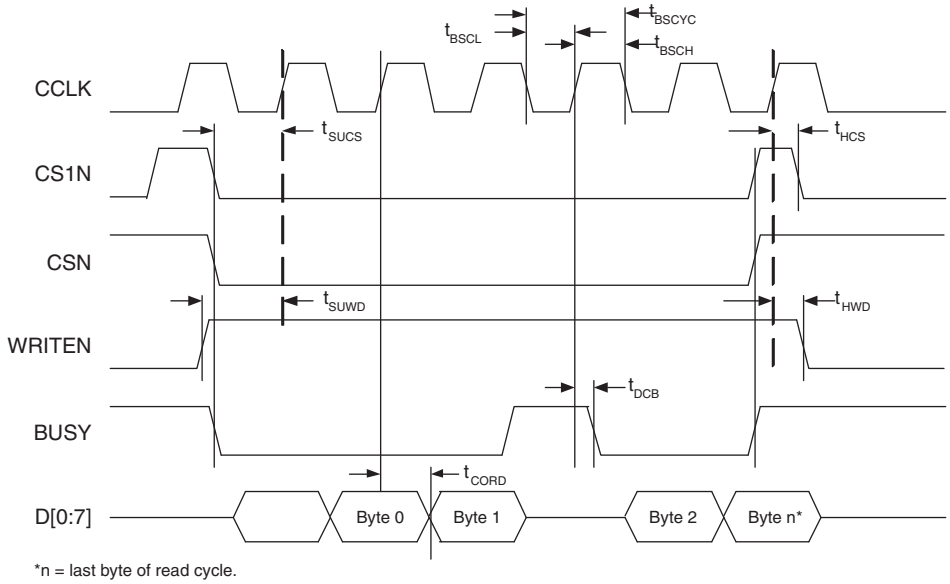
Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
t_{CHHH}	HOLDN Low Hold Time (Relative to CCLK)	5	—	ns
Master and Slave SPI (Continued)				
t_{CHHL}	HOLDN High Hold Time (Relative to CCLK)	5	—	ns
t_{HHCH}	HOLDN High Setup Time (Relative to CCLK)	5	—	ns
t_{HLQZ}	HOLDN to Output High-Z	—	9	ns
t_{HHQX}	HOLDN to Output Low-Z	—	9	ns

1. Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of the PROGRAMN.

Parameter	Min.	Max.	Units
Master Clock Frequency	Selected value - 15%	Selected value + 15%	MHz
Duty Cycle	40	60	%

Figure 3-20. sysCONFIG Parallel Port Read Cycle



*n = last byte of read cycle.