Lattice Semiconductor Corporation - LAE3-17EA-6LFTN256E Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	716800
Number of I/O	133
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lae3-17ea-6lftn256e

Figure 2-4. General Purpose PLL Diagram

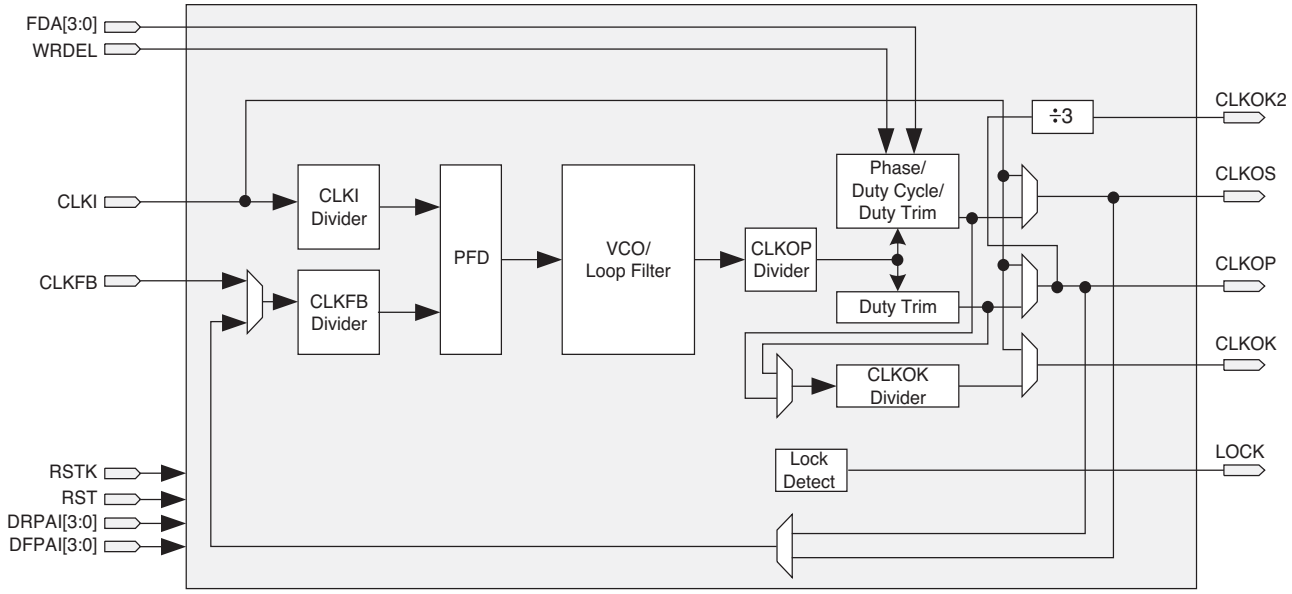


Table 2-4 provides a description of the signals in the PLL blocks.

Table 2-4. PLL Blocks Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP, CLKOS, or from a user clock (pin or logic)
RST	I	“1” to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	“1” to reset K-divider
WRDEL	I	DPA Fine Delay Adjust input
CLKOS	O	PLL output to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
CLKOK2	O	PLL output to clock tree (CLKOP divided by 3)
LOCK	O	“1” indicates PLL LOCK to CLKI
FDA [3:0]	I	Dynamic fine delay adjustment on CLKOS output
DRPAI[3:0]	I	Dynamic coarse phase shift, rising edge setting
DFPAI[3:0]	I	Dynamic coarse phase shift, falling edge setting

Delay Locked Loops (DLL)

In addition to PLLs, the LA-LatticeECP3 family of devices has two DLLs per device.

CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Detector (PD) input mux. The reference signal for the PD can also be generated from the Delay Chain signals. The feedback input to the PD is generated from the CLKFB pin or from a tapped signal from the Delay chain.

The PD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. Based on these inputs, the ALU determines the correct digital control codes to send to the delay

Table 2-5. DLL Signals

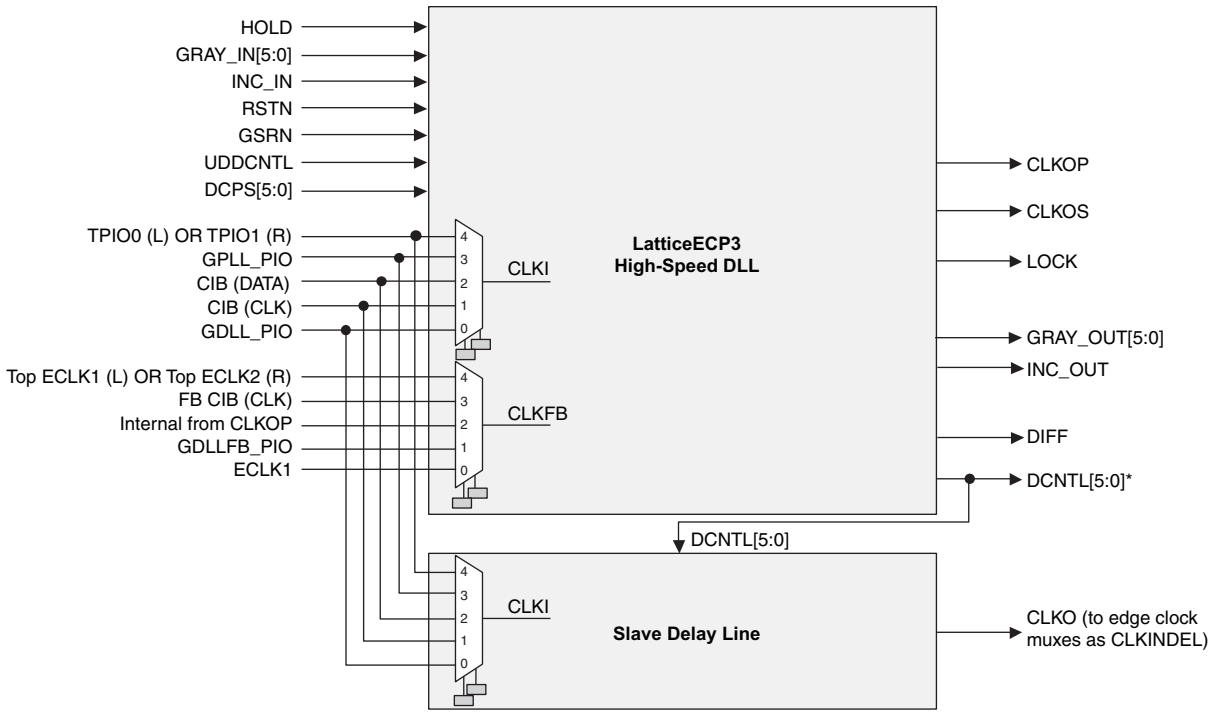
Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine delay shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator
INCI	I	Incremental indicator from another DLL via CIB.
GRAYI[5:0]	I	Gray-coded digital control bus from another DLL in time reference mode.
DIFF	O	Difference indicator when DCNTL is difference than the internal setting and update is needed.
INCO	O	Incremental indicator to other DLLs via CIB.
GRAYO[5:0]	O	Gray-coded digital control bus to other DLLs via CIB

LA-LatticeECP3 devices have two general DLLs and four Slave Delay lines, two per DLL. The DLLs are in the lowest EBR row and located adjacent to the EBR. Each DLL replaces one EBR block. One Slave Delay line is placed adjacent to the DLL and the duplicate Slave Delay line (in Figure 2-6) for the DLL is placed in the I/O ring between Banks 6 and 7 and Banks 2 and 3.

The outputs from the DLL and Slave Delay lines are fed to the clock distribution network.

For more information, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide.

Figure 2-6. Top-Level Block Diagram, High-Speed DLL and Slave Delay Line



* This signal is not user accessible. It can only be used to feed the slave delay line.

PLL/DLL Cascading

LA-LatticeECP3 devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

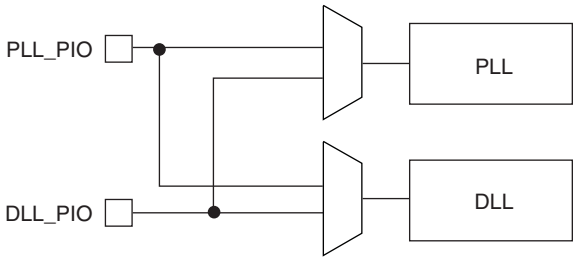
The DLLs in the LA-LatticeECP3 are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of technical documentation at the end of this data sheet.

PLL/DLL PIO Input Pin Connections

All LA-LatticeECP3 devices contains two DLLs and up to ten PLLs, arranged in quadrants. If a PLL and a DLL are next to each other, they share input pins as shown in the Figure 2-7.

Figure 2-7. Sharing of PIO Pins by PLLs and DLLs in LA-LatticeECP3 Devices



Note: Not every PLL has an associated DLL.

Clock Dividers

LA-LatticeECP3 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, the Slave Delay lines, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide. Figure 2-8 shows the clock divider connections.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

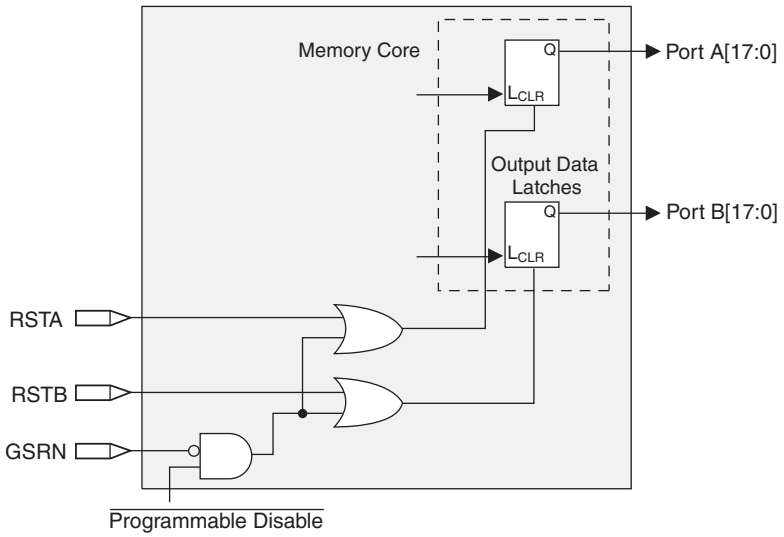
EBR memory supports the following forms of write behavior for single port or dual port operation:

1. **Normal** – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. **Write Through** – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.
3. **Read-Before-Write (EA devices only)** – When new data is written, the old content of the address appears at the output. This mode is supported for x9, x18, and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2-21.

Figure 2-21. Memory Core Reset



For further information on the sysMEM EBR block, please see the list of technical documentation at the end of this data sheet.

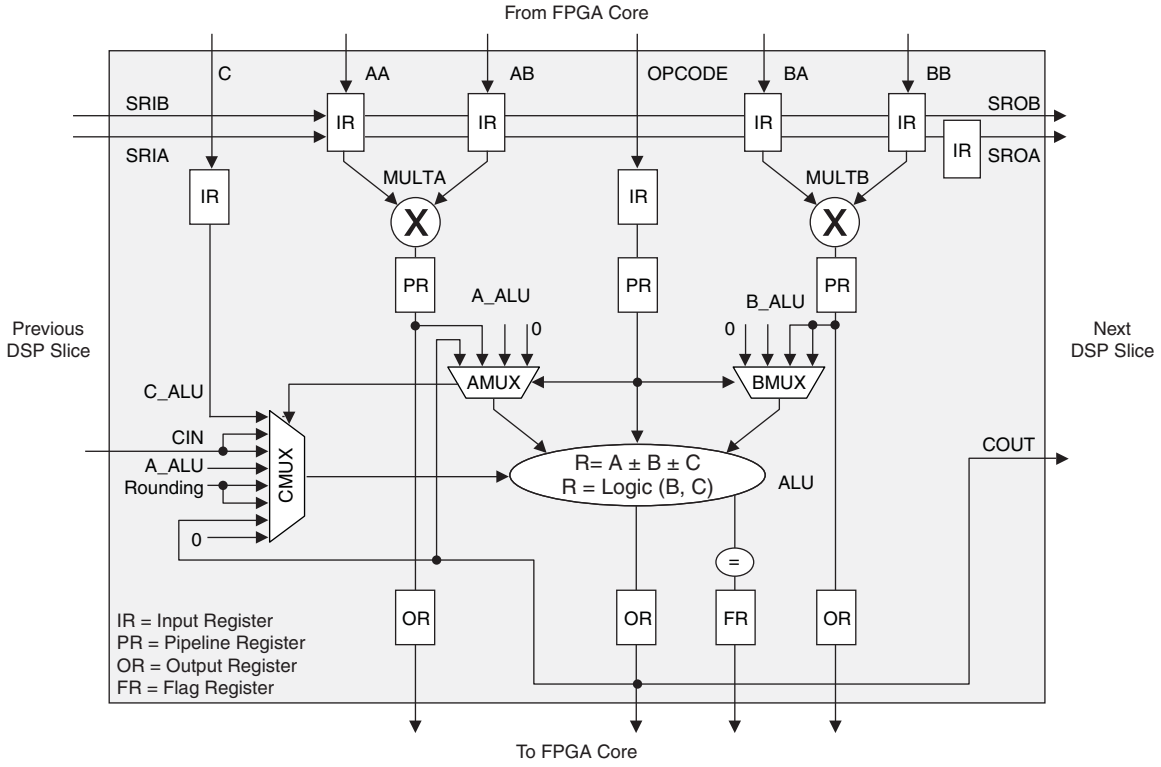
sysDSP™ Slice

The LA-LatticeECP3 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, high-performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LA-LatticeECP3, on the other hand, has many DSP slices that support different data

Figure 2-24. Detailed sysDSP Slice Diagram



Note: A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LA-LatticeECP3 slices versus the above functions.

Table 2-8. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	—
MULTADDSUB	2	1	—
MULTADDSUBSUM	1[1]	1/2	—

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

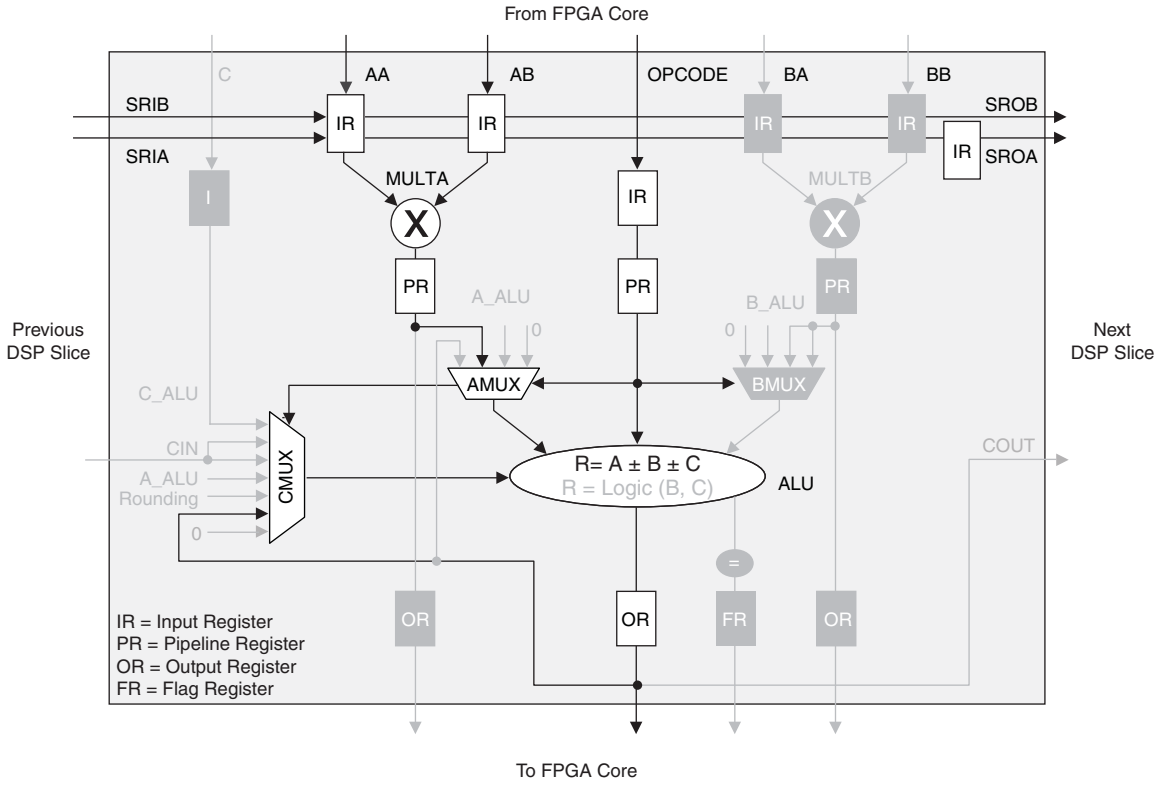
Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting “dynamic operation” the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

MAC DSP Element

In this case, the two operands, AA and AB, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers, but the output register is always enabled. The output register is used to store the accumulated value. The ALU is configured as the accumulator in the sysDSP slice in the LA-LatticeECP3 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-26 shows the MAC sysDSP element.

Figure 2-26. MAC DSP Element



Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In single data rate (SDR) the data is registered with the system clock by one of the registers in the single data rate sync register block.

In DDR mode, two registers are used to sample the data on the positive and negative edges of the modified DQS (ECLKDQSR) in the DDR Memory mode or ECLK signal when using DDR Generic mode, creating two data streams. Before entering the core, these two data streams are synchronized to the system clock to generate two data streams.

A gearbox function can be implemented in each of the input registers on the left and right sides. The gearbox function takes a double data rate signal applied to PIOA and converts it as four data streams, INA, IPA, INB and IPB. The two data streams from the first set of DDR registers are synchronized to the edge clock and then to the system clock before entering the core. Figure 2-29 provides further information on the use of the gearbox function.

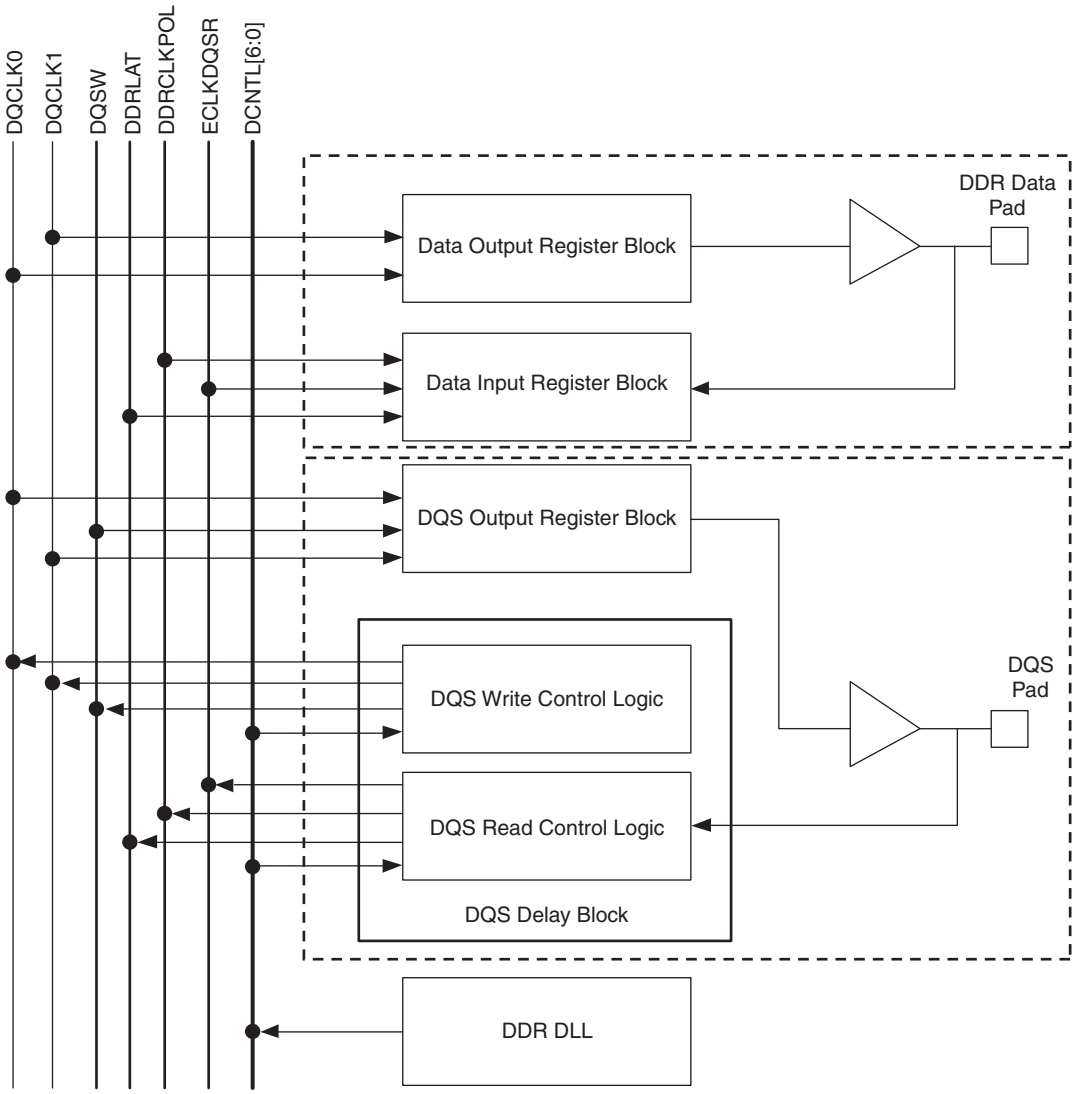
The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred to the system clock domain from the ECLKDQSR (DDR Memory Interface mode) or ECLK (DDR Generic mode). The DDRLAT signal is used to ensure the data transfer from the synchronization registers to the clock transfer and gearbox registers.

The ECLKDQSR, DDRCLKPOL and DDRLAT signals are generated in the DQS Read Control Logic Block. See Figure 2-36 for an overview of the DQS read control logic.

Further discussion about using the DQS strobe in this module is discussed in the DDR Memory section of this data sheet.

Please see TN1180, LatticeECP3 High-Speed I/O Interface for more information on this topic.

Figure 2-36. DQS Local Bus



Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LA-LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

DDR3 Memory Support

LA-LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.

Table 2-14. Available SERDES Quads per LA-LatticeECP3 Devices

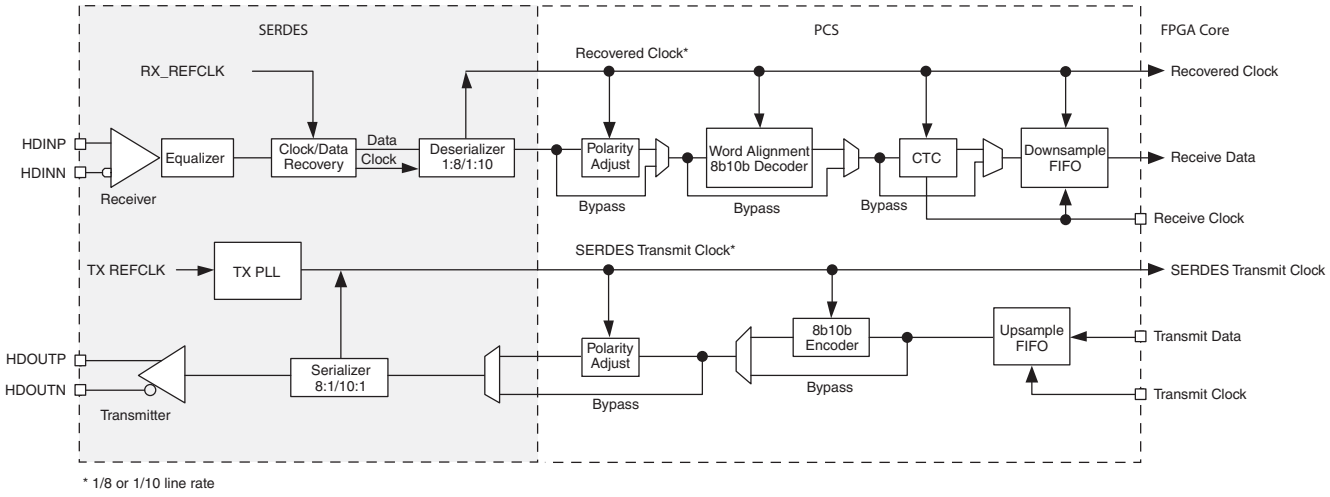
Package	LAE3-17	LAE3-35
256 ftBGA	1	1
328 csBGA	2 channels	—
484 fpBGA	1	1
672 fpBGA	—	1

SERDES Block

A SERDES receiver channel may receive the serial differential data stream, equalize the signal, perform Clock and Data Recovery (CDR) and de-serialize the data stream before passing the 8- or 10-bit data to the PCS logic. The SERDES transmitter channel may receive the parallel 8- or 10-bit data, serialize the data and transmit the serial bit stream through the differential drivers. Figure 2-40 shows a single-channel SERDES/PCS block. Each SERDES channel provides a recovered clock and a SERDES transmit clock to the PCS block and to the FPGA core logic.

Each transmit channel, receiver channel, and SERDES PLL shares the same power supply (VCCA). The output and input buffers of each channel have their own independent power supplies (VCCOB and VCCIB).

Figure 2-40. Simplified Channel Block Diagram for SERDES/PCS Block



PCS

As shown in Figure 2-40, the PCS receives the parallel digital data from the deserializer and selects the polarity, performs word alignment, decodes (8b/10b), provides Clock Tolerance Compensation and transfers the clock domain from the recovered clock to the FPGA clock via the Down Sample FIFO.

For the transmit channel, the PCS block receives the parallel data from the FPGA core, encodes it with 8b/10b, selects the polarity and passes the 8/10 bit data to the transmit SERDES channel.

The PCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic. The PCS interface to the FPGA can also be programmed to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic.

SCI (SERDES Client Interface) Bus

The SERDES Client Interface (SCI) is an IP interface that allows the SERDES/PCS Quad block to be controlled by registers rather than the configuration memory cells. It is a simple register configuration interface that allows SERDES/PCS configuration without power cycling the device.

sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS33	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS18	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS15	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS12	-0.3	0.35 V_{CC}	0.65 V_{CC}	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL33	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI33	-0.3	0.3 V_{CCIO}	0.5 V_{CCIO}	3.6	0.1 V_{CCIO}	0.9 V_{CCIO}	1.5	-0.5
SSTL18_I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
SSTL18_II (DDR2 Memory)	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.28	V_{CCIO} - 0.28	8	-8
							11	-11
SSTL2_I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
							12	-12
SSTL2_II (DDR Memory)	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
							20	-20
SSTL3_I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3_II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL15 (DDR3 Memory)	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.3	V_{CCIO} - 0.3	7.5	-7.5
						V_{CCIO} * 0.8	9	-9
HSTL15_I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	4	-4
							8	-8
HSTL18_I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
							12	-12
HSTL18_II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16

1. For electromigration, the average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA, where n is the number of I/Os between bank GND connections or between the last VCCIO and GND in a bank and the end of a bank.

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tool are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

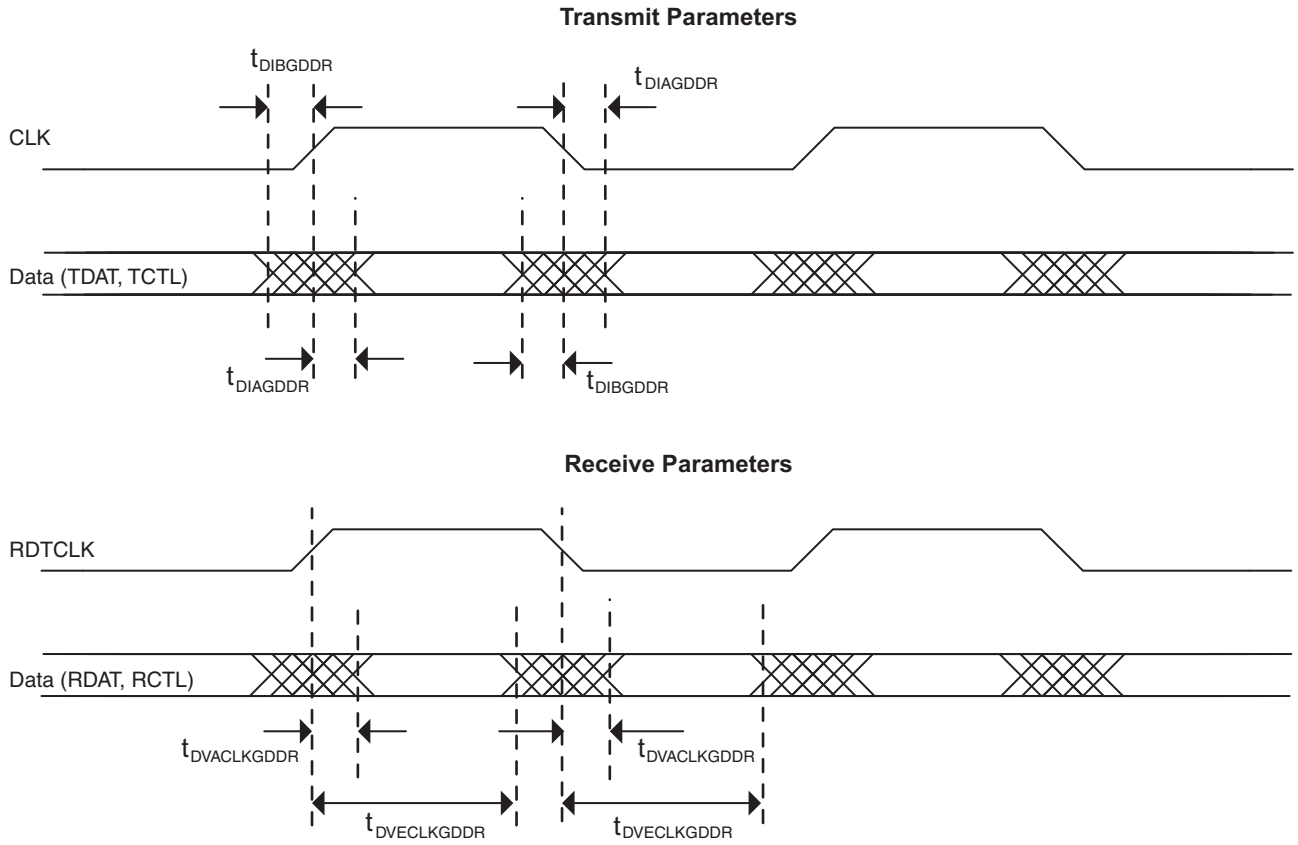
LA-LatticeECP3 External Switching Characteristics[1, 2]

Over Recommended Operating Ranges

Parameter	Description	Device	-6 / -6L		Units
			Min.	Max.	
Clocks					
Primary Clock [6]					
f_{MAX_PRI}	Frequency for Primary Clock Tree	LAE3-35EA	—	375	MHz
t_{W_PRI}	Pulse Width for Primary Clock	LAE3-35EA	1	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	LAE3-35EA	—	360	ps
t_{SKEW_PRIB}	Primary Clock Skew Within a Bank	LAE3-35EA	—	300	ps
f_{MAX_PRI}	Frequency for Primary Clock Tree	LAE3-17EA	—	375	MHz
t_{W_PRI}	Pulse Width for Primary Clock	LAE3-17EA	1	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	LAE3-17EA	—	370	ps
t_{SKEW_PRIB}	Primary Clock Skew Within a Bank	LAE3-17EA	—	240	ps
Edge Clock [6]					
f_{MAX_EDGE}	Frequency for Edge Clock	LAE3-35EA	—	375	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	LAE3-35EA	1.2	—	ns
$t_{SKEW\_EDGE\_DQS}$	Edge Clock Skew Within an Edge of the Device	LAE3-35EA	—	220	ps
f_{MAX_EDGE}	Frequency for Edge Clock	LAE3-17EA	—	375	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	LAE3-17EA	1.2	—	ns
$t_{SKEW\_EDGE\_DQS}$	Edge Clock Skew Within an Edge of the Device	LAE3-17EA	—	220	ps
Generic SDR					
General I/O Pin Parameters (using dedicated clock input Primary Clock without PLL) [2]					
t_{CO}	Clock to Output - PIO Output Register	LAE3-35EA	-	4.54	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LAE3-35EA	0.00	-	ns
t_{H}	Clock to Data Hold - PIO Input Register	LAE3-35EA	1.62	-	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LAE3-35EA	1.48	-	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LAE3-35EA	0.00	-	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LAE3-35EA	-	375	Mhz
t_{CO}	Clock to Output - PIO Output Register	LAE3-17EA	-	4.34	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LAE3-17EA	0.00	-	ns
t_{H}	Clock to Data Hold - PIO Input Register	LAE3-17EA	1.62	-	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LAE3-17EA	1.48	-	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LAE3-17EA	0.00	-	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LAE3-17EA	-	375	Mhz

Parameter	Description	Device	-6 / -6L		Units
			Min.	Max.	
General I/O Pin Parameters (using dedicated clock input Primary Clock with PLL with clock injection removal setting) [2]					
t_{COPLL}	Clock to Output - PIO Output Register	LAE3-35EA	-	2.72	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	LAE3-35EA	0.81	-	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	LAE3-35EA	0.37	-	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LAE3-35EA	1.82	-	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LAE3-35EA	0.00	-	ns
t_{COPLL}	Clock to Output - PIO Output Register	LAE3-17EA	-	2.49	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	LAE3-17EA	0.81	-	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	LAE3-17EA	0.37	-	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LAE3-17EA	1.82	-	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LAE3-17EA	0.00	-	ns
Generic DDR[12]					
Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Centered at Pin (GDDRX1_RX.SCLK.Centered) Using PCLK Pin for Clock Input					
t_{SUGDDR}	Data Setup Before CLK	All Devices	480	—	ps
t_{HOGDDR}	Data Hold After CLK	All Devices	480	—	ps
f_{MAX_GDDR}	DDRX1 Clock Frequency	All Devices	—	250	MHz
Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX1_RX.SCLK.PLL.Aligned) Using PLLCLKIN Pin for Clock Input					
Data Left, Right, and Top Sides and Clock Left and Right Sides					
$t_{DVACLKGDDR}$	Data Setup Before CLK	All Devices	—	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	All Devices	0.775	—	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency	All Devices	—	250	MHz
Generic DDRX1 Inputs with Clock and Data (>10 Bits Wide) Aligned at Pin (GDDRX1_RX.SCLK.Aligned) Using DLL - CLKIN Pin for Clock Input					
Data Left, Right and Top Sides and Clock Left and Right Sides					
$t_{DVACLKGDDR}$	Data Setup Before CLK	All Devices	-	0.225	UI
$t_{DVECLKGDDR}$	Data Hold After CLK	All Devices	0.775	-	UI
f_{MAX_GDDR}	DDRX1 Clock Frequency	All Devices	-	250	MHz

Figure 3-6. Generic DDRX1/DDRX2 (With Clock and Data Edges Aligned)



LA-LatticeECP3 Internal Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	-6 / -6L		Units
		Min.	Max.	
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register	0.080	-	ns
PLL Parameters				
t_{RSTREC_GPLL}	Reset Recovery to Rising Clock	1.00	—	ns
DSP Block Timing[2, 3]				
t_{SUI_DSP}	Input Register Setup Time	0.39	—	ns
t_{HI_DSP}	Input Register Hold Time	-0.21	—	ns
t_{SUP_DSP}	Pipeline Register Setup Time	2.39	—	ns
t_{HP_DSP}	Pipeline Register Hold Time	-1.16	—	ns
t_{SUO_DSP}	Output Register Setup Time	3.37	—	ns
t_{HO_DSP}	Output Register Hold Time	-1.86	—	ns
t_{COI_DSP}	Input Register Clock to Output Time	—	3.77	ns
t_{COP_DSP}	Pipeline Register Clock to Output Time	—	1.66	ns
t_{COO_DSP}	Output Register Clock to Output Time	—	0.63	ns
t_{SUOPT_DSP}	Opcode Register Setup Time	0.39	—	ns
t_{HOPT_DSP}	Opcode Register Hold Time	-0.27	—	ns
t_{SUDATA_DSP}	Cascade_data through ALU to Output Register Setup Time	2.16	—	ns
t_{HPDATA_DSP}	Cascade_data through ALU to Output Register Hold Time	-0.98	—	ns

1. Internal parameters are characterized but not tested on every device.
2. These parameters apply to LA-LatticeECP3 devices only.
3. DSP Block is configured in Multiply Add/Sub 18x18 Mode.

SERDES High-Speed Data Transmitter[1]

Table 3-8. Serial Output Timing and Levels

Symbol	Description	Frequency	Min.	Typ.	Max.	Units
$V_{TX-DIFF-P-P-1.44}$	Differential swing (1.44V setting)[1, 2]	0.15 to 3.125 Gbps	1150	1440	1730	mV, p-p
$V_{TX-DIFF-P-P-1.35}$	Differential swing (1.35V setting)[1, 2]	0.15 to 3.125 Gbps	1080	1350	1620	mV, p-p
$V_{TX-DIFF-P-P-1.26}$	Differential swing (1.26V setting)[1, 2]	0.15 to 3.125 Gbps	1000	1260	1510	mV, p-p
$V_{TX-DIFF-P-P-1.13}$	Differential swing (1.13V setting)[1, 2]	0.15 to 3.125 Gbps	840	1130	1420	mV, p-p
$V_{TX-DIFF-P-P-1.04}$	Differential swing (1.04V setting)[1, 2]	0.15 to 3.125 Gbps	780	1040	1300	mV, p-p
$V_{TX-DIFF-P-P-0.92}$	Differential swing (0.92V setting)[1, 2]	0.15 to 3.125 Gbps	690	920	1150	mV, p-p
$V_{TX-DIFF-P-P-0.87}$	Differential swing (0.87V setting)[1, 2]	0.15 to 3.125 Gbps	650	870	1090	mV, p-p
$V_{TX-DIFF-P-P-0.78}$	Differential swing (0.78V setting)[1, 2]	0.15 to 3.125 Gbps	585	780	975	mV, p-p
$V_{TX-DIFF-P-P-0.64}$	Differential swing (0.64V setting)[1, 2]	0.15 to 3.125 Gbps	480	640	800	mV, p-p
V_{OCM}	Output common mode voltage	—	V_{CCOB} -0.75	V_{CCOB} -0.60	V_{CCOB} -0.45	V
T_{TX-R}	Rise time (20% to 80%)	—	145	185	265	ps
T_{TX-F}	Fall time (80% to 20%)	—	145	185	265	ps
$Z_{TX-OI-SE}$	Output Impedance 50/75/HiZ Ohms (single ended)	—	-20%	50/75/ Hi Z	+20%	Ohms
R_{LTX-RL}	Return loss (with package)	—	10			dB
$T_{TX-INTRASKEW}$	Lane-to-lane TX skew within a SERDES quad block (intra-quad)	—	—	—	200	ps

1. All measurements are with 50 ohm impedance.
2. See TN1176, LatticeECP3 SERDES/PCS Usage Guide for actual binary settings and the min-max range.

SERDES External Reference Clock

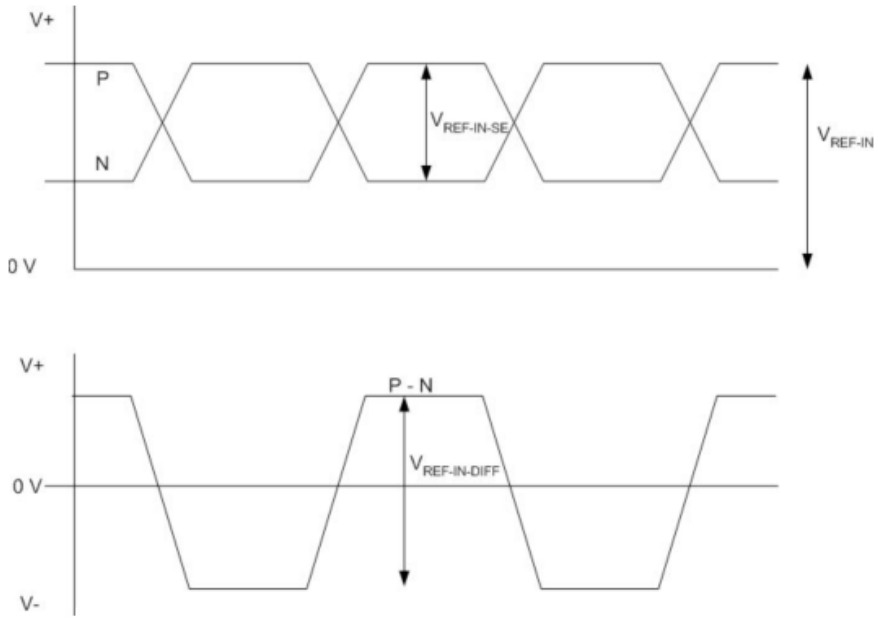
The external reference clock selection and its interface are a critical part of system applications for this product. Table 3-14 specifies reference clock requirements, over the full range of operating conditions.

Table 3-14. External Reference Clock Specification (refclkp/refclkn)

Symbol	Description	Min.	Typ.	Max.	Units
F_{REF}	Frequency range	15	—	320	MHz
$F_{REF-PPM}$	Frequency tolerance[1]	-1000	—	1000	ppm
$V_{REF-IN-SE}$	Input swing, single-ended clock[2]	200	—	V_{CCA}	mV, p-p
$V_{REF-IN-DIFF}$	Input swing, differential clock	200	—	$2*V_{CCA}$	mV, p-p differential
V_{REF-IN}	Input levels	0	—	V_{CCA} + 0.3	V
D_{REF}	Duty cycle[3]	40	—	60	%
T_{REF-R}	Rise time (20% to 80%)	200	500	1000	ps
T_{REF-F}	Fall time (80% to 20%)	200	500	1000	ps
$Z_{REF-IN-TERM-DIFF}$	Differential input termination	-20%	100/2K	+20%	Ohms
$C_{REF-IN-CAP}$	Input capacitance	—	—	7	pF

1. Depending on the application, the PLL_LOL_SET and CDR_LOL_SET control registers may be adjusted for other tolerance values as described in TN1176, LatticeECP3 SERDES/PCS Usage Guide.
2. The signal swing for a single-ended input clock must be as large as the p-p differential swing of a differential input clock to get the same gain at the input receiver. Lower swings for the clock may be possible, but will tend to increase jitter.
3. Measured at 50% amplitude.

Figure 3-13. SERDES External Reference Clock Waveforms



XAUI/Serial Rapid I/O Type 3/CPRI LV E.30 Electrical and Timing Characteristics

AC and DC Characteristics

Table 3-15. Transmit

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
T_{RF}	Differential rise/fall time	20%-80%	—	80	—	ps
$Z_{TX\_DIFF\_DC}$	Differential impedance		80	100	120	Ohms
J_{TX_DDJ}[2, 3, 4]	Output data deterministic jitter		—	—	0.17	UI
J_{TX_TJ}[1, 2, 3, 4]	Total output data jitter		—	—	0.35	UI

1. Total jitter includes both deterministic jitter and random jitter.
2. Jitter values are measured with each CML output AC coupled into a 50-ohm impedance (100-ohm differential impedance).
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Values are measured at 2.5 Gbps.

Table 3-16. Receive and Jitter Tolerance

Over Recommended Operating Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
RL_{RX_DIFF}	Differential return loss	From 100 MHz to 3.125 GHz	10	—	—	dB
RL_{RX_CM}	Common mode return loss	From 100 MHz to 3.125 GHz	6	—	—	dB
Z_{RX_DIFF}	Differential termination resistance		80	100	120	Ohms
J_{RX_DJ}[1, 2, 3]	Deterministic jitter tolerance (peak-to-peak)		—	—	0.37	UI
J_{RX_RJ}[1, 2, 3]	Random jitter tolerance (peak-to-peak)		—	—	0.18	UI
J_{RX_SJ}[1, 2, 3]	Sinusoidal jitter tolerance (peak-to-peak)		—	—	0.10	UI
J_{RX_TJ}[1, 2, 3]	Total jitter tolerance (peak-to-peak)		—	—	0.65	UI
T_{RX_EYE}	Receiver eye opening		0.35	—	—	UI

1. Total jitter includes deterministic jitter, random jitter and sinusoidal jitter. The sinusoidal jitter tolerance mask is shown in Figure 3-18.
2. Jitter values are measured with each high-speed input AC coupled into a 50-ohm impedance.
3. Jitter and skew are specified between differential crossings of the 50% threshold of the reference signal.
4. Jitter tolerance parameters are characterized when Full Rx Equalization is enabled.
5. Values are measured at 2.5 Gbps.

Pin Information Summary

Pin Information Summary		ECP3-17EA			ECP3-35EA		
Pin Type		256 ftBGA	328 csBGA	484 fpBGA	256 ftBGA	484 fpBGA	672 fpBGA
General Purpose Inputs/Outputs per Bank	Bank 0	26	20	36	26	42	48
	Bank 1	14	10	24	14	36	36
	Bank 2	6	7	12	6	24	24
	Bank 3	18	12	44	16	54	59
	Bank 6	20	11	44	18	63	61
	Bank 7	19	26	32	19	36	42
	Bank 8	24	24	24	24	24	24
General Purpose Inputs per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	2	2	2	2	4	4
	Bank 3	0	0	0	2	4	4
	Bank 6	0	0	0	2	4	4
	Bank 7	4	4	4	4	4	4
	Bank 8	0	0	0	0	0	0
General Purpose Outputs per Bank	Bank 0	0	0	0	0	0	0
	Bank 1	0	0	0	0	0	0
	Bank 2	0	0	0	0	0	0
	Bank 3	0	0	0	0	0	0
	Bank 6	0	0	0	0	0	0
	Bank 7	0	0	0	0	0	0
	Bank 8	0	0	0	0	0	0
Total Single-Ended User I/O		133	116	222	133	295	310
VCC		6	16	16	6	16	32
VCCAUX		4	5	8	4	8	12
VTT		4	7	4	4	4	4
VCCA		4	6	4	4	4	8
VCCPLL		2	2	4	2	4	4
VCCIO	Bank 0	2	3	2	2	2	4
	Bank 1	2	3	2	2	2	4
	Bank 2	2	2	2	2	2	4
	Bank 3	2	3	2	2	2	4
	Bank 6	2	3	2	2	2	4
	Bank 7	2	3	2	2	2	4
	Bank 8	1	2	2	1	2	2
VCCJ		1	1	1	1	1	1
TAP		4	4	4	4	4	4
GND, GNDIO		51	126	98	51	98	139
NC		0	0	73	0	0	96
Reserved[1]		0	0	2	0	2	2
SERDES		26	18	26	26	26	26
Miscellaneous Pins		8	8	8	8	8	8
Total Bonded Pins		256	328	484	256	484	672

Package Pinout Information

Package pinout information can be found under “Data Sheets” on the LatticeECP3 product pages on the Lattice website at www.latticesemi.com/products/fpga/ecp3 and in the Diamond software tool. To create a pin information file from within Diamond select **Tools > Spreadsheet View** or **Tools >Package View**; then, select **File > Export** and choose a type of output file. See Diamond Help for more information.

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following:

- Thermal Management document
- TN1181, Power Consumption and Management for LatticeECP3 Devices
- Power Calculator tool included with the Diamond design tool, or as a standalone download from www.latticesemi.com/software