



Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2125
Number of Logic Elements/Cells	17000
Total RAM Bits	716800
Number of I/O	116
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	328-LFBGA, CSBGA
Supplier Device Package	328-CSBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lae3-17ea-6lmg328e

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 2-2. PFU Diagram



Slice

Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 through Slice 2 can be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/ asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2-1.	Resources and	Modes Available	e per Slice
------------	---------------	-----------------	-------------

	PFU E	PFU BLock PFF Block		
Slice	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 10 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.



PLL/DLL Cascading

LA-LatticeECP3 devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are:

- PLL to PLL supported
- PLL to DLL supported

The DLLs in the LA-LatticeECP3 are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

For further information about the DLL, please see the list of technical documentation at the end of this data sheet.

PLL/DLL PIO Input Pin Connections

All LA-LatticeECP3 devices contains two DLLs and up to ten PLLs, arranged in quadrants. If a PLL and a DLL are next to each other, they share input pins as shown in the Figure 2-7.

Figure 2-7. Sharing of PIO Pins by PLLs and DLLs in LA-LatticeECP3 Devices





Clock Dividers

LA-LatticeECP3 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, the Slave Delay lines, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets input and asynchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see TN1178, LatticeECP3 sysCLOCK PLL/DLL Design and Usage Guide. Figure 2-8 shows the clock divider connections.



Primary Clock Routing

The purpose of the primary clock routing is to distribute primary clock sources to the destination quadrants of the device. A global primary clock is a primary clock that is distributed to all quadrants. The clock routing structure in LA-LatticeECP3 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-11 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

Figure 2-11. Per Quadrant Primary Clock Selection



Dynamic Clock Control (DCC)

The DCC (Quadrant Clock Enable/Disable) feature allows internal logic control of the quadrant primary clock network. When a clock network is disabled, all the logic fed by that clock does not toggle, reducing the overall power consumption of the device.

Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved regardless of when the select signal is toggled. There are two DCS blocks per quadrant; in total, there are eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-11).

Figure 2-12 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, please see the list of technical documentation at the end of this data sheet.



Figure 2-12. DCS Waveforms



Secondary Clock/Control Sources

LA-LatticeECP3 devices derive eight secondary clock sources (SC0 through SC7) from six dedicated clock input pads and the rest from routing. Figure 2-13 shows the secondary clock sources. All eight secondary clock sources are defined as inputs to a per-region mux SC0-SC7. SC0-SC3 are primary for control signals (CE and/or LSR), and SC4-SC7 are for the clock.

In an actual implementation, there is some overlap to maximize routability. In addition to SC0-SC3, SC7 is also an input to the control signals (LSR or CE). SC0-SC2 are also inputs to clocks along with SC4-SC7.





Note: Clock inputs can be configured in differential or single-ended mode.

Secondary Clock/Control Routing

Global secondary clock is a secondary clock that is distributed to all regions. The purpose of the secondary clock routing is to distribute the secondary clock sources to the secondary clock regions. Secondary clocks in the LA-LatticeECP3 devices are region-based resources. Certain EBR rows and special vertical routing channels bind the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP slice in the DSP row or the center of the DSP row. Figure 2-14 shows this special vertical routing channel and the 20 secondary clock regions for the LA-LatticeECP3 family of devices. All devices in the LA-LatticeECP3 family have eight secondary clock resources per region (SC0 to SC7). The same secondary clock routing can be used for control signals.



Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs, DLLs, Slave Delay and clock dividers as shown in Figure 2-18.





Notes:

1. Clock inputs can be configured in differential or single ended mode.

2. The two DLLs can also drive the two top edge clocks.

3. The top left and top right PLL can also drive the two top edge clocks.

Edge Clock Routing

LA-LatticeECP3 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are six edge clocks per device: two edge clocks on each of the top, left, and right edges. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL Slave Delay Line block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-19 shows the selection muxes for these clocks.



as, overflow, underflow and convergent rounding, etc.

- Flexible cascading across slices to get larger functions
- RTL Synthesis friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

For most cases, as shown in Figure 2-23, the LA-LatticeECP3 DSP slice is backwards-compatible with the LatticeECP2[™] sysDSP block, such that, legacy applications can be targeted to the LA-LatticeECP3 sysDSP slice. The functionality of one LatticeECP2 sysDSP Block can be mapped into two adjacent LA-LatticeECP3 sysDSP slices, as shown in Figure 2-24.



Figure 2-23. Simplified sysDSP Slice Block Diagram







Note: A_ALU, B_ALU and C_ALU are internal signals generated by combining bits from AA, AB, BA BB and C inputs. See TN1182, LatticeECP3 sysDSP Usage Guide, for further information.

The LatticeECP2 sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

Table 2-8 shows the capabilities of each of the LA-LatticeECP3 slices versus the above functions.

Table 2-8. Maximum Number of Elements in a Slice

Width of Multiply	x9	x18	x36
MULT	4	2	1/2
MAC	1	1	_
MULTADDSUB	2	1	—
MULTADDSUBSUM	1 ¹	1/2	_

1. One slice can implement 1/2 9x9 m9x9addsubsum and two m9x9addsubsum with two slices.

Some options are available in the four elements. The input register in all the elements can be directly loaded or can be loaded as a shift register from previous operand registers. By selecting "dynamic operation" the following operations are possible:

- In the Add/Sub option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.



MULTADDSUB DSP Element

In this case, the operands AA and AB are multiplied and the result is added/subtracted with the result of the multiplier operation of operands BA and BB. The user can enable the input, output and pipeline registers. Figure 2-28 shows the MULTADDSUB sysDSP element.

Figure 2-28. MULTADDSUB





Figure 2-36. DQS Local Bus



Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LA-LatticeECP3 family contains dedicated circuits to transfer data between these domains. A clock polarity selector is used to prevent set-up and hold violations at the domain transfer between DQS (delayed) and the system clock. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects the first DQS rising edge after the preamble state. This signal is used to control the polarity of the clock to the synchronizing registers.

DDR3 Memory Support

LA-LatticeECP3 supports the read and write leveling required for DDR3 memory interfaces.

Read leveling is supported by the use of the DDRCLKPOL and the DDRLAT signals generated in the DQS Read Control logic block. These signals dynamically control the capture of the data with respect to the DQS at the input register block.



Figure 2-37. LA-LatticeECP3 Banks



LA-LatticeECP3 devices contain two types of sysI/O buffer pairs.

1. Top (Bank 0 and Bank 1) and Bottom sysIO Buffer Pairs (Single-Ended Outputs Only)

The sysl/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input. Only the top edge buffers have a programmable PCI clamp.

The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

The top and bottom sides are ideal for general purpose I/O, PCI, and inputs for LVDS (LVDS outputs are only allowed on the left and right sides). The top side can be used for the DDR3 ADDR/CMD signals.

The I/O pins located on the top and bottom sides of the device (labeled PTxxA/B or PBxxA/B) are fully hot socketable. Note that the pads in Banks 3, 6 and 8 are wrapped around the corner of the device. In these banks, only the pads located on the top or bottom of the device are hot socketable. The top and bottom side pads can be identified by the Lattice Diamond tool.

DC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
$I_{\rm IL}, I_{\rm IH}^{1,4}$	Input or I/O Low Leakage	$0 \le V_{IN} \le (V_{CCIO} - 0.2V)$	—		10	μΑ
I _{IH} ^{1, 3}	Input or I/O High Leakage	$(V_{CCIO} - 0.2V) < V_{IN} \le 3.6V$	—	_	150	μΑ
I _{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7 V_{CCIO}$	-30	_	-210	μΑ
I _{PD}	I/O Active Pull-down Current	$V_{IL} (MAX) \le V_{IN} \le V_{CCIO}$	30	_	210	μΑ
I _{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL} (MAX)$	30	_	—	μΑ
I _{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7 V_{CCIO}$	-30	_	—	μΑ
I _{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	_	210	μΑ
I _{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{CCIO}$	—	_	-210	μΑ
V _{BHT}	Bus Hold Trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{IL} (MAX)		V_{IH} (MIN)	V
C1	I/O Capacitance ²	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} \text{ (MAX)}$	_	5	8	pf
C2	Dedicated Input Capacitance ²	$V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 \text{ to } V_{IH} \text{ (MAX)}$	_	5	7	pf

Over Recommended Operating Conditions

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. $T_A 25^{\circ}C$, f = 1.0MHz.

3. Applicable to general purpose I/Os in top and bottom banks. 4. When used as V_{REF} maximum leakage= 25µA.



BLVDS25

The LA-LatticeECP3 devices support the BLVDS standard. This standard is emulated using complementary LVC-MOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.





Table 3-4. BLVDS25 DC Conditions¹

Over Recommended	Operating	Conditions
------------------	-----------	------------

		Typical		
Parameter	Description	Ζο = 45 Ω	Ζο = 90 Ω	Units
V _{CCIO}	Output Driver Supply (+/- 5%)	2.50	2.50	V
Z _{OUT}	Driver Impedance	10.00	10.00	Ω
R _S	Driver Series Resistor (+/- 1%)	90.00	90.00	Ω
R _{TL}	Driver Parallel Resistor (+/- 1%)	45.00	90.00	Ω
R _{TR}	Receiver Termination (+/- 1%)	45.00	90.00	Ω
V _{OH}	Output High Voltage	1.38	1.48	V
V _{OL}	Output Low Voltage	1.12	1.02	V
V _{OD}	Output Differential Voltage	0.25	0.46	V
V _{CM}	Output Common Mode Voltage	1.25	1.25	V
I _{DC}	DC Output Current	11.24	10.20	mA

1. For input buffer, see LVDS table.



Typical Building Block Function Performance

Pin-to-Pin Performance (LVCMOS25 12mA Drive)¹

Function	-6 / -6L Timing	Units
Basic Functions		
16-bit Decoder	4.9	ns
32-bit Decoder	5.3	ns
64-bit Decoder	7.0	ns
4:1 MUX	4.9	ns
8:1 MUX	5.2	ns
16:1 MUX	5.7	ns
32:1 MUX	5.8	ns

1. Automotive timing numbers are shown.

Register-to-Register Performance¹

Function	-6 / -6L Timing	Units
Basic Functions	· ·	
16-bit Decoder	368	MHz
32-bit Decoder	368	MHz
64-bit Decoder	247	MHz
4:1 MUX	368	MHz
8:1 MUX	368	MHz
16:1 MUX	368	MHz
32:1 MUX	358	MHz
8-bit Adder	368	MHz
16-bit Adder	368	MHz
64-bit Adder	252	MHz
16-bit Counter	368	MHz
32-bit Counter	368	MHz
64-bit Counter	262	MHz
64-bit Accumulator	251	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	272	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	272	MHz
1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers	103	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	222	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	368	MHz
32x4 Pseudo-Dual Port RAM	368	MHz
64x8 Pseudo-Dual Port RAM	324	MHz
DSP Function		
18x18 Multiplier (All Registers)	331	MHz
9x9 Multiplier (All Registers)	331	MHz
36x36 Multiply (All Registers)	212	MHz
18x18 Multiply/Accumulate (Input & Output Registers)	176	MHz
18x18 Multiply-Add/Sub (All Registers)	331	MHz
1. Automotive timing numbers are shown.	I	



Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tool are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.



Figure 3-6. Generic DDRX1/DDRX2 (With Clock and Data Edges Aligned)





Figure 3-7. DDR/DDR2/DDR3 Parameters



Figure 3-8. Generic DDRX1/DDRX2 (With Clock Center on Data Window)



Transmit Parameters



sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Clock	Min.	Тур.	Max.	Units
4	Input clock frequency (CLKI,		Edge clock	2	—	500	MHz
IN	CLKFB)		Primary clock ⁴	2	—	420	MHz
4	Output clock frequency (CLKOP,		Edge clock	4	—	500	MHz
OUT	CLKOS)		Primary clock ⁴	4		420	MHz
f _{OUT1}	K-Divider output frequency	CLKOK		0.03125		250	MHz
f _{OUT2}	K2-Divider output frequency	CLKOK2		0.667		166	MHz
f _{VCO}	PLL VCO frequency			500	_	1000	MHz
f _{PFD} ³	Phase detector input frequency		Edge clock	2		500	MHz
			Primary clock ⁴	2		420	MHz
AC Charac	teristics						
t _{PA}	Programmable delay unit			65	130	260	ps
			Edge clock	45	50	55	%
t _{DT}	CLKOS at 50% setting)	$f_{OUT} \le 250 \text{ MHz}$	Primary clock	45	50	55	%
		f _{OUT} > 250MHz	Primary clock	30	50	70	%
t _{CPA}	Coarse phase shift error (CLKOS, at all settings)			-5	0	+5	% of period
t _{OPW}	Output clock pulse width high or low (CLKOS)			1.8	_	_	ns
	Output clock period jitter	$f_{OUT} \ge 420 MHz$		—	—	200	ps
t _{OPJIT} 1		$420MHz > f_{OUT} \ge 100MHz$		—	—	250	ps
t _{DT}		f _{OUT} < 100MHz		—		0.025	UIPP
t _{SK}	Input clock to output clock skew when N/M = integer			_	_	500	ps
+ 2		2 to 25 MHz		—		200	us
LOCK_	Lock lime	25 to 500 MHz		—	—	50	us
t _{UNLOCK}	Reset to PLL unlock time to ensure fast reset			_	_	50	ns
t _{HI}	Input clock high time	90% to 90%		0.5	—	-	ns
t _{LO}	Input clock low time	10% to 10%		0.5	—	-	ns
t _{IPJIT}	Input clock period jitter			—	—	400	ps
+	Reset signal pulse width high, RSTK			10	—	—	ns
^I RST	Reset signal pulse width high, RST			500	_	_	ns

Over Recommended Operating Conditions

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock with no additional I/O toggling.

2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} > 4MHz$. For $f_{PFD} < 4MHz$, the jitter numbers may not be met in certain conditions. Please contact the factory for $f_{PFD} < 4MHz$.

4. When using internal feedback, maximum can be up to 500 MHz.



Figure 3-18. XAUI Sinusoidal Jitter Tolerance Mask



Note: The sinusoidal jitter tolerance is measured with at least 0.37Ulpp of Deterministic jitter (Dj) and the sum of Dj and Rj (random jitter) is at least 0.55Ulpp. Therefore, the sum of Dj, Rj and Sj (sinusoidal jitter) is at least 0.65Ulpp (Dj = 0.37, Rj = 0.18, Sj = 0.1).



JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
f _{MAX}	TCK clock frequency	_	25	MHz
t _{BTCP}	TCK [BSCAN] clock pulse width	40	_	ns
t _{BTCPH}	TCK [BSCAN] clock pulse width high	20	_	ns
t _{BTCPL}	TCK [BSCAN] clock pulse width low	20	_	ns
t _{BTS}	TCK [BSCAN] setup time	10	_	ns
t _{BTH}	TCK [BSCAN] hold time	8	_	ns
t _{BTRF}	TCK [BSCAN] rise/fall time	50	_	mV/ns
t _{BTCO}	TAP controller falling edge of clock to valid output	_	10	ns
t _{BTCODIS}	TAP controller falling edge of clock to valid disable	_	10	ns
t _{BTCOEN}	TAP controller falling edge of clock to valid enable	_	10	ns
t _{BTCRS}	BSCAN test capture register setup time	8	_	ns
t _{BTCRH}	BSCAN test capture register hold time	25	_	ns
t _{BUTCO}	BSCAN test update register, falling edge of clock to valid output	_	25	ns
t _{BTUODIS}	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
t _{BTUPOEN}	BSCAN test update register, falling edge of clock to valid enable	_	25	ns

Figure 3-28. JTAG Port Timing Waveforms





sysl/O Differential Electrical Characteristics

Transition Reduced LVDS (TRLVDS DC Specification)

Over Recommended Operating Conditions

Symbol	Description	Min.	Nom.	Max.	Units
V _{CCO}	Driver supply voltage (+/- 5%)	3.14	3.3	3.47	V
V _{ID}	Input differential voltage	150	_	1200	mV
V _{ICM}	Input common mode voltage	3	_	3.265	V
V _{CCO}	Termination supply voltage	3.14	3.3	3.47	V
R _T	Termination resistance (off-chip)	45	50	55	Ohms

Note: LA-LatticeECP3 only supports the TRLVDS receiver.



Mini LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Тур.	Max.	Units
Z _O	Single-ended PCB trace impedance	30	50	75	ohms
R _T	Differential termination resistance	50	100	150	ohms
V _{OD}	Output voltage, differential, V _{OP} - V _{OM}	300	_	600	mV
V _{OS}	Output voltage, common mode, $ V_{OP} + V_{OM} /2$	1	1.2	1.4	V
ΔV_{OD}	Change in V _{OD} , between H and L	—	_	50	mV
ΔV_{ID}	Change in V _{OS} , between H and L	—	_	50	mV
V _{THD}	Input voltage, differential, V _{INP} - V _{INM}	200	_	600	mV
V _{CM}	Input voltage, common mode, $ V_{INP} + V_{INM} /2$	0.3+(V _{THD} /2)	_	2.1-(V _{THD} /2)	
T _R , T _F	Output rise and fall times, 20% to 80%	—	_	550	ps
T _{ODUTY}	Output clock duty cycle	40	_	60	%

Note: Data is for 6mA differential current drive. Other differential driver current options are available.