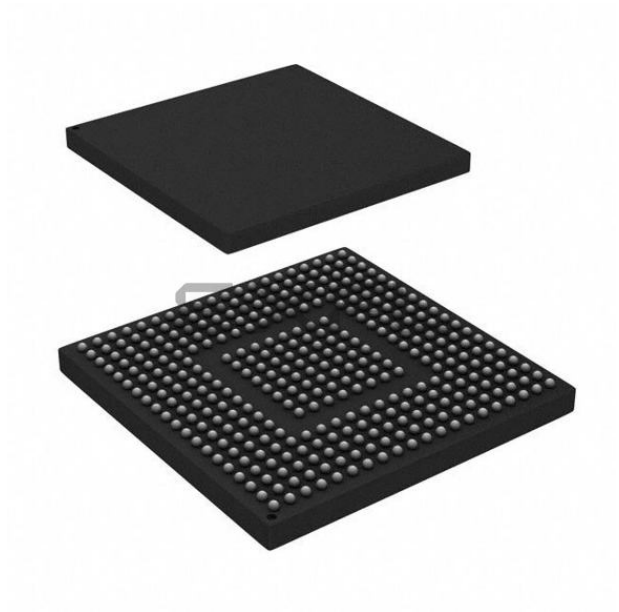

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5 + Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	400MHz, 133MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, Hashing, RNG, RTC, RTIC, Secure JTAG, SNVS, TZ ASC, TZ WDOG
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/svf532r2k1cmk4

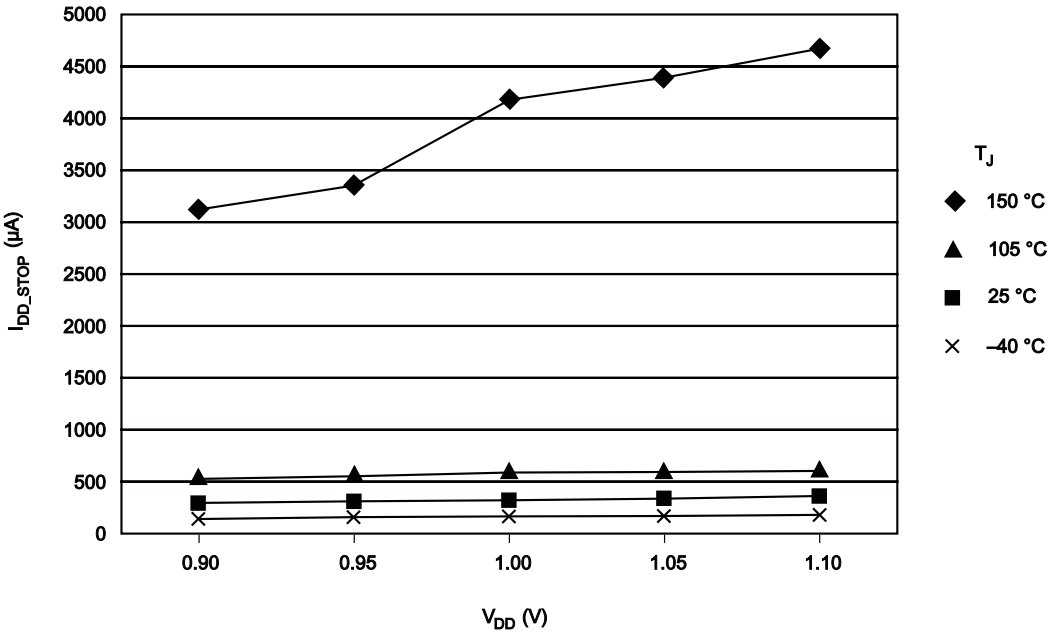
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

6.2.3.3 LDO_3P0

Table 14. LDO_3P0 parameters

Specification	Min	Typ	Max	Unit	Comments
Input OTG VBUS Supply	4.4		5.25	V	
Input HOST VBUS Supply	4.4		5.25	V	
VDD3P0_OUT	2.9	3.0	3.1	V	Regulator output at default setting
I_out	-		50	mA	500 mV drop-out voltage
Regulator output programming range	2.625		3.4	V	Programmable in 25mV steps
[P:][C:] Brownout Voltage	2.75	2.85		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

NOTE

These values are with Anadig_REG_3P0[ENABLE_ILIMIT]= 0 and Anadig_REG_3P0[ENABLE_LINREG]= 1. It is required to set these values before using USB.

6.2.4 Power consumption operating behaviors

Table 15. Power consumption operating behaviors

Symbol	Description	Typ.[1]	Max.[2]	Unit	Notes
I_{DD_RUN}	Run mode current — All functionalities of the chip available	400	850	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.3 V ± 10%	80	500	mA	3
I_{DD_LPRUN}	Low-power run mode current at 3.3 V ± 10%, 24MHz operation, PLL Bypass.	13	325	mA	4
I_{DD_ULPRUN}	Ultra-low-power run mode current at 3.3 V ± 10%	12	395	mA	5
I_{DD_STOP}	Stop mode current at 3.3 V ± 10%	7	300	mA	6
I_{DD_LPS3}	Low-power stop3 mode current at 3.3 V ± 10%	300	1300	uA	7
I_{DD_LPS2}	Low-power stop 2 mode current at 3.3 V ± 10%	50	875	uA	8
I_{DD_VBAT}	Battery backup mode	5	45	uA	9

1. The Typ numbers represent the average value taken from a matrix lot of parts across normal process variation at ambient temperature.

3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
4. IEC Level Maximums: N ≤ 12dBmV, M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV

6.2.7 EMC Radiated Emissions Web Search Procedure boilerplate

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

6.2.8 Capacitance attributes

Table 18. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

7 I/O parameters

7.1 GPIO parameters

Table 19. GPIO DC operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
vddi[1]	Core internal supply voltage		1.2		V
ovdd	I/O output supply voltage	3	3.3	3.6	V

1. This is internally controlled.

Table 20. GPIO DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Voh	High-level output voltage	Ioh= -1mA	ovdd-0.15			V

Table continues on the next page...

1. Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac).
2. The typical value of Vix(ac) is expected to be about 0.5*ovdd, and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 27. DDR3 mode AC Electrical characteristics

Symbol	Parameter	Test condition	Min	Max	Unit	Notes
Vih(ac)	AC input logic high		Vref+0.175	ovdd	V	Note that the JEDEC JESD79_3E specification supersedes any specification in this document
Vil(ac)	AC input logic low		ovss	Vref-0.175	V	
Vidh(ac)	AC differential input high voltage		0.35	-	V	
Vidl(ac)[1]	AC differential input low voltage		0.35		V	
Vix(ac)[2]	AC differential input crosspoint voltage	relative to ovdd/2	Vref-0.15	Vref+0.15	V	
Vpeak	Over/undershoot peak			0.4	V	
Varea	Over/undershoot area (above ovdd or below ovss)	at 800 MHz data rate		0.5	V*ns	
tsr	Single output slew rate		0.4	2	V/ns	
tskd	Skew between pad rise/fall asymmetry + skew cased by SSN			0.2	ns	

1. Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac).
2. The typical value of Vix(ac) is expected to be about 0.5*ovdd, and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

8 Power supplies and sequencing

8.1 Power sequencing

Table 28. Power sequencing

Power Supply (PKG Level)	Board Level Power Nets	Parameters	Power Order	Comment
VBAT	VBAT	Battery supply in case of LDOIN fails	NA	

Table continues on the next page...

9.1.1.2 12-bit ADC characteristics

Table 32. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions	Symb	Min	Typ	Max	Unit	Comment
Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}		250		µA	ADLSMP=0 ADSTS=10 ADCO=1
	ADLPC=0, ADHSC=0			350			
	ADLPC=0, ADHSC=1			400			
Supply Current	Stop, Reset, Module Off	I_{DDAD}		0.01	0.8	µA	
ADC Asynchronous Clock Source	ADHSC=0	f_{ADACK}		10		MHz	t_{ADACK} = 1/f_{ADACK}
	ADHSC=1			20			
Sample Cycles	ADLSMP=0, ADSTS=00	Csamp		2		cycles	
	ADLSMP=0, ADSTS=01			4			
	ADLSMP=0, ADSTS=10			6			
	ADLSMP=0, ADSTS=11			8			
	ADLSMP=1, ADSTS=00			12			
	ADLSMP=1, ADSTS=01			16			
	ADLSMP=1, ADSTS=10			20			
	ADLSMP=1, ADSTS=11			24			
Conversion Cycles	ADLSMP=0 ADSTS=00	Cconv		28		cycles	
	ADLSMP=0 ADSTS=01			30			
	ADLSMP=0 ADSTS=10			32			
	ADLSMP=0 ADSTS=11			34			
	ADLSMP=1 ADSTS=00			38			
	ADLSMP=1 ADSTS=01			42			
	ADLSMP=1 ADSTS=10			46			
	ADLSMP=1, ADSTS=11			50			
Conversion Time	ADLSMP=0 ADSTS=00	Tconv		0.7		µs	Fadc=40 MHz
	ADLSMP=0 ADSTS=01			0.75			

Table continues on the next page...

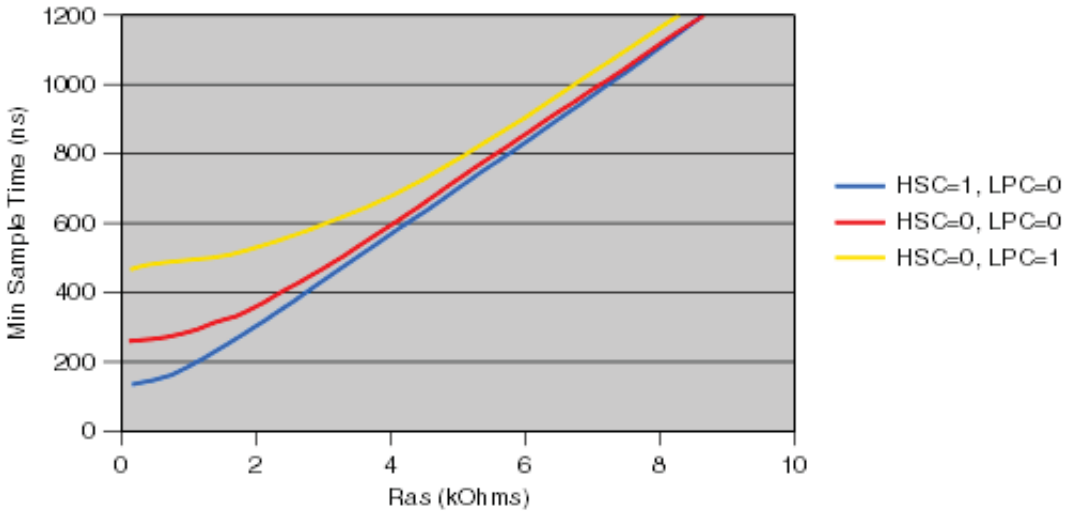


Figure 8. Minimum Sample Time Vs Ras (Cas = 10pF)

9.1.2 12-bit DAC electrical characteristics

9.1.2.1 12-bit DAC operating requirements

Table 33. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Typ	Max.	Unit	Notes
VDDA33_ADC	Supply voltage	3.0	3.3	3.6	V	
VREFH_ADC	Reference voltage	2.5	3.3	VDDA33_ADC	V	1
C_L	Output load capacitance	—		100	pF	2
I_L	Output load current	—		1	mA	

1. User will need to set up DACx_STATCTRL [DACRFS]=1 to select the valid VREFH_ADC reference. When DACx_STATCTRL [DACRFS]=0, the DAC reference is connected to an internal ground node and is not a valid voltage reference. Note that the DAC and ADC share the VREFH_ADC reference simultaneously.)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

9.1.2.2 12-bit DAC operating behaviors

Table 34. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	100	µA	
I_{DDA_DACHP}	Supply current — high-power mode	—	—	500	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	10	15	µs	

Table continues on the next page...

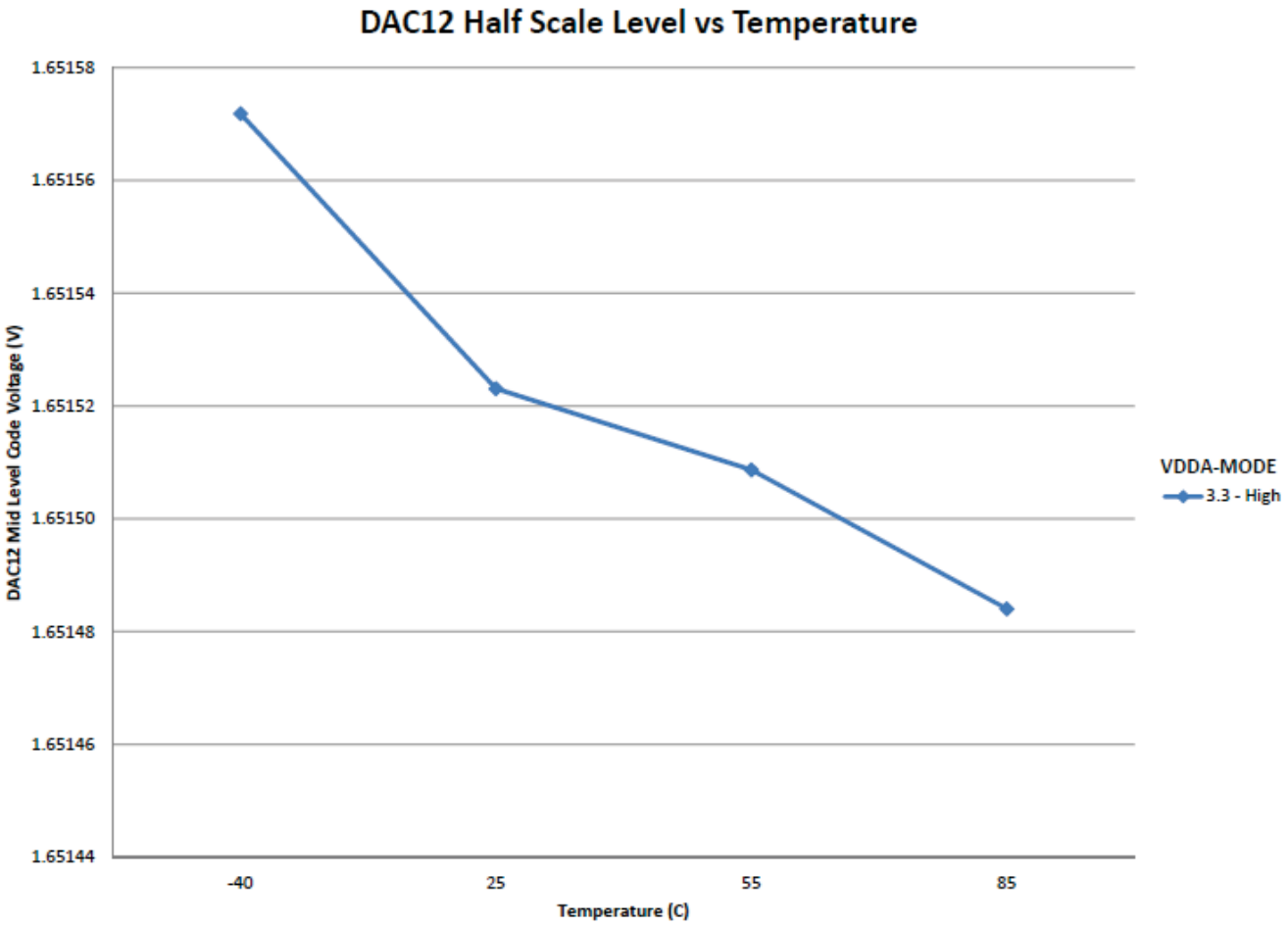


Figure 11. Offset at half scale vs. temperature

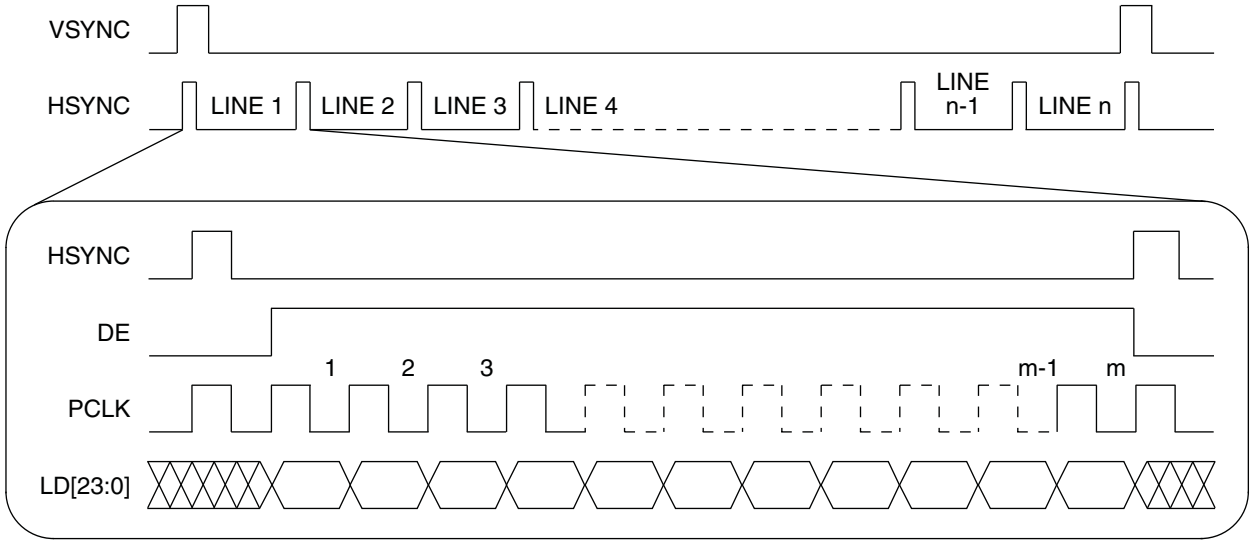
9.1.3 VideoADC Specifications

This section describes the electrical specification and characteristics of the VideoADC Analog Front End.

Table 35. VideoADC Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDDA33_AFE	Supply voltage	3.0	3.3	3.6	V	—
	Supply current	—	—	41	mA	—
VDDA12_AFE	Supply voltage	1.1	1.2	1.26	V	—
	Supply current	—	—	14	mA	—
V_{in}	Input signal voltage range	0	0.5	1.4	V	—
	External AC coupling	10	47		nF	The external AC coupling capacitance cannot be too large.

Table continues on the next page...



9.2.1.2 Interface to TFT LCD Panels—Pixel Level Timings

This section provides the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the figure below are programmable. This timing diagram corresponds to positive polarity of the PCLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the HSYNC, VSYNC and DE signals. The user can select the polarity of the HSYNC and VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DE signal is always active-high. Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the clock divide . The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

Table 36. LCD interface timing parameters—horizontal and vertical

Symbol	Characteristic		Unit
t_{PCP}	Display pixel clock period	11.2	ns
t_{PWH}	HSYNC pulse width	PW_H * t_{PCP}	ns
t_{BPH}	HSYNC back porch width	BP_H * t_{PCP}	ns
t_{FPH}	HSYNC front porch width	FP_H * t_{PCP}	ns
t_{SW}	Screen width	DELTA_X * t_{PCP}	ns
t_{HSP}	HSYNC (line) period	(PW_H + BP_H + FP_H + DELTA_X) * t_{PCP}	ns
t_{PWV}	VSYNC pulse width	PWV * t_{HSP}	ns
t_{BPV}	VSYNC back porch width	BP_V * t_{HSP}	ns
t_{FPV}	VSYNC front porch width	FP_V * t_{HSP}	ns
t_{SH}	Screen height	DELTA_Y * t_{HSP}	ns
t_{VSP}	VSYNC (frame) period	(PW_V + BP_V + FP_V + DELTA_Y) * t_{HSP}	ns

9.5 Memory interfaces

9.5.1 QuadSPI timing

- All data is based on a negative edge data launch from the device and a negative edge data capture, as shown in the timing diagrams in this section. This corresponds to the N/1 sample point as shown in the reference manual QSPI section "Internal Sampling of Serial Flash Input Data."
- Measurements are with a load of 35 pF on output pins. I/P Slew : 1ns
- Timings assume a setting of 0x0000_000x for QSPI_SMPR register (see the reference manual for details).

SDR mode

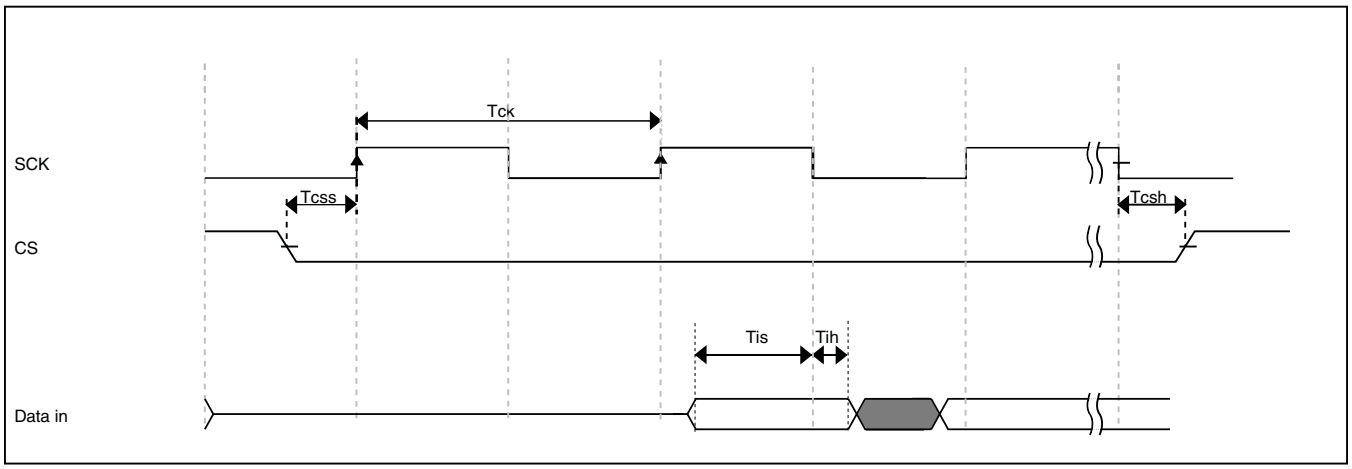


Figure 30. QuadSPI Input/Read timing (SDR mode)

Table 48. QuadSPI Input/Read timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	4.5	—	ns
T_{ih}	Hold time requirement for incoming data	0	—	ns

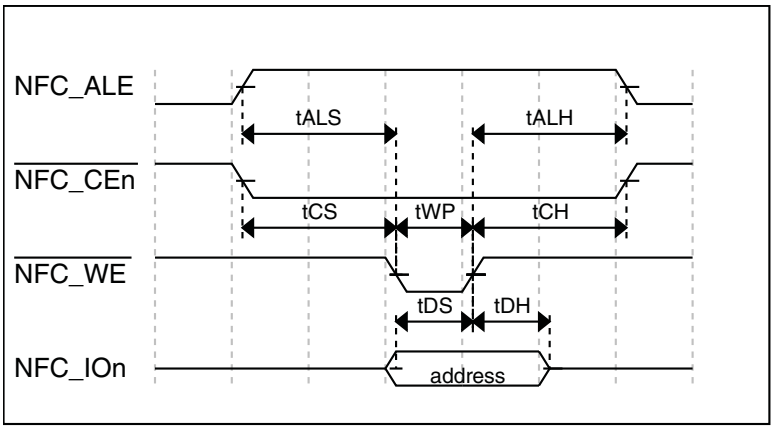


Figure 35. Address latch cycle timing

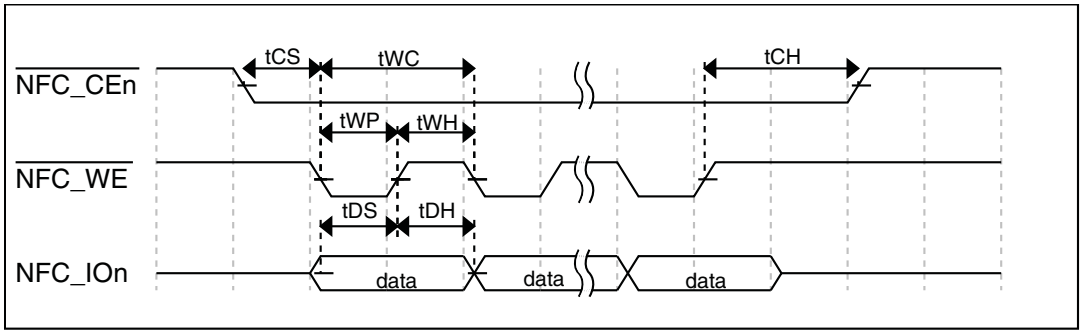


Figure 36. Write data latch cycle timing

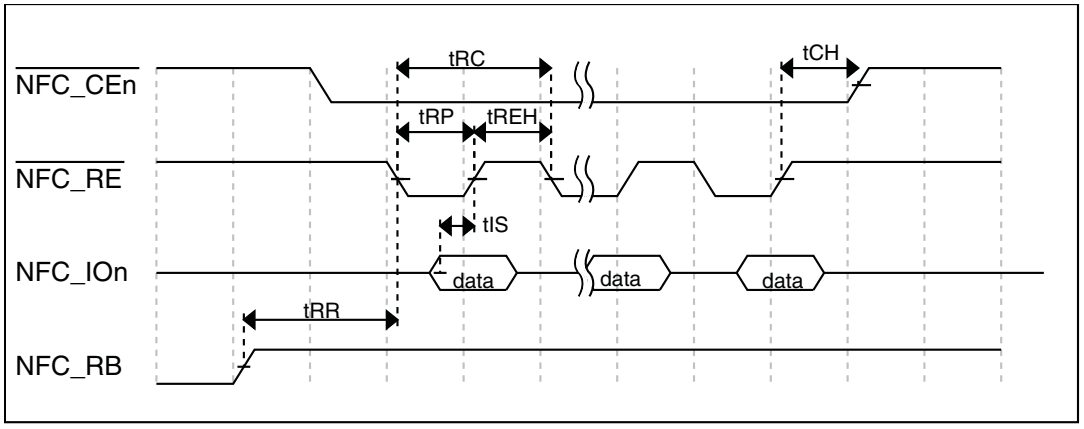


Figure 37. Read data latch cycle timing in non-fast mode

9.5.4.2 DDR3 Read Cycle

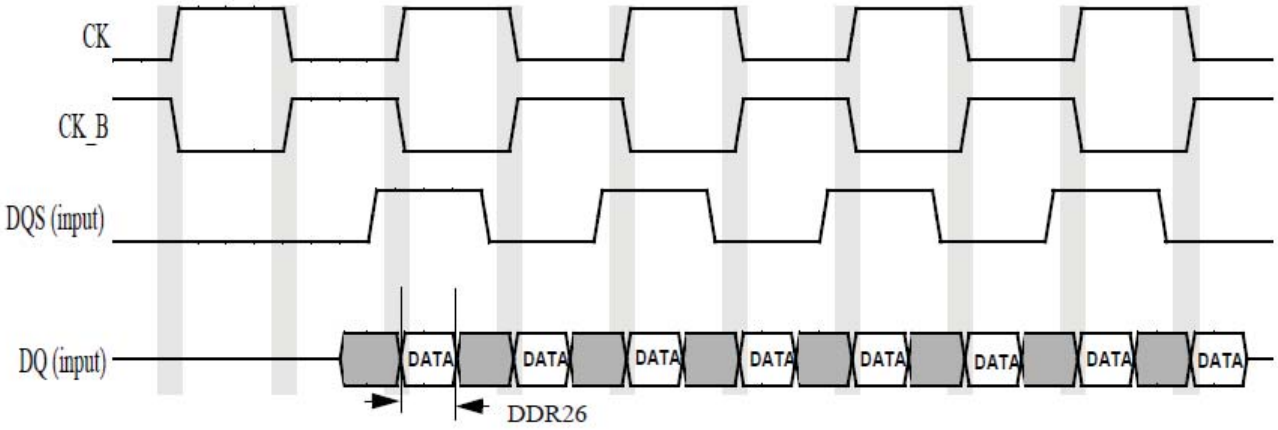


Figure 42. DDR3 Read Cycle

Table 55. DDR3 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR26	Minimum required DQ valid window width	-	750	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

9.5.4.6 LPDDR2 Write Cycle

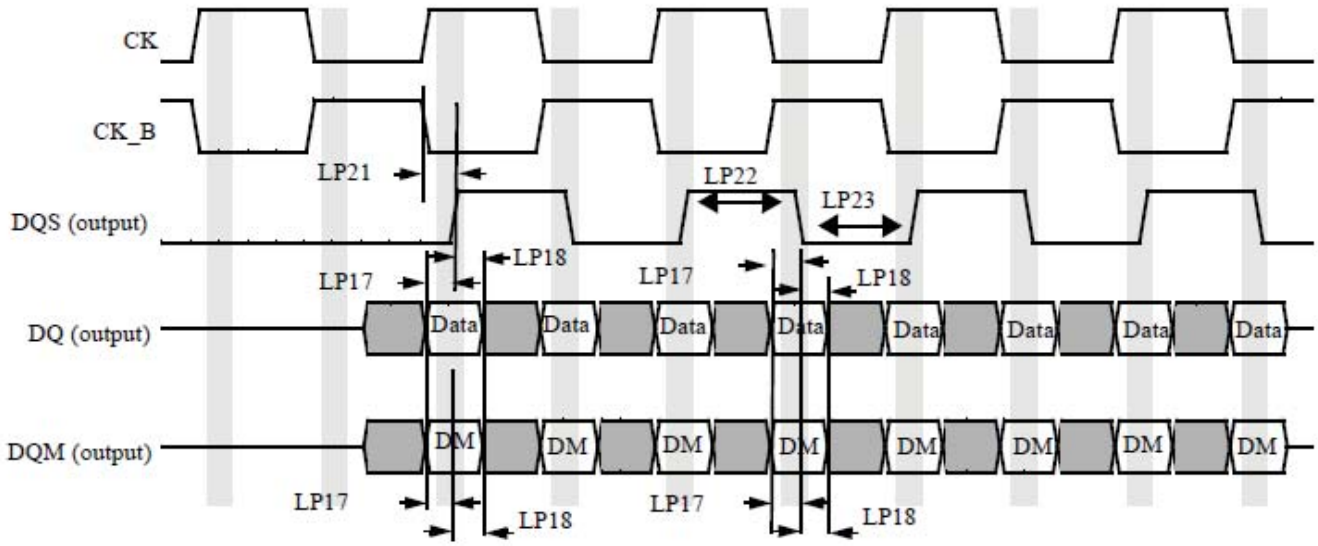


Figure 46. LPDDR3 Write Cycle

Table 59. LPDDR2 Write Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP17	DQ and DQM setup time to DQS (differential strobe)	tDS	220	0.55	ps
LP18	DQ and DQM hold time to DQS (differential strobe)	tDH	220	0.55	ps
LP21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
LP22	DQS high level width	tDQSH	0.4	-	tCK
LP23	DQS low level width	tDQSL	0.4	-	tCK

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.6 Communication interfaces

9.6.1 MediaLB (MLB) DC Characteristics

The section lists the MediaLB 3-pin interface electrical characteristics.

Table 60. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = –6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = –6 mA	2.0	—	V
Input leakage current	$_{IL}$	0 < Vin < VDD	—	±10	µA

1. Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

9.6.2 MediaLB (MLB) Controller AC Timing Electrical Specifications

This section describes the timing electrical information of the MediaLB module.

9.8 Debug specifications

9.8.1 JTAG electricals

Table 76. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	-	25	
	• JTAG and CJTAG	-	25	
	• Serial Wire Debug	-	25	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	20	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	20	—	ns
J4	TCLK rise and fall times	Refer Table 21		ns
J5	Boundary scan input data setup time to TCLK rise	8	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.3	—	ns
J7	TCLK low to boundary scan output data valid	—	17	ns
J8	TCLK low to boundary scan output high-Z	—	17	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.3	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns

NOTE

Input transition (1ns), output load (25 pf) and SRE (000), DSE (111), FSEL(011).

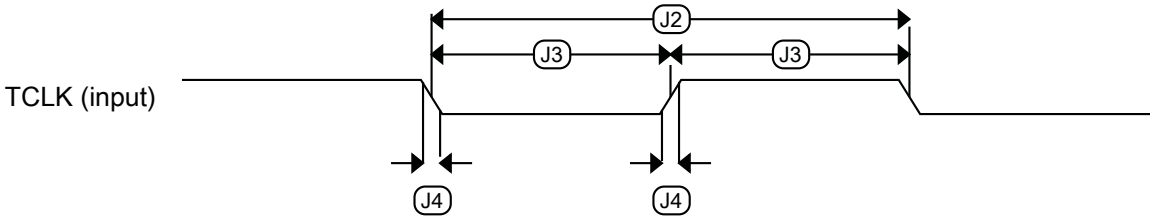


Figure 54. Test clock input timing

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
B14	162	PTB14		PTB14	CAN0_RX	I2C0_SCL		DCU0_ TCON8			DCU1_PCLK	
A14	161	PTB15		PTB15	CAN0_TX	I2C0_SDA		DCU0_ TCON9			VIU_PIX_ CLK	
C14	163	PTB16		PTB16	CAN1_RX	I2C1_SCL		DCU0_ TCON10				
A15	160	PTB17		PTB17	CAN1_TX	I2C1_SDA		DCU0_ TCON11				
B12	171	PTB18		PTB18	SPI0_PCS1	EXT_AUDIO_ MCLK				VIU_DATA9	CCM_OBS0	
C13	167	PTB19		PTB19	SPI0_PCS0					VIU_DATA10	CCM_OBS1	
A13	169	PTB20		PTB20	SPI0_SIN			LCD42		VIU_DATA11	CCM_OBS2	
E12	173	PTB21		PTB21	SPI0_SOUT			LCD43		VIU_DATA12	DCU1_PCLK	
D12	172	PTB22		PTB22	SPI0_SCK				VIU_FID			
V10	61	USB0_GND			USB0_GND							
T10	63	USB0_DP			USB0_DP							
T9	62	USB0_DM			USB0_DM							
W11	60	USB0_VBUS			USB0_VBUS							
Y10	59	USB_DCAP			USB_DCAP							
Y11	64	USB0_ VBUS_ DETECT			USB0_ VBUS_ DETECT							
Y9	—	USB1_GND			USB1_GND							
W9	—	USB1_DP			USB1_DP							
V9	—	USB1_DM			USB1_DM							
W10	—	USB1_VBUS			USB1_VBUS							
U9	—	USB1_ VBUS_ DETECT			USB1_ VBUS_ DETECT							
L4	8	PTC0		PTC0	RMII0_MDC/ MII0_MDC	FTM1CH0	SPI0_PCS3	ESAI_SCKT	SDHC0_CLK	VIU_DATA0	RCON18	
L5	9	PTC1		PTC1	RMII0_MDIO/ MII0_MDC	FTM1CH1	SPI0_PCS2	ESAI_FST	SDHC0_CMD	VIU_DATA1	RCON19	
M5	11	PTC2		PTC2	RMII0_CRS_ DV	SCI1_TX		ESAI_SDO0	SDHC0_ DAT0	VIU_DATA2	RCON20	
M3	12	PTC3		PTC3	RMII0_RXD1/ MII0_RXD[1]	SCI1_RX		ESAI_SDO1	SDHC0_ DAT1	VIU_DATA3	DCU0_R0	
L2	14	PTC4		PTC4	RMII0_RXD0/ MII0_RXD[0]	SCI1_RTS	SPI1_PCS1	ESAI_SDO2/ ESAI_SDI3	SDHC0_ DAT2	VIU_DATA4	DCU0_R1	
M1	15	PTC5		PTC5	RMII0_RXER/ MII0_RXER	SCI1_CTS	SPI1_PCS0	ESAI_SDO3/ ESAI_SDI2	SDHC0_ DAT3	VIU_DATA5	DCU0_G0	
N1	16	PTC6		PTC6	RMII0_TXD1/ MII0_TXD[1]		SPI1_SIN	ESAI_SDO5/ ESAI_SDI0	SDHC0_WP	VIU_DATA6	DCU0_G1	
N2	17	PTC7		PTC7	RMII0_TXD0/ MII0_TXD[0]		SPI1_SOUT	ESAI_SDO4/ ESAI_SDI1		VIU_DATA7	DCU0_B0	

13 Power Supply Pins

13.1 Power Supply Pins

Table 80. Power Supply Pins

Supply Rail Name	364 MAP BGA	176 LQFP (R-series ONLY)	Comment
DECAP_V11_ LDO_OUT	V12	69	On-chip 1.1V LDO output
DECAP_V25_ LDO_OUT	T11	65	On-chip 2.5V LDO output (Intended to supply DRAM IO when required)
FA_VDD	N7	—	Factory Use Only (Connect to VDD, internally bonded in LQFP)
SDRAMC_ VDD1P5	D5, D11, E4, E7, E9, F5, H5, K5	DRAM not supported in LQFP	1.5V DDR3 DRAM Supply (1.2V for LPDDR2)
SDRAMC_ VDD2P5	E6, E10, J5	DRAM not supported in LQFP	2.5V DRAM Supply
USB_DCAP	Y10	59	On-chip 3V LDO output (Intended to be fed by external USB VBUS supply)
USB0_GND	V10	61	
USB1_GND	Y9	USB1 not supported in LQFP	
VADC_AFE_ BANDGAP	U5	41	Video ADC Bandgap Output
VBAT	V14	VBAT not supported in LQFP	On-chip SNVS regulator battery back-up supply option
VDD	G7, G9, G11, G13, H8, H10, H12, H14, J7, J13, K8, K14, L7, L13, M8, M14, N9, N11, N13, P8, P10, P12, P14	2, 22, 48, 85, 102, 125, 136, 174	1.2V Core Supply (Internally Regulated)
VDD33	C12, C15, C18, F18, K3, K17, N3, N17, T17, U16, V8, W18	10, 21, 52, 83, 95, 108, 127, 140, 146, 158, 168	3.3V IO Supply
VDDA33_ADC	V1	31	3.3V Analog To Digital convertor supply
VDD12_AFE	T5	36	1.2V Analog Front End supply for Video ADC
VDDA33_AFE	V3	40	3.3V Analog Front End supply for Video ADC
VDD33_ LDOIN	T12	68	On-chip 2.5V LDO, 1.1V LDO and SNVS regulators input supply
VDDREG	P5	24	On-chip HPREG, LPREG, WBREG and ULPREG regulators input supply
VREFH_ADC	W1	34	ATD High Voltage Reference
VREFL_ADC	U3	33	ATD Low Voltage Reference

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Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTB3	W7	53	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB4	Y7	54	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB5	Y8	55	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB6	W8	56	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB7	D13	166	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB8	J16	121	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB9	J19	123	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB10	B15	159	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB11	D14	164	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB12	E13	165	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB13	D15	156	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB14	B14	162	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB15	A14	161	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB16	C14	163	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB17	A15	160	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB18	B12	171	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB19	C13	167	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB20	A13	169	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB21	E12	173	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB22	D12	172	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB23	A19	141	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB24	A18	142	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB25	B17	149	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB26	A17	150	VDD33	GPIO	ALT3	RCON21	Input	Disabled
PTB27	U8	57	VDD33	GPIO	ALT3	RCON22	Input	Disabled
PTB28	A16	151	VDD33	GPIO	ALT3	RCON23	Input	Disabled
PTC0	L4	8	VDD33	GPIO	ALT7	RCON18	Input	Disabled
PTC1	L5	9	VDD33	GPIO	ALT7	RCON19	Input	Disabled
PTC2	M5	11	VDD33	GPIO	ALT7	RCON20	Input	Disabled
PTC3	M3	12	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC4	L2	14	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC5	M1	15	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC6	N1	16	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC7	N2	17	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC8	N4	18	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC9	T15	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC10	U15	—	VDD33	GPIO	ALT0	GPIO	Disabled	

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Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTC11	P4	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC12	P3	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC13	P1	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC14	R1	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC15	P2	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC16	R3	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC17	R4	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC26	D16	153	VDD33	GPIO	ALT3	RCON24	Input	Disabled
PTC27	E16	154	VDD33	GPIO	ALT3	RCON25	Input	Disabled
PTC28	E15	155	VDD33	GPIO	ALT3	RCON26	Input	Disabled
PTC29	C16	152	VDD33	GPIO	ALT3	RCON27	Input	Disabled
PTC30	T8	58	VDD33	GPIO	ALT3	RCON28	Input	Disabled
PTC31	W5	42	VDD33	GPIO	ALT3	RCON29	Input	Disabled
PTD0	Y17	86	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD1	Y18	87	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD2	V18	88	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD3	Y19	89	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD4	W19	90	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD5	W20	91	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD6	V20	92	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD7	V19	93	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD8	U17	94	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD9	U18	97	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD10	U20	98	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD11	T20	99	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD12	T19	100	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD13	T18	101	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD16	D20	133	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD17	E20	132	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD18	E18	131	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD19	F16	130	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD20	F17	129	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD21	F19	128	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD22	F20	126	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD23	G20	124	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD24	G19	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD25	G18	—	VDD33	GPIO	ALT0	GPIO	Disabled	

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Table 82. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Removed Temperature Voltage Monitor section to security RM • Updated VideoADC Specifications table
Rev 5	April 2013	Updated pin muxing table with the following changes: • Added MII0 including M AC0.TXDATA[2], MAC0.TXDATA[3], MAC0.RXDATA[2], MAC0.RXDATA[3] , MAC0.TXERR, MAC0.TXCLK, MAC0.RXCLK, MAC0.COL, MAC0.CRS • Following signals muxed on same RMII0 Pins : MII0_MDC, MII0_MDC, MII0_RXD[1], MII0_RXD[0], MII0_RXER, MII0_TXD[1], MII0_TXD[0], MII0_TXEN • Replaced FB_ALE with FB_MUXED_ALE, FB_CS4_b with FB_MUXED_TSIZ0, FB_TSIZ1 with FB_MUXED_TSIZ1, FB_TBST_b with FB_MUXED_TBST_b, FB_BE0_b with FB_MUXED_BE0_b • Removed RCON18,19,20 • Replaced ESAI_SDO2 with ESAI_SDO2/ESAI_SDI3 Replaced ESAI_SDO3 with ESAI_SDO3/ ESAI_SDI2 Replaced ESAI_SDI0 with ESAI_SDO5/ESAI_SDI0 Replaced ESAI_SDI1 with ESAU_SDO4/ESAI_SDI1 • CKO1 additionally muxed at PAD40
Rev 5	May 2013	In the Features, minor editorial updates Added Part Number Format figure Updated the Fields table as per the device part numbers Added Part Numbers table Added External NPN Ballast section In the LVD Dig Electrical Specs, minimum value of Upper Voltage Threshold and Lower Voltage threshold In the FlexBus timing specifications table, clarified the Frequency of operation In the Power consumption, filled TBDs. Updated footnotes

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