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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 64MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, LVD, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 16KB (8K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 5.5V |
| Data Converters | A/D 24x10b; D/A 1x5b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18f24k40t-i-ss |

## Digital Peripherals (Continued)

- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate CRC over any portion of Flash or EEPROM
  - High-speed or background operation
- Hardware Limit Timer (TMR2/4/6+HLT):
  - Hardware monitoring and Fault detection
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O
- Data Signal Modulator (DSM)

## Analog Peripherals

- 10-Bit Analog-to-Digital Converter with Computation (ADC[2]):
  - 24 external channels
  - Conversion available during Sleep
  - Four internal analog channels
  - Internal and external trigger options
  - Automated math functions on input signals:
    - averaging, filter calculations, oversampling and threshold comparison
- Hardware Capacitive Voltage Divider (CVD) Support:
  - 8-bit precharge timer
  - Adjustable sample and hold capacitor array
  - Guard ring digital output drive
- Zero-Cross Detect (ZCD):
  - Detect when AC signal on pin crosses ground
- 5-Bit Digital-to-Analog Converter (DAC):
  - Output available externally
  - Programmable 5-bit voltage (% of $V_{DD}$)
  - Internal connections to comparators, Fixed Voltage Reference and ADC
- Two Comparators (CMP):
  - Four external inputs
  - External output via PPS
- Fixed Voltage Reference (FVR) module:
  - 1.024V, 2.048V and 4.096V output levels

## Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequency range up to 64 MHz
  - ±1% at calibration
- 32 kHz Low-Power Internal Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External Oscillator Block:
  - Three crystal/resonator modes
  - 4x PLL with external sources
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops
- Oscillator Start-up Timer (OST)

## Programming/Debug Features

- In-Circuit Debug Integrated On-Chip
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins

### 4.3.1.5 Secondary Oscillator

The secondary oscillator is a separate oscillator block that can be used as an alternate system clock source. The secondary oscillator is optimized for 32.768 kHz, and can be used with an external crystal oscillator connected to the SOSCI and SOSCO device pins, or an external clock source connected to the SOSCIN pin. The secondary oscillator can be selected during run-time using clock switching. Refer to **Section 4.4 "Clock Switching"** for more information.

### FIGURE 4-5: QUARTZ CRYSTAL OPERATION (SECONDARY OSCILLATOR)
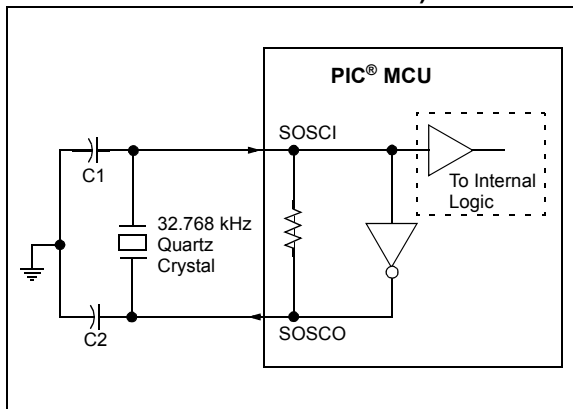


**Note 1:** Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

**2:** Always verify oscillator performance over the V$_{DD}$ and temperature range that is expected for the application.

**3:** For oscillator design assistance, reference the following Microchip Application Notes:

- AN826, "*Crystal Oscillator Basics and Crystal Selection for PIC® and PIC® Devices*" (DS00826)

- AN849, "*Basic PIC® Oscillator Design*" (DS00849)

- AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943)

- AN949, "*Making Your Oscillator Work*" (DS00949)

- TB097, "*Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS*" (DS91097)

- AN1288, "*Design Practices for Low-Power External Oscillators*" (DS01288)

### 4.3.2 INTERNAL CLOCK SOURCES

The device may be configured to use the internal oscillator block as the system clock by performing one of the following actions:

- Program the RSTOSC<2:0> bits in Configuration Words to select the INTOSC clock source, which will be used as the default system clock upon a device Reset.
- Write the NOSC<2:0> bits in the OSCCON1 register to switch the system clock source to the internal oscillator during run-time. See **Section 4.4 "Clock Switching"** for more information.

In INTOSC mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT is available for general purpose I/O or CLKOUT.

The function of the OSC2/CLKOUT pin is determined by the $\overline{\text{CLKOUTEN}}$ bit in Configuration Words.

The internal oscillator block has two independent oscillators that can produce two internal system clock sources.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory-calibrated and operates from 1 to 64 MHz. The frequency of HFINTOSC can be selected through the OSCFRQ Frequency Selection register, and fine-tuning can be done via the OSCTUNE register.

2. The **LFINTOSC** (Low-Frequency Internal Oscillator) is factory-calibrated and operates at 31 kHz.

## 8.3 Power-on Reset (POR)

The POR circuit holds the device in Reset until $V_{DD}$ has reached an acceptable level for minimum operation. Slow rising $V_{DD}$, fast operating speeds or analog performance may require greater than minimum $V_{DD}$. The PWRT, BOR or $\overline{MCLR}$ features can be used to extend the start-up period until all device operation conditions have been met.

## 8.4 Brown-out Reset (BOR)

The BOR circuit holds the device in Reset when $V_{DD}$ reaches a selectable minimum level. Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

The Brown-out Reset module has four operating modes controlled by the BOREN<1:0> bits in Configuration Words. The four operating modes are:

- BOR is always on
- BOR is off when in Sleep
- BOR is controlled by software
- BOR is always off

Refer to Table 8-1 for more information.

The Brown-out Reset voltage level is selectable by configuring the BORV<1:0> bits in Configuration Words.

A $V_{DD}$ noise rejection filter prevents the BOR from triggering on small events. If $V_{DD}$ falls below $V_{BOR}$ for a duration greater than parameter $T_{BORDC}$, the device will reset. See Table 37-11 for more information.

### 8.4.1 BOR IS ALWAYS ON

When the BOREN bits of Configuration Words are programmed to '11', the BOR is always on. The device start-up will be delayed until the BOR is ready and $V_{DD}$ is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

### 8.4.2 BOR IS OFF IN SLEEP

When the BOREN bits of Configuration Words are programmed to '10', the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and $V_{DD}$ is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

### 8.4.3 BOR CONTROLLED BY SOFTWARE

When the BOREN bits of Configuration Words are programmed to '01', the BOR is controlled by the SBOREN bit of the BORCON register. The device start-up is not delayed by the BOR ready condition or the $V_{DD}$ level.

BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the BORRDY bit of the BORCON register.

BOR protection is unchanged by Sleep.

### 8.4.4 BOR AND BULK ERASE

BOR is forced ON during PFM Bulk Erase operations to make sure that the system code protection cannot be compromised by reducing $V_{DD}$.

During Bulk Erase, the BOR is enabled at 2.45V for F and LF devices, even if it is configured to some other value. If $V_{DD}$ falls, the erase cycle will be aborted, but the device will not be reset.

## 10.0 MEMORY ORGANIZATION

There are three types of memory in PIC18 enhanced microcontroller devices:

• Program Memory
• Data RAM
• Data EEPROM

As Harvard architecture devices, the data and program memories use separate buses; this allows for concurrent access of the two memory spaces. The data EEPROM, for practical purposes, can be regarded as a peripheral device, since it is addressed and accessed through a set of control registers.

Additional detailed information on the operation of the Program Flash Memory and Data EEPROM Memory is provided in **Section 11.0 "Nonvolatile Memory (NVM) Control"**.

## 10.1 Program Memory Organization

PIC18 microcontrollers implement a 21-bit program counter, which is capable of addressing a 2 Mbyte program memory space. Accessing a location between the upper boundary of the physically implemented memory and the 2 Mbyte address will return all '0's (a NOP instruction).

These devices contains the following:

• PIC18(L)F24K40: 16 Kbytes of Flash memory, up to 8,192 single-word instructions
• PIC18(L)F25K40: 32 K bytes of Flash memory, up to 16,384 single-word instructions

PIC18 devices have two interrupt vectors. The Reset vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

| Note: | For memory information on this family of devices, see Table 10-1 and Table 10-2. |
|---|---|

**FIGURE 10-5:** **USE OF THE BANK SELECT REGISTER (DIRECT ADDRESSING)**



**Note 1:** The Access RAM bit of the instruction can be used to force an override of the selected bank (BSR<3:0>) to the registers of the Access Bank.

**2:** The MOVFF instruction embeds the entire 12-bit address in the instruction.
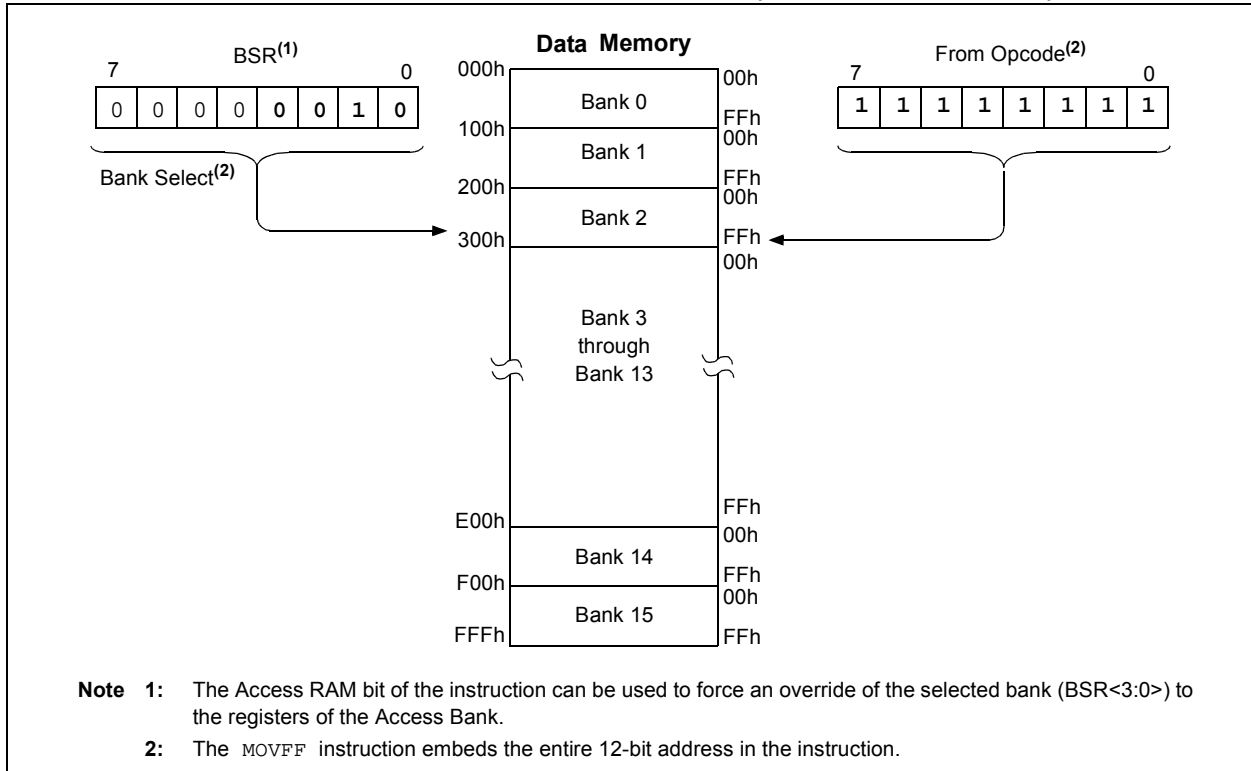
**TABLE 10-5:   REGISTER FILE SUMMARY FOR PIC18(L)F24/25K40 DEVICES (CONTINUED)**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR |
|---|---|---|---|---|---|---|---|---|---|---|
| F74h | CRCDATL | DATA<7:0> | | | | | | | | xxxxxxxx |
| F73h | ADFLTRH | ADFLTRH<15:8> | | | | | | | | xxxxxxxx |
| F72h | ADFLTRL | ADFLTRL<7:0> | | | | | | | | xxxxxxxx |
| F71h | ADACCH | ADACCH<15:8> | | | | | | | | xxxxxxxx |
| F70h | ADACCL | ADACCL<7:0> | | | | | | | | xxxxxxxx |
| F6Fh | ADERRH | ADERRH<15:8> | | | | | | | | 00000000 |
| F6Eh | ADERRL | ADERRL<7:0> | | | | | | | | 00000000 |
| F6Dh | ADUTHH | ADUTHH<15:8> | | | | | | | | 00000000 |
| F6Ch | ADUTHL | ADUTHL<7:0> | | | | | | | | 00000000 |
| F6Bh | ADLTHH | ADLTHH<15:8> | | | | | | | | 00000000 |
| F6Ah | ADLTHL | ADLTHL<7:0> | | | | | | | | 00000000 |
| F69h | ADSTPTH | ADSTPTH<15:8> | | | | | | | | 00000000 |
| F68h | ADSTPTL | ADSTPTL<7:0> | | | | | | | | 00000000 |
| F67h | ADCNT | ADCNT<7:0> | | | | | | | | 00000000 |
| F66h | ADRPT | ADRPT<7:0> | | | | | | | | 00000000 |
| F65h | ADSTAT | ADAOV | ADUTHR | ADLTHR | ADMATH | — | ADSTAT<2:0> | | | 0000-000 |
| F64h | ADRESH | ADRESH<7:0> | | | | | | | | 00000000 |
| F63h | ADRESL | ADRESL<7:0> | | | | | | | | 00000000 |
| F62h | ADPREVH | ADPREVH<15:8> | | | | | | | | 00000000 |
| F61h | ADPREVL | ADPREVL<7:0> | | | | | | | | 00000000 |
| F60h | ADCON0 | ADON | ADCONT | — | ADSC | — | ADFM | — | ADGO | 00-000-0 |
| F5Fh | ADPCH | — | — | ADPCH<5:0> | | | | | | --000000 |
| F5Eh | ADPRE | ADPRE<7:0> | | | | | | | | 00000000 |
| F5Dh | ADCAP | — | — | — | ADCAP<4:0> | | | | | ---00000 |
| F5Ch | ADACQ | ADACQ<7:0> | | | | | | | | 00000000 |
| F5Bh | ADCON3 | — | ADCALC<2:0> | | | ADSOI | ADTMD<2:0> | | | -0000000 |
| F5Ah | ADCON2 | ADPSIS | ADCRS<2:0> | | | ADACLR | ADMD<2:0> | | | 00000000 |
| F59h | ADCON1 | ADPPOL | ADIPEN | ADGPOL | — | — | — | — | ADDSEN | 000----0 |
| F58h | ADREF | — | — | — | ADNREF | — | — | ADPREF<1:0> | | ---0--00 |
| F57h | ADCLK | — | — | ADCS<5:0> | | | | | | --000000 |
| F56h | ADACT | — | — | — | ADACT<4:0> | | | | | ---00000 |
| F55h | MDCARH | — | — | — | — | — | CHS<2:0> | | | -----000 |
| F54h | MDCARL | — | — | — | — | — | CLS<2:0> | | | -----000 |
| F53h | MDSRC | — | — | — | — | SRCS<3:0> | | | | ----0000 |
| F52h | MDCON1 | — | — | CHPOL | CHSYNC | — | — | CLPOL | CLSYNC | --00--00 |
| F51h | MDCON0 | EN | — | **OUT** | **OPOL** | — | — | — | MDBIT | 0-00---0 |
| F50h | SCANTRIG | — | — | — | — | TSEL<3:0> | | | | ----0000 |
| F4Fh | SCANCON0 | SCANEN | SCANGO | BUSY | INVALID | INTM | — | MODE<1:0> | | 00000-00 |
| F4Eh | SCANHADRU | — | — | HADR<21:16> | | | | | | --111111 |

**Legend:**   x = unknown, u = unchanged, — = unimplemented, q = value depends on condition
**Note    1:**   Not available on LF devices.

## REGISTER 14-15: PIE5: PERIPHERAL INTERRUPT ENABLE REGISTER 5

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|-----|-----|-----|-----|-----|---------|---------|---------|
| — | — | — | — | — | TMR5GIE | TMR3GIE | TMR1GIE |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-3     **Unimplemented:** Read as '0'

bit 2       **TMR5GIE:** TMR5 Gate Interrupt Enable bit
            1 = Enabled
            0 = Disabled

bit 1       **TMR3GIE:** TMR3 Gate Interrupt Enable bit
            1 = Enabled
            0 = Disabled

bit 0       **TMR1GIE:** TMR1 Gate Interrupt Enable bit
            1 = Enabled
            0 = Disabled

## 15.0   I/O PORTS

**TABLE 15-1:   PORT AVAILABILITY PER DEVICE**

| Device | PORTA | PORTB | PORTC | PORTD | PORTE |
|--------|-------|-------|-------|-------|-------|
| PIC18(L)F24/25K40 | ● | ● | ● | | ● |

Each port has eight registers to control the operation. These registers are:

- PORTx registers (reads the levels on the pins of the device)
- LATx registers (output latch)
- TRISx registers (data direction)
- ANSELx registers (analog select)
- WPUx registers (weak pull-up)
- INLVLx (input level control)
- SLRCONx registers (slew rate control)
- ODCONx registers (open-drain control)

Most port pins share functions with device peripherals, both analog and digital. In general, when a peripheral is enabled on a port pin, that pin cannot be used as a general purpose output; however, the pin can still be read.

The Data Latch (LATx registers) is useful for read-modify-write operations on the value that the I/O pins are driving.

A write operation to the LATx register has the same effect as a write to the corresponding PORTx register. A read of the LATx register reads of the values held in the I/O PORT latches, while a read of the PORTx register reads the actual I/O pin value.

Ports that support analog inputs have an associated ANSELx register. When an ANSELx bit is set, the digital input buffer associated with that bit is disabled.

Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 15-1.

**FIGURE 15-1:    GENERIC I/O PORT OPERATION**
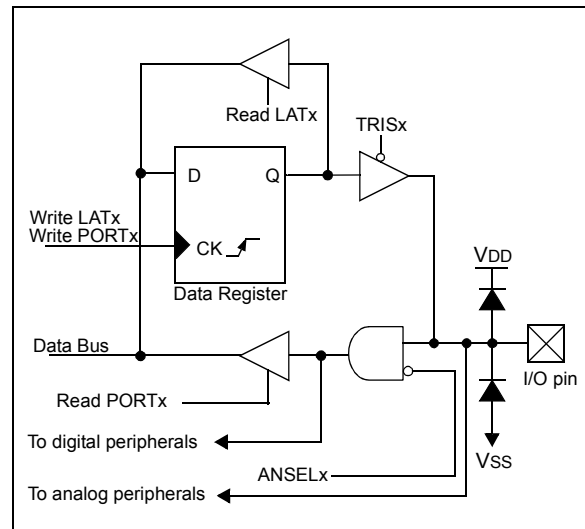
## 21.2    Register Definitions: CCP Control

Long bit name prefixes for the CCP peripherals are shown in Table 21-2. Refer to **Section 1.4.2.2 "Long Bit Names"** for more information.

**TABLE 21-2:**

| Peripheral | Bit Name Prefix |
|------------|-----------------|
| CCP1 | CCP1 |
| CCP2 | CCP2 |

**REGISTER 21-1:    CCPxCON: CCPx CONTROL REGISTER**

| R/W-0/0 | U-0 | R-x | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---------|-----|-----|---------|---------|---------|---------|---------|
| EN | — | OUT | FMT | MODE<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared          x = Bit is unknown |

bit 7         **EN:** CCP Module Enable bit
              1 =  CCP is enabled
              0 =  CCP is disabled

bit 6         **Unimplemented:** Read as '0'

bit 5         **OUT:** CCPx Output Data bit (read-only)

bit 4         **FMT:** CCPW (pulse-width) Alignment bit
              <u>MODE = Capture mode:</u>
              Unused
              <u>MODE = Compare mode:</u>
              Unused
              <u>MODE = PWM mode:</u>
              1 =  Left-aligned format
              0 =  Right-aligned format

**Note  1:**  The set and clear operations of the Compare mode are reset by setting MODE = 4'b0000 or EN = 0.
     **2:**  When MODE = 0001 or 1011, then the timer associated with the CCP module is cleared. TMR1 is the default selection for the CCP module, so it is used for indication purpose only.

## 22.2 Register Definitions: PWM Control

Long bit name prefixes for the PWM peripherals are shown in Table 22-3. Refer to **Section 1.4.2.2 "Long Bit Names"** for more information.

**TABLE 22-3:**

| Peripheral | Bit Name Prefix |
|---|---|
| PWM3 | PWM3 |
| PWM4 | PWM4 |

**REGISTER 22-1: PWMxCON: PWM CONTROL REGISTER**

| R/W-0/0 | U-0 | R-0/0 | R/W-0/0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| EN | — | OUT | POL | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7     **EN:** PWM Module Enable bit
　　　　1 = PWM module is enabled
　　　　0 = PWM module is disabled

bit 6     **Unimplemented:** Read as '0'

bit 5     **OUT:** PWM Module Output Level When Bit is Read

bit 4     **POL:** PWM Output Polarity Select bit
　　　　1 = PWM output is inverted
　　　　0 = PWM output is normal

bit 3-0   **Unimplemented:** Read as '0'

**FIGURE 24-3:** **SIMPLIFIED CWG BLOCK DIAGRAM (PUSH-PULL MODE, MODE<2:0> = 101)**
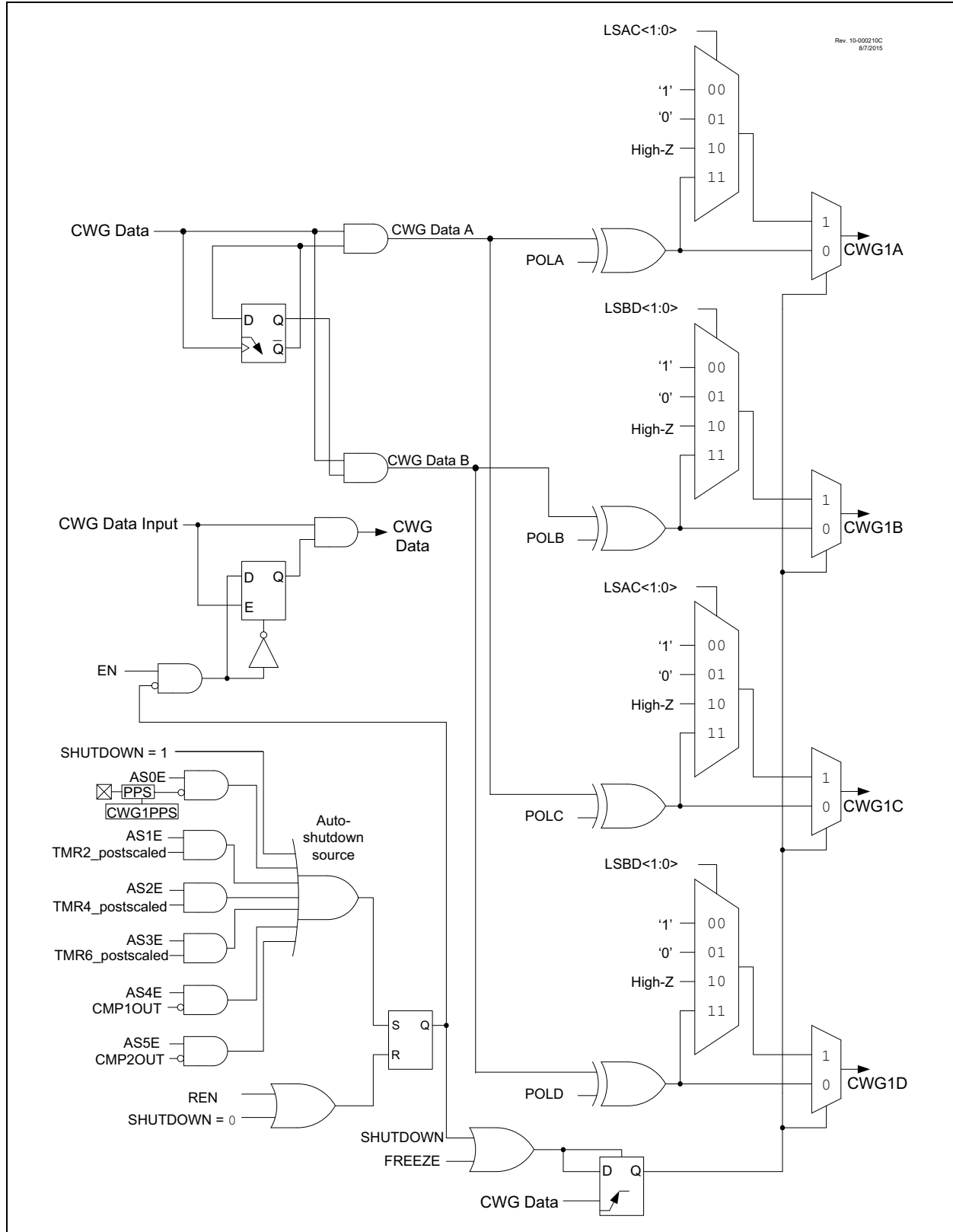
## 26.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP1)MODULE

### 26.1 MSSP Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The PIC18(L)F24/25K40 devices have one MSSP module that can operate in one of two modes:

• Serial Peripheral Interface (SPI)
• Inter-Integrated Circuit (I$^2$C)

The SPI interface supports the following modes and features:

• Master mode
• Slave mode
• Clock Parity
• Slave Select Synchronization (Slave mode only)
• Daisy-chain connection of slave devices

The I$^2$C interface supports the following modes and features:

• Master mode
• Slave mode
• Byte NACKing (Slave mode)
• Limited multi-master support
• 7-bit and 10-bit addressing
• Start and Stop interrupts
• Interrupt masking
• Clock stretching
• Bus collision detection
• General call address matching
• Address masking
• Address Hold and Data Hold modes
• Selectable SDA hold times

### 26.2 SPI Mode Overview

The Serial Peripheral Interface (SPI) bus is a synchronous serial data communication bus that operates in Full-Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a Chip Select known as Slave Select.

The SPI bus specifies four signal connections:

• Serial Clock (SCK)
• Serial Data Out (SDO)
• Serial Data In (SDI)
• Slave Select ($\overline{SS}$)

Figure 26-1 shows the block diagram of the MSSP module when operating in SPI mode.

**FIGURE 26-14:** I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 0, DHEN = 0)



**PIC18(L)F24/25K40**
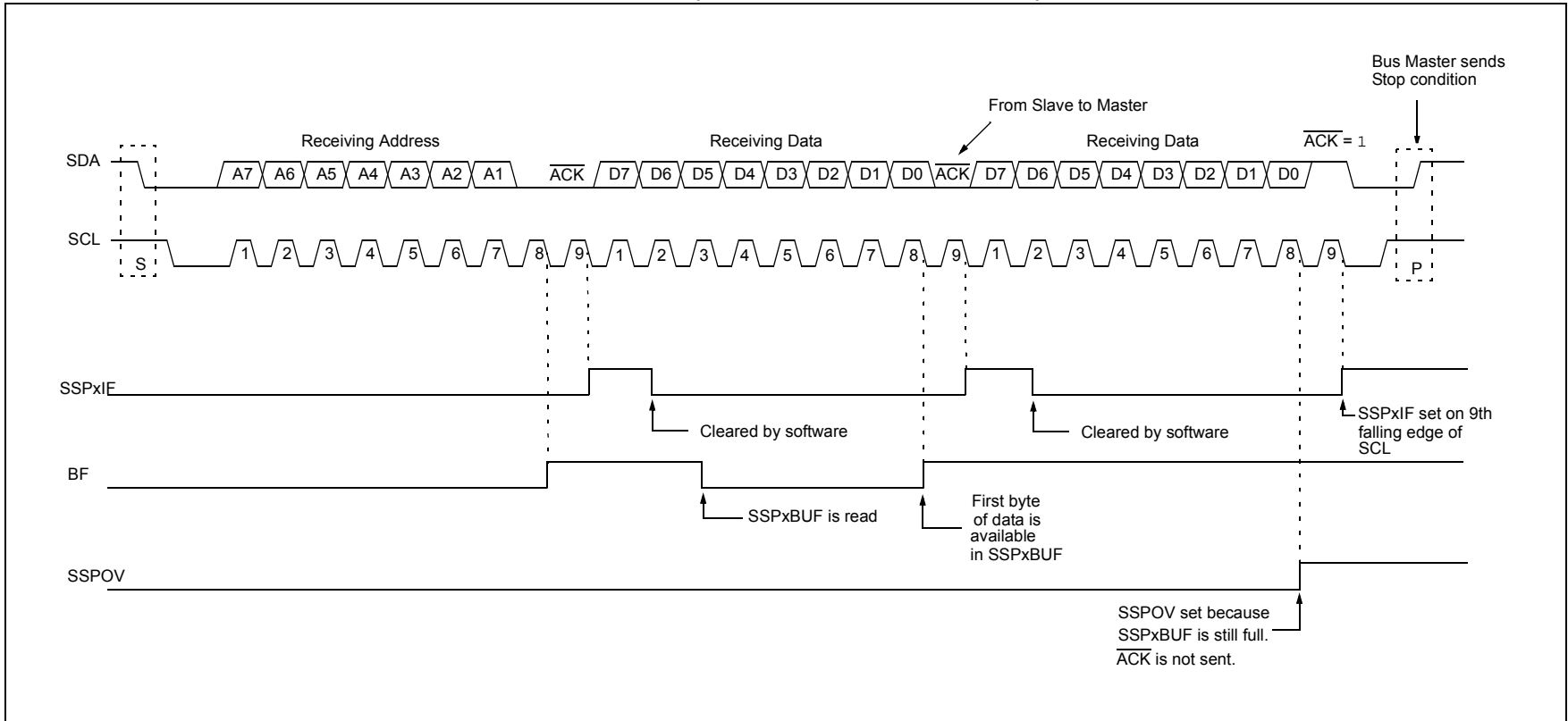
### 26.10.7    I²C Master Mode Reception

Master mode reception (Figure 26-29) is enabled by programming the Receive Enable bit, RCEN bit of the SSP1CON2 register.

> **Note:** The MSSP module must be in an Idle state before the RCEN bit is set or the RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPxBUF, the BF flag bit is set, the SSPxIF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSPxCON2 register.

#### 26.10.7.1    BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPxBUF from SSPSR. It is cleared when the SSPxBUF register is read.

#### 26.10.7.2    SSPOV Status Flag

In receive operation, the SSPOV bit is set when eight bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

#### 26.10.7.3    WCOL Status Flag

If the user writes the SSPxBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

### 26.10.7.4    Typical Receive Sequence:

1. The user generates a Start condition by setting the SEN bit of the SSPxCON2 register.
2. SSPxIF is set by hardware on completion of the Start.
3. SSPxIF is cleared by software.
4. User writes SSPxBUF with the slave address to transmit and the R/$\overline{\text{W}}$ bit set.
5. Address is shifted out the SDA pin until all eight bits are transmitted. Transmission begins as soon as SSPxBUF is written to.
6. The MSSP module shifts in the $\overline{\text{ACK}}$ bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
7. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
8. User sets the RCEN bit of the SSPxCON2 register and the master clocks in a byte from the slave.
9. After the eighth falling edge of SCL, SSPxIF and BF are set.
10. Master clears SSPxIF and reads the received byte from SSPUF, clears BF.
11. Master sets the $\overline{\text{ACK}}$ value sent to slave in the ACKDT bit of the SSPxCON2 register and initiates the $\overline{\text{ACK}}$ by setting the ACKEN bit.
12. Master's $\overline{\text{ACK}}$ is clocked out to the slave and SSPxIF is set.
13. User clears SSPxIF.
14. Steps 8-13 are repeated for each received byte from the slave.
15. Master sends a not $\overline{\text{ACK}}$ or Stop to end communication.

### 27.2.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCxSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCxREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCxSTA register which resets the EUSART. Clearing the CREN bit of the RCxSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

> **Note:** If all receive characters in the receive FIFO have framing errors, repeated reads of the RCxREG will not clear the FERR bit.

### 27.2.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCxSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCxSTA register or by resetting the EUSART by clearing the SPEN bit of the RCxSTA register.

### 27.2.2.6 Receiving 9-Bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCxSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCxSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCxREG.

### 27.2.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCxSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCxIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

**REGISTER 31-30: ADUTHH: ADC UPPER THRESHOLD HIGH BYTE REGISTER**

| R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x |
|---|---|---|---|---|---|---|---|
| | | | ADUTH<15:8> | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-0    **ADUTH<15:8>**: ADC Upper Threshold MSB. ADLTH and ADUTH are compared with ADERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.

**REGISTER 31-31: ADUTHL: ADC UPPER THRESHOLD LOW BYTE REGISTER**

| R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x | R/W-x/x |
|---|---|---|---|---|---|---|---|
| | | | ADUTH<7:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-0    **ADUTH<7:0>**: ADC Upper Threshold LSB. ADLTH and ADUTH are compared with ADERR to set the ADUTHR and ADLTHR bits of ADSTAT. Depending on the setting of ADTMD, an interrupt may be triggered by the results of this comparison.

## 32.2    Register Definitions: Comparator Control

Long bit name prefixes for the Comparators are shown in Table 32-1. Refer to **Section 1.4.2.2 "Long Bit Names"** for more information.

**TABLE 32-1:**

| Peripheral | Bit Name Prefix |
|:---:|:---:|
| C1 | C1 |
| C2 | C2 |

**REGISTER 32-1:    CMxCON0: COMPARATOR x CONTROL REGISTER 0**

| R/W-0/0 | R-0/0 | U-0 | R/W-0/0 | U-0 | U-1 | R/W-0/0 | R/W-0/0 |
|:---:|:---:|:---:|:---:|:---:|:---:|:---:|:---:|
| EN | OUT | — | POL | — | — | HYS | SYNC |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared    x = Bit is unknown |

bit 7        **EN:** Comparator Enable bit

1 =   Comparator is enabled
0 =   Comparator is disabled and consumes no active power

bit 6        **OUT:** Comparator Output bit

If POL = 0 (non-inverted polarity):
1 =   CxVP > CxVN
0 =   CxVP < CxVN
If POL = 1 (inverted polarity):
1 =   CxVP < CxVN
0 =   CxVP > CxVN

bit 5        **Unimplemented:** Read as '0'

bit 4        **POL:** Comparator Output Polarity Select bit

1 =   Comparator output is inverted
0 =   Comparator output is not inverted

bit 3        **Unimplemented:** Read as '0'

bit 2        **Unimplemented:** Read as '1'

bit 1        **HYS:** Comparator Hysteresis Enable bit

1 =   Comparator hysteresis enabled
0 =   Comparator hysteresis disabled

bit 0        **SYNC:** Comparator Output Synchronous Mode bit

1 =   Comparator output to Timer1/3/5 and I/O pin is synchronous to changes on Timer1 clock source.
0 =   Comparator output to Timer1/3/5 and I/O pin is asynchronous
        Output updated on the falling edge of Timer1/3/5 clock source.

**REGISTER 33-2:    HLVDCON0: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER 0**

| R/W-0/0 | U-0 | R-x | R-x | U-0 | U-0 | R/W-0/0 | R/W-0/0 |
|---------|-----|-----|-----|-----|-----|---------|---------|
| EN | — | OUT | RDY | — | — | INTH | INTL |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7    **EN:** High/Low-voltage Detect Power Enable bit

1 =   Enables HLVD, powers up HLVD circuit and supporting reference circuitry
0 =   Disables HLVD, powers down HLVD and supporting circuitry

bit 6    **Unimplemented:** Read as '0'

bit 5    **OUT:** HLVD Comparator Output bit

1 =   Voltage ≤ selected detection limit (HLVDL<3:0>)
0 =   Voltage ≥ selected detection limit (HLVDL<3:0>)

bit 4    **RDY:** Band Gap Reference Voltages Stable Status Flag bit

1 =   Indicates HLVD Module is ready and output is stable
0 =   Indicates HLVD Module is not ready

bit 3-2    **Unimplemented:** Read as '0'

bit 1    **INTH:** HLVD Positive going (High Voltage) Interrupt Enable

1 =   HLVDIF will be set when voltage ≥ selected detection limit (HLVDSEL<3:0>)
0 =   HLVDIF will not be set

bit 0    **INTL:** HLVD Negative going (Low Voltage) Interrupt Enable

1 =   HLVDIF will be set when voltage ≤ selected detection limit (HLVDSEL<3:0>)
0 =   HLVDIF will not be set

**TABLE 33-2:    REGISTERS ASSOCIATED WITH HIGH/LOW-VOLTAGE DETECT MODULE**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|------|-------|-------|-------|-------|-------|-------|-------|-------|------------------|
| HLVDCON0 | EN | — | OUT | RDY | — | — | INTH | INTL | 476 |
| HLVDCON1 | — | — | — | — | SEL<3:0> | | | | 475 |
| INTCON | GIE/GIEH | PEIE/GIEL | IPEN | — | — | INT2EDG | INT1EDG | INT0EDG | 166 |
| PIR2 | HLVDIF | ZCDIF | — | — | — | — | C2IF | C1IF | 169 |
| PIE2 | HLVDIE | ZCDIE | — | — | — | — | C2IE | C1IE | 177 |
| IPR2 | HLVDIP | ZCDIP | — | — | — | — | C2IP | C1IP | 185 |
| PMD0 | SYSCMD | FVRMD | HLVDMD | CRCMD | SCANMD | NVMMD | CLKRMD | IOCMD | 64 |

**Legend:**    — = unimplemented, read as '0'. Shaded cells are unused by the HLVD module.
**Note   1:**    PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes.
When disabled, these bits read as '0'.

## TABLE 37-15: COMPARATOR SPECIFICATIONS

| Operating Conditions (unless otherwise stated) $V_{DD}$ = 3.0V, $T_A$ = 25°C | | | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Sym. | Characteristics | Min. | Typ. | Max. | Units | Comments |
| CM01 | $V_{IOFF}$ | Input Offset Voltage | — | — | ±30 | mV | $V_{ICM}$ = $V_{DD}$/2 |
| CM02 | $V_{ICM}$ | Input Common Mode Range | GND | — | $V_{DD}$ | V | |
| CM03 | CMRR | Common Mode Input Rejection Ratio | — | 50 | — | dB | |
| CM04 | $V_{HYST}$ | Comparator Hysteresis | 10 | 25 | 40 | mV | |
| CM05 | $T_{RESP}$[1] | Response Time, Rising Edge | — | 300 | 600 | ns | |
| | | Response Time, Falling Edge | — | 220 | 500 | ns | |

   * These parameters are characterized but not tested.

**Note 1:** Response time measured with one comparator input at $V_{DD}$/2, while the other input transitions from $V_{SS}$ to $V_{DD}$.

    **2:** A mode change includes changing any of the control register values, including module enable.

## TABLE 37-16: 5-BIT DAC SPECIFICATIONS

| Standard Operating Conditions (unless otherwise stated) $V_{DD}$ = 3.0V, $T_A$ = 25°C | | | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Sym. | Characteristics | Min. | Typ. | Max. | Units | Comments |
| DSB01 | $V_{LSB}$ | Step Size | — | ($V_{DACREF+}$ -$V_{DACREF-}$) / 32 | — | V | |
| DSB01 | $V_{ACC}$ | Absolute Accuracy | — | — | ± 0.5 | LSb | |
| DSB03* | $R_{UNIT}$ | Unit Resistor Value | — | 5000 | — | Ω | |
| DSB04* | $T_{ST}$ | Settling Time[1] | — | — | 10 | µs | |

   * These parameters are characterized but not tested.

   † Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Settling time measured while DACR<4:0> transitions from '00000' to '01111'.

## TABLE 37-17: FIXED VOLTAGE REFERENCE (FVR) SPECIFICATIONS

| Standard Operating Conditions (unless otherwise stated) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Param. No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
| FVR01 | $V_{FVR1}$ | 1x Gain (1.024V) | -4 | — | +4 | % | $V_{DD} \geq$ 2.5V, -40°C to 85°C |
| FVR02 | $V_{FVR2}$ | 2x Gain (2.048V) | -4 | — | +4 | % | $V_{DD} \geq$ 2.5V, -40°C to 85°C |
| FVR03 | $V_{FVR4}$ | 4x Gain (4.096V) | -5 | — | +5 | % | $V_{DD} \geq$ 4.75V, -40°C to 85°C |
| FVR04 | $T_{FVRST}$ | FVR Start-up Time | — | 25 | — | us | |

## TABLE 37-18: ZERO CROSS DETECT (ZCD) SPECIFICATIONS

| Standard Operating Conditions (unless otherwise stated) $V_{DD}$ = 3.0V, $T_A$ = 25°C | | | | | | | |
|---|---|---|---|---|---|---|---|
| Param. No. | Sym. | Characteristics | Min | Typ† | Max | Units | Comments |
| ZC01 | $V_{PINZC}$ | Voltage on Zero Cross Pin | — | 0.75 | — | V | |
| ZC02 | $I_{ZCD\_MAX}$ | Maximum source or sink current | — | — | 600 | µA | |
| ZC03 | $T_{RESPH}$ | Response Time, Rising Edge | — | 1 | — | µs | |
| | $T_{RESPL}$ | Response Time, Falling Edge | — | 1 | — | µs | |

   † Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]**

| Note: | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|

TOP VIEW

SEATING PLANE

BOTTOM VIEW
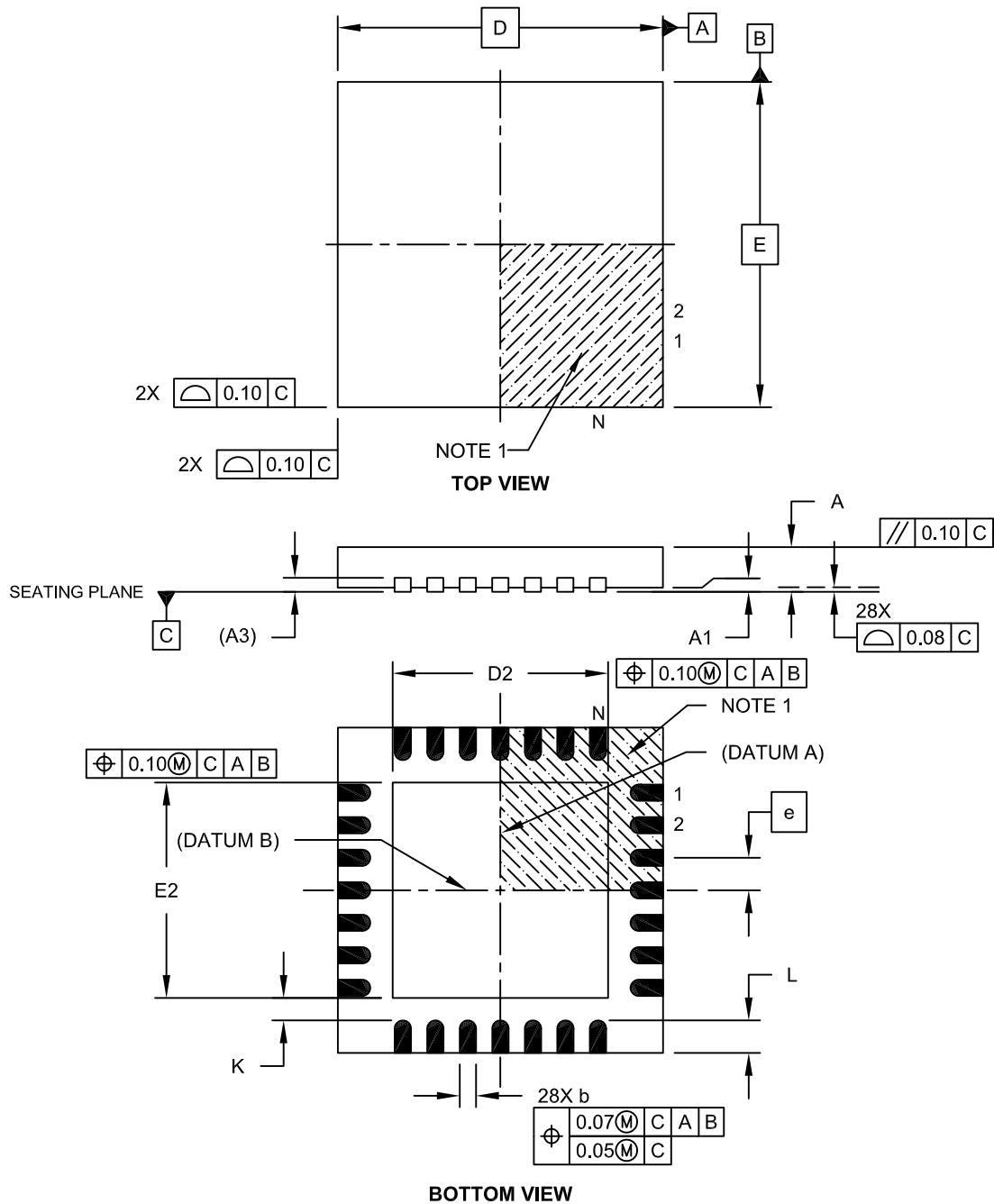
Microchip Technology Drawing  C04-152A Sheet 1 of 2

**Preliminary**