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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 35x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f25k40-e-ss

1.0 DEVICE OVERVIEW

This document contains device specific information for the following devices:

- PIC18F24K40
- PIC18LF24K40
- PIC18F25K40
- PIC18LF25K40

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Program Flash Memory. In addition to these features, the PIC18(L)F2x/4xK40 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

1.1 New Core Features

1.1.1 XLP TECHNOLOGY

All of the devices in the PIC18(L)F2x/4xK40 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the secondary oscillator or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Peripheral Module Disable:** Modules that are not being used in the code can be selectively disabled using the PMD module. This further reduces the power consumption.

1.1.2 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18(L)F2x/4xK40 family offer several different oscillator options. The PIC18(L)F2x/4xK40 family can be clocked from several different sources:

- HFINTOSC
  - 1-64 MHz precision digitally controlled internal oscillator
- LFINTOSC
  - 31 kHz internal oscillator
- EXTOSC
  - External clock (EC)
  - Low-power oscillator (LP)
  - Medium power oscillator (XT)
  - High-power oscillator (HS)
- SOSC
  - Secondary oscillator circuit operating at 31 kHz
- A Phase Lock Loop (PLL) frequency multiplier (4x) is available to the External Oscillator modes enabling clock speeds of up to 64 MHz
- Fail-Safe Clock Monitor: This option constantly monitors the main clock source against a reference signal provided by the LFINTOSC. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued operation or a safe application shutdown.

REGISTER 3-6: CONFIGURATION WORD 3H (30 0005h): WINDOWED WATCHDOG TIMER

U-1	U-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	WDTCCS<2:0>			WDTCWS<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'	
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '1'

bit 5-3 **WDTCCS<2:0>:** WDT Input Clock Selector bits

If WDTE<1:0> fuses = 2'b00

This bit is ignored.

Otherwise:

111 = Software Control
110 = Reserved (Default to LFINTOSC)
.
.
.
010 = Reserved (Default to LFINTOSC)
001 = WDT reference clock is the 31.25 kHz MFINTOSC
000 = WDT reference clock is the 31.0 kHz LFINTOSC (default value)

bit 2-0 **WDTCWS<2:0>:** WDT Window Select bits

WDTCWS	WINDOW at POR			Software control of WINDOW	Keyed access required?
	Value	Window delay Percent of time	Window opening Percent of time		
111	111	n/a	100	Yes	No
110	111	n/a	100	No	Yes
101	101	25	75		
100	100	37.5	62.5		
011	011	50	50		
010	010	62.5	37.5		
001	001	75	25		
000	000	87.5	12.5		

REGISTER 4-3: OSCCON3: OSCILLATOR CONTROL REGISTER 3

R/W/HC-0/0	R/W-0/0	U-0	R-0/0	R-0/0	U-0	U-0	U-0
CSWHOLD	SOSCPWR	—	ORDY	NOSCR	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **CSWHOLD:** Clock Switch Hold bit
- 1 = Clock switch will hold (with interrupt) when the oscillator selected by NOSC is ready
- 0 = Clock switch may proceed when the oscillator selected by NOSC is ready; NOSCR becomes '1', the switch will occur

bit 6 **SOSCPWR:** Secondary Oscillator Power Mode Select bit
- 1 = Secondary oscillator operating in High-Power mode
- 0 = Secondary oscillator operating in Low-Power mode

bit 5 **Unimplemented:** Read as '0'

bit 4 **ORDY:** Oscillator Ready bit (read-only)
- 1 = OSCCON1 = OSCCON2; the current system clock is the clock specified by NOSC
- 0 = A clock switch is in progress

bit 3 **NOSCR:** New Oscillator is Ready bit (read-only)**(1)**
- 1 = A clock switch is in progress and the oscillator selected by NOSC indicates a "ready" condition
- 0 = A clock switch is not in progress, or the NOSC-selected oscillator is not yet ready

bit 2-0 **Unimplemented:** Read as '0'

Note 1: If CSWHOLD = 0, the user may not see this bit set because, when the oscillator becomes ready there may be a delay of one instruction clock before this bit is set. The clock switch occurs in the next instruction cycle and this bit is cleared.

REGISTER 4-4: OSCSTAT: OSCILLATOR STATUS REGISTER 1

R-q/q	R-q/q	R-q/q	R-q/q	R-q/q	R-q/q	U-0	R-q/q
EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLR
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Reset value is determined by hardware

bit 7 **EXTOR:** EXTOSC (external) Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used

bit 6 **HFOR:** HFINTOSC Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used

bit 5 **MFOR:** MFINTOSC Oscillator Ready
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used

bit 4 **LFOR:** LFINTOSC Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used

bit 3 **SOR:** Secondary (Timer1) Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used

bit 2 **ADOR:** ADC Oscillator Ready bit
1 = The oscillator is ready to be used
0 = The oscillator is not enabled, or is not yet ready to be used

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **PLLR:** PLL is Ready bit
1 = The PLL is ready to be used
0 = The PLL is not enabled, the required input source is not ready, or the PLL is not locked.

10.6 Data Addressing Modes

Note: The execution of some instructions in the core PIC18 instruction set are changed when the PIC18 extended instruction set is enabled. See **Section 10.7 "Data Memory and the Extended Instruction Set"** for more information.

While the program memory can be addressed in only one way – through the program counter – information in the data memory space can be addressed in several ways. For most instructions, the addressing mode is fixed. Other instructions may use up to three modes, depending on which operands are used and whether or not the extended instruction set is enabled.

The addressing modes are:

- Inherent
- Literal
- Direct
- Indirect

An additional addressing mode, Indexed Literal Offset, is available when the extended instruction set is enabled (XINST Configuration bit = 1). Its operation is discussed in greater detail in **Section 10.7.1 "Indexed Addressing with Literal Offset"**.

10.6.1 INHERENT AND LITERAL ADDRESSING

Many PIC18 control instructions do not need any argument at all; they either perform an operation that globally affects the device or they operate implicitly on one register. This addressing mode is known as Inherent Addressing. Examples include SLEEP, RESET and DAW.

Other instructions work in a similar way but require an additional explicit argument in the opcode. This is known as Literal Addressing mode because they require some literal value as an argument. Examples include ADDLW and MOVLW, which respectively, add or move a literal value to the W register. Other examples include CALL and GOTO, which include a 20-bit program memory address.

10.6.2 DIRECT ADDRESSING

Direct addressing specifies all or part of the source and/or destination address of the operation within the opcode itself. The options are specified by the arguments accompanying the instruction.

In the core PIC18 instruction set, bit-oriented and byte-oriented instructions use some version of direct addressing by default. All of these instructions include some 8-bit literal address as their Least Significant Byte. This address specifies either a register address in one of the banks of data RAM (**Section 10.4.3 "General Purpose Register File"**) or a location in the Access Bank (**Section 10.4.2 "Access Bank"**) as the data source for the instruction.

The Access RAM bit 'a' determines how the address is interpreted. When 'a' is '1', the contents of the BSR (**Section 10.4.1 "Bank Select Register (BSR)"**) are used with the address to determine the complete 12-bit address of the register. When 'a' is '0', the address is interpreted as being a register in the Access Bank. Addressing that uses the Access RAM is sometimes also known as Direct Forced Addressing mode.

A few instructions, such as MOVFF, include the entire 12-bit address (either source or destination) in their opcodes. In these cases, the BSR is ignored entirely.

The destination of the operation's results is determined by the destination bit 'd'. When 'd' is '1', the results are stored back in the source register, overwriting its original contents. When 'd' is '0', the results are stored in the W register. Instructions without the 'd' argument have a destination that is implicit in the instruction; their destination is either the target register being operated on or the W register.

10.6.3 INDIRECT ADDRESSING

Indirect addressing allows the user to access a location in data memory without giving a fixed address in the instruction. This is done by using File Select Registers (FSRs) as pointers to the locations which are to be read or written. Since the FSRs are themselves located in RAM as Special File Registers, they can also be directly manipulated under program control. This makes FSRs very useful in implementing data structures, such as tables and arrays in data memory.

The registers for indirect addressing are also implemented with Indirect File Operands (INDFs) that permit automatic manipulation of the pointer value with auto-incrementing, auto-decrementing or offsetting with another value. This allows for efficient code, using loops, such as the example of clearing an entire RAM bank in Example 10-5.

EXAMPLE 10-5: HOW TO CLEAR RAM (BANK 1) USING INDIRECT ADDRESSING

```
         LFSR   FSR0, 100h ;
NEXT     CLRF   POSTINC0   ; Clear INDF
                           ; register then
                           ; inc pointer
         BTFSS  FSR0H, 1   ; All done with
                           ; Bank1?
         BRA    NEXT       ; NO, clear next
CONTINUE                   ; YES, continue
```

REGISTER 13-3: CRCDATH: CRC DATA HIGH BYTE REGISTER

R/W-xx	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
DATA<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **DATA<15:8>**: CRC Input/Output Data bits

REGISTER 13-4: CRCDATL: CRC DATA LOW BYTE REGISTER

R/W-xx	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
DATA<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **DATA<7:0>**: CRC Input/Output Data bits
Writing to this register fills the shifter.

REGISTER 13-5: CRCACCH: CRC ACCUMULATOR HIGH BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ACC<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ACC<15:8>**: CRC Accumulator Register bits
Writing to this register writes to the CRC accumulator register. Reading from this register reads the CRC accumulator.

FIGURE 16-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM (PORTA EXAMPLE)

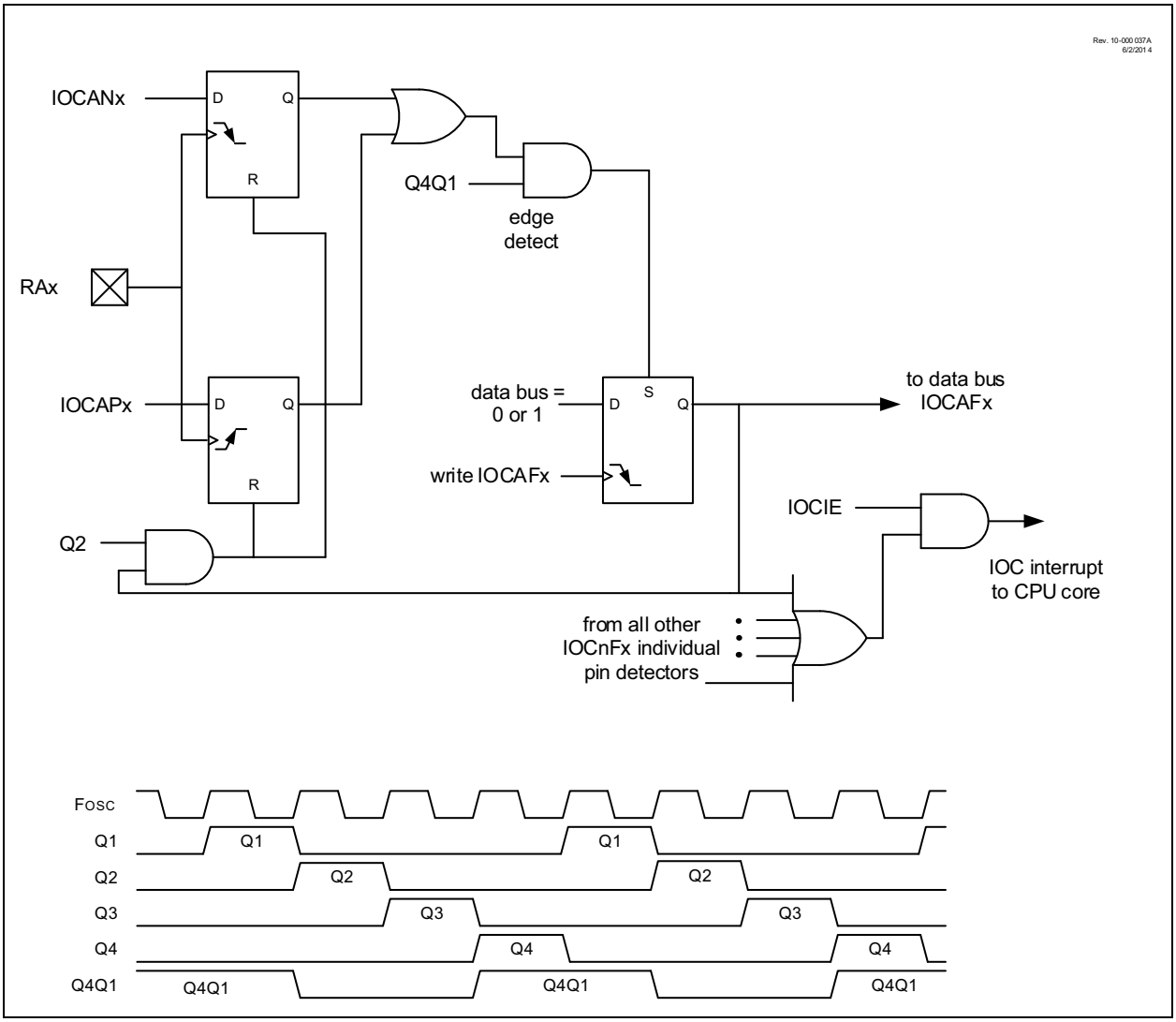


TABLE 17-1: PPS INPUT REGISTER DETAILS

Peripheral	PPS Input Register	Default Pin Selection at POR	Register Reset Value at POR	Input Available from Selected PORTx		
Interrupt 0	INT0PPS	RB0	5'b0 1000	A	B	—
Interrupt 1	INT1PPS	RB1	5'b0 1001	A	B	—
Interrupt 2	INT2PPS	RB2	5'b0 1010	A	B	—
Timer0 Clock	T0CKIPPS	RA4	5'b0 0100	A	B	—
Timer1 Clock	T1CKIPPS	RC0	5'b1 0000	A	—	C
Timer1 Gate	T1GPPS	RB5	5'b0 1101	—	B	C
Timer3 Clock	T3CKIPPS	RC0	5'b1 0000	—	B	C
Timer3 Gate	T3GPPS	RC0	5'b1 0000	A	—	C
Timer5 Clock	T5CKIPPS	RC2	5'b1 0010	A	—	C
Timer5 Gate	T5GPPS	RB4	5'b0 1100	—	B	C
Timer2 Clock	T2INPPS	RC3	5'b1 0011	A	—	C
Timer4 Clock	T4INPPS	RC5	5'b1 0101	—	B	C
Timer6 Clock	T6INPPS	RB7	5'b0 1111	—	B	C
CCP1	CCP1PPS	RC2	5'b1 0010	—	B	C
CCP2	CCP2PPS	RC1	5'b1 0001	—	B	C
CWG	CWG1PPS	RB0	5'b0 1000	—	B	C
DSM Carrier Low	MDCARLPPS	RA3	5'b0 0011	A	—	C
DSM Carrier High	MDCARHPPS	RA4	5'b0 0100	A	—	C
DSM Source	MDSRCPPS	RA5	5'b0 0101	A	—	C
ADC Conversion Trigger	ADACTPPS	RB4	5'b0 1100	—	B	C
MSSP1 Clock	SSP1CLKPPS	RC3	5'b1 0011	—	B	C
MSSP1 Data	SSP1DATPPS	RC4	5'b1 0100	—	B	C
MSSP1 Slave Select	SSP1SSPPS	RA5	5'b0 0101	A	—	C
EUSART1 Receive	RX1PPS	RC7	5'b1 0111	—	B	C
EUSART1 Transmit	TX1PPS	RC6	5'b1 0110	—	B	C

REGISTER 17-2: RxyPPS: PIN Rxy OUTPUT SOURCE SELECTION REGISTER

U-0	U-0	U-0	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	RxyPPS<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RxyPPS<4:0>:** Pin Rxy Output Source Selection bits

RxyPPS<4:0>	**Pin Rxy Output Source**	**Device Configuration**		
		PIC18(L)F24/25K40		
0x13	ADGRDB	A	—	C
0x12	ADGRDA	A	—	C
0x11	DSM	A	—	C
0x10	CLKR	—	B	C
0x0F	TMR0	—	B	C
0x0E	MSSP1 (SDO/SDA)	—	B	C
0x0D	MSSP1 (SCK/SCL)	—	B	C
0x0C	CMP2	A	—	C
0x0B	CMP1	A	—	C
0x0A	EUSART1 (RX)	—	B	C
0x09	EUSART1 (TX)	—	B	C
0x08	PWM4	A	—	C
0x07	PWM3	A	—	C
0x06	CCP2	—	B	C
0x05	CCP1	—	B	C
0x04	CWG1D	—	B	C
0x03	CWG1C	—	B	C
0x02	CWG1B	—	B	C
0x01	CWG1A	—	B	C
0x00	LATxy	A	B	C

REGISTER 18-2: T0CON1: TIMER0 CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
T0CS<2:0>			T0ASYNC	T0CKPS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **T0CS<2:0>:**Timer0 Clock Source Select bits
111 = Reserved
110 = Reserved
101 = SOSC
100 = LFINTOSC
011 = HFINTOSC
010 = FOSC/4
001 = Pin selected by T0CKIPPS (Inverted)
000 = Pin selected by T0CKIPPS (Non-inverted)

bit 4 **T0ASYNC:** TMR0 Input Asynchronization Enable bit
1 = The input to the TMR0 counter is not synchronized to system clocks
0 = The input to the TMR0 counter is synchronized to FOSC/4

bit 3-0 **T0CKPS<3:0>:** Prescaler Rate Select bit
1111 = 1:32768
1110 = 1:16384
1101 = 1:8192
1100 = 1:4096
1011 = 1:2048
1010 = 1:1024
1001 = 1:512
1000 = 1:256
0111 = 1:128
0110 = 1:64
0101 = 1:32
0100 = 1:16
0011 = 1:8
0010 = 1:4
0001 = 1:2
0000 = 1:1

REGISTER 18-3: TMR0L: TIMER0 COUNT REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TMR0<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **TMR0<7:0>:** TMR0 Counter bits <7:0>

REGISTER 18-4: TMR0H: TIMER0 PERIOD REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TMR0<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 When T016BIT = 0
PR0<7:0>: TMR0 Period Register Bits <7:0>
When T016BIT = 1
TMR0<15:8>: TMR0 Counter bits <15:8>

TABLE 18-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
TMR0L	TMR0<7:0>								220
TMR0H	TMR0<15:8>								220
T0CON0	T0EN	—	T0OUT	T016BIT	T0OUTPS<3:0>				218
T0CON1	T0CS<2:0>			T0ASYNC	T0CKPS<3:0>				219
T0CKIPPS	—	—	—	T0CKIPPS<4:0>					211
TMR0PPS	—	—	—	TMR0PPS<4:0>					211
INTCON	GIE/GIEH	PEIE/GIEL	IPEN	—	—	INT2EDG	INT1EDG	INT0EDG	166
PIR0	—	—	TMR0IF	IOCIF	—	INT2IF	INT1IF	INT0IF	167
PIE0	—	—	TMR0IE	IOCIE	—	INT2IE	INT1IE	INT0IE	175
IPR0	—	—	TMR0IP	IOCIP	—	INT2IP	INT1IP	INT0IP	183
PMD1	—	TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	TMR0MD	65

Legend: — = Unimplemented location, read as ‘0’. Shaded cells are not used by the Timer0 module.

REGISTER 19-4: TMRxGATE: TIMERx GATE ISM REGISTER

U-0	U-0	U-0	U-0	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	—	GSS<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	u = unchanged

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **GSS<3:0>:** Timerx Gate Source Selection bits

GSS	Timer1	Timer3	Timer5
	Gate Source	Gate Source	Gate Source
1111	Reserved	Reserved	Reserved
1110	ZCDOUT	ZCDOUT	ZCDOUT
1101	CMP2OUT	CMP2OUT	CMP2OUT
1100	CMP1OUT	CMP1OUT	CMP1OUT
1011	PWM4OUT	PWM4OUT	PWM4OUT
1010	PWM3OUT	PWM3OUT	PWM3OUT
1001	CCP2OUT	CCP2OUT	CCP2OUT
1000	CCP1OUT	CCP1OUT	CCP1OUT
0111	TMR6OUT (post-scaled)	TMR6OUT (post-scaled)	TMR6OUT (post-scaled)
0110	TMR5 overflow	TMR5 overflow	Reserved
0101	TMR4OUT (post-scaled)	TMR4OUT (post-scaled)	TMR4OUT (post-scaled)
0100	TMR3 overflow	Reserved	TMR3 overflow
0011	TMR2OUT (post-scaled)	TMR2OUT (post-scaled)	TMR2OUT (post-scaled)
0010	Reserved	TMR1 overflow	TMR1 overflow
0001	TMR0 overflow	TMR0 overflow	TMR0 overflow
0000	Pin selected by T1GPPS	Pin selected by T3GPPS	Pin selected by T5GPPS

TABLE 19-4: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1/3/5 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
INTCON	GIE/GIEH	PEIE/GIEL	IPEN	—	—	INT2EDG	INT1EDG	INT0EDG	166
PIE4	—	—	TMR6IE	TMR5IE	TMR4IE	TMR3IE	TMR2IE	TMR1IE	179
PIE5	—	—	—	—	—	TMR5GIE	TMR3GIE	TMR1GIE	180
PIR4	—	—	TMR6IF	TMR5IF	TMR4IF	TMR3IF	TMR2IF	TMR1IF	170
PIR5	—	—	—	—	—	TMR5GIF	TMR3GIF	TMR1GIF	171
IPR4	—	—	TMR6IP	TMR5IP	TMR4IP	TMR3IP	TMR2IP	TMR1IP	187
IPR5	—	—	—	—	—	TMR5GIP	TMR3GIP	TMR1GIP	188
PMD1	—	TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	TMR0MD	65
T1CON	—	—	CKPS<1:0>		—	$\overline{\text{SYNC}}$	RD16	ON	223
T1GCON	GE	GPOL	GTM	GSPM	GO/$\overline{\text{DONE}}$	GVAL	—	—	224
T3CON	—	—	CKPS<1:0>		—	$\overline{\text{SYNC}}$	RD16	ON	223
T3GCON	GE	GPOL	GTM	GSPM	GO/$\overline{\text{DONE}}$	GVAL	—	—	224
T5CON	—	—	CKPS<1:0>		—	$\overline{\text{SYNC}}$	RD16	ON	223
T5GCON	GE	GPOL	GTM	GSPM	GO/$\overline{\text{DONE}}$	GVAL	—	—	224
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								227
TMR1L	Least Significant Byte of the 16-bit TMR1 Register								227
TMR3H	Holding Register for the Most Significant Byte of the 16-bit TMR3 Register								227
TMR3L	Least Significant Byte of the 16-bit TMR3 Register								227
TMR5H	Holding Register for the Most Significant Byte of the 16-bit TMR5 Register								227
TMR5L	Least Significant Byte of the 16-bit TMR5 Register								227
T1CKIPPS	—	—	—	T1CKIPPS<4:0>					211
T1GPPS	—	—	—	T1GPPS<4:0>					211
T3CKIPPS	—	—	—	T3CKIPPS<4:0>					211
T3GPPS	—	—	—	T3GPPS<4:0>					211
T5CKIPPS	—	—	—	T5CKIPPS<4:0>					211
T5GPPS	—	—	—	T5GPPS<4:0>					211

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by TIMER1/3/5.

20.0 TIMER2/4/6 MODULE

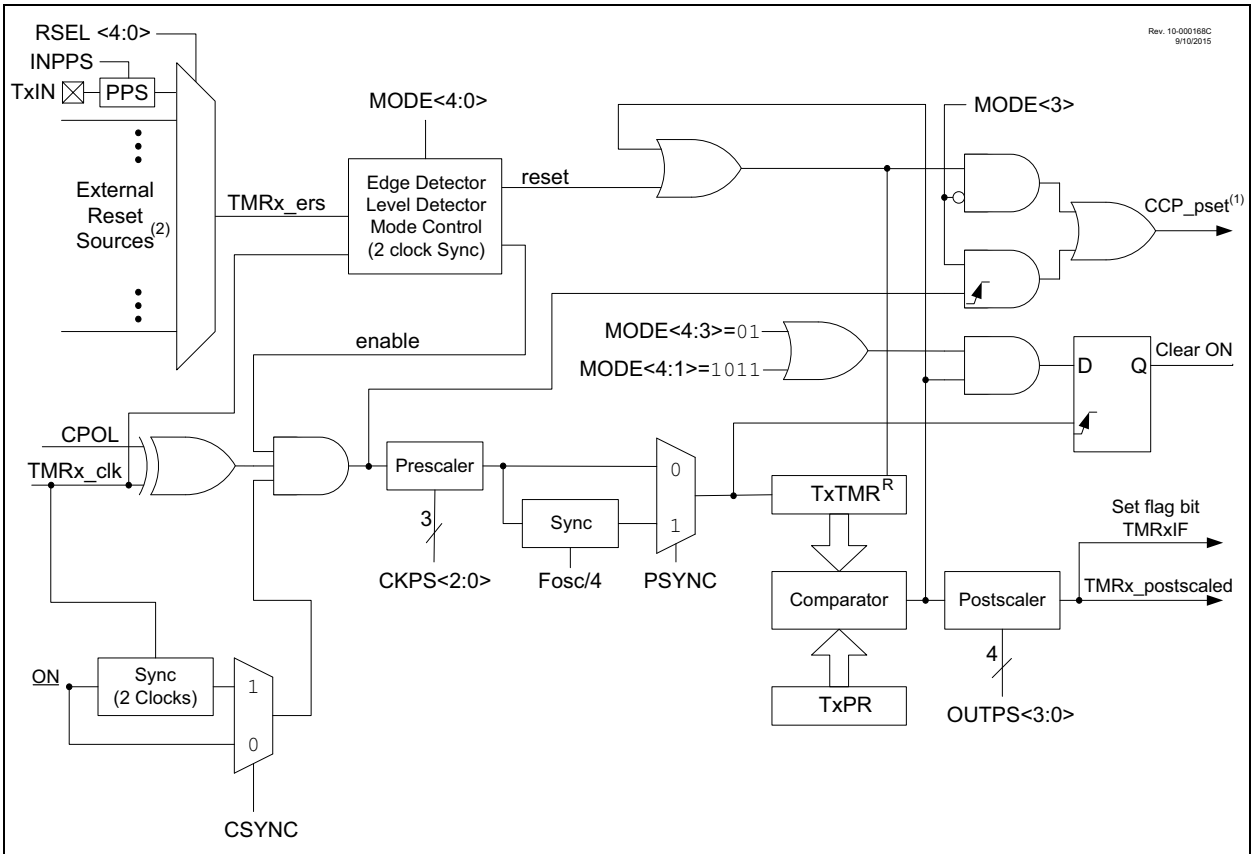
The Timer2/4/6 modules are 8-bit timers that can operate as free-running period counters or in conjunction with external signals that control start, run, freeze, and reset operation in One-Shot and Monostable modes of operation. Sophisticated waveform control such as pulse density modulation are possible by combining the operation of these timers with other internal peripherals such as the comparators and CCP modules. Features of the timer include:

- 8-bit timer register
- 8-bit period register
- Selectable external hardware timer Resets
- Programmable prescaler (1:1 to 1:128)
- Programmable postscaler (1:1 to 1:16)
- Selectable synchronous/asynchronous operation
- Alternate clock sources
- Interrupt-on-period
- Three modes of operation:
  - Free Running Period
  - One-shot
  - Monostable

See Figure 20-1 for a block diagram of Timer2. See Figure 20-2 for the clock source block diagram.

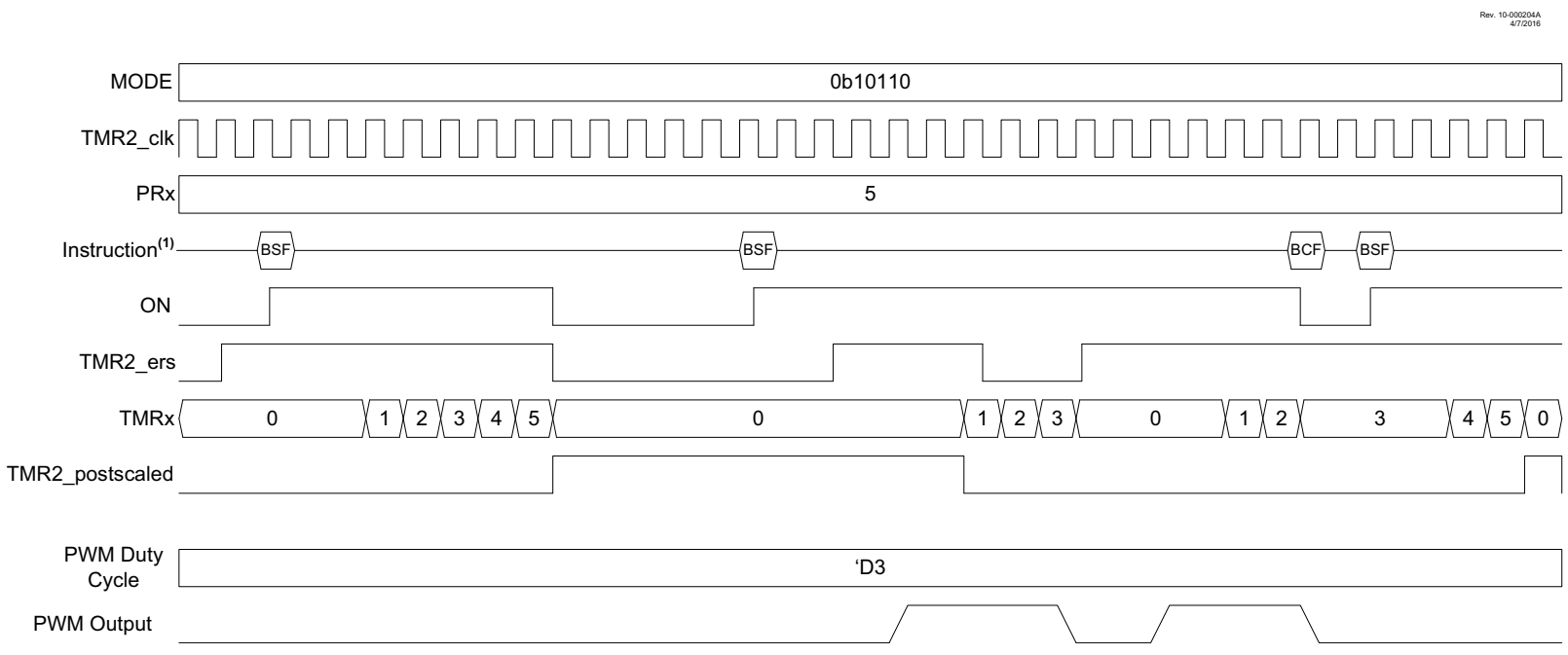
Note:	Three identical Timer2 modules are implemented on this device. The timers are named Timer2, Timer4 and Timer6. All references to Timer2 apply as well to Timer4 and Timer6. All references to PR2 apply equally to other timers as well.

FIGURE 20-1: TIMER2 BLOCK DIAGRAM



Note 1: Signal to the CCP to trigger the PWM pulse.
2: See Table 20.5 for description of CCP interaction in the different TMR modes.
3: See Table 20.5 for external Reset sources.

FIGURE 20-13: LEVEL-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 10110)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

REGISTER 31-13: ADCNT: ADC REPEAT COUNTER REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADCNT<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ADCNT<7:0>**: ADC Repeat Count bits
Determines the number of times that the ADC is triggered before the threshold is checked when the computation is Low-pass Filter, Burst Average, or Average modes. See Table 31-2 for more details.

REGISTER 31-14: ADFLTRH: ADC FILTER HIGH BYTE REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADFLTR<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ADFLTR<15:8>**: ADC Filter Output Most Significant bits
In Accumulate, Average, and Burst Average mode, this is equal to ADACC right shifted by the ADCRS bits of ADCON2. In LPF mode, this is the output of the Low-pass Filter.

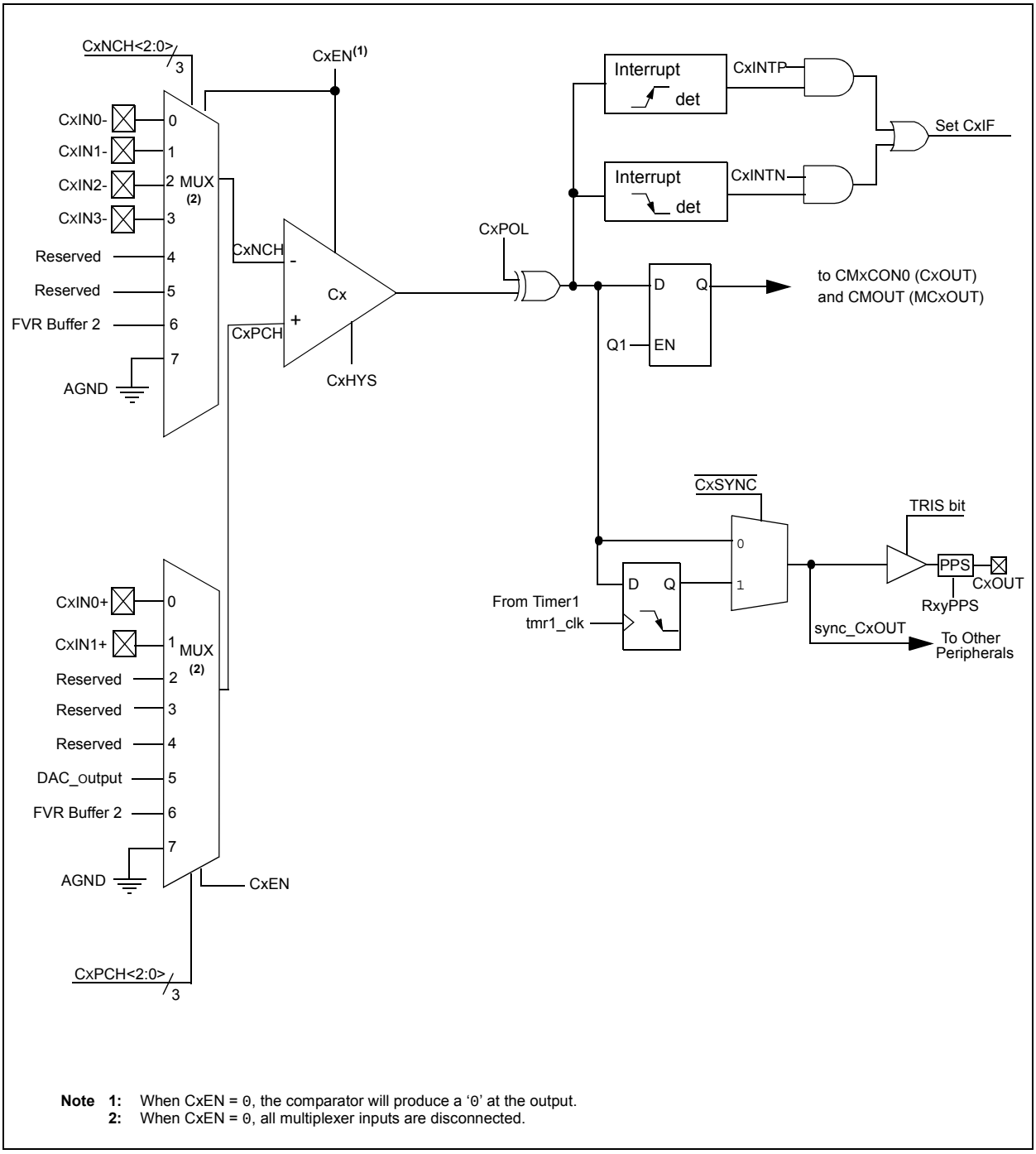
REGISTER 31-15: ADFLTRL: ADC FILTER LOW BYTE REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADFLTR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ADFLTR<7:0>**: ADC Filter Output Least Significant bits
In Accumulate, Average, and Burst Average mode, this is equal to ADACC right shifted by the ADCRS bits of ADCON2. In LPF mode, this is the output of the Low-pass Filter.

FIGURE 32-2: COMPARATOR MODULE SIMPLIFIED BLOCK DIAGRAM



Note 1: When CxEN = 0, the comparator will produce a '0' at the output.
2: When CxEN = 0, all multiplexer inputs are disconnected.

TABLE 37-4: I/O PORTS

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O PORT:					
D300		with TTL buffer	—	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
D301			—	—	0.15 VDD	V	1.8V ≤ VDD ≤ 4.5V
D302		with Schmitt Trigger buffer	—	—	0.2 VDD	V	2.0V ≤ VDD ≤ 5.5V
D303		with I^2C levels	—	—	0.3 VDD	V	
D304		with SMBus levels	—	—	0.8	V	2.7V ≤ VDD ≤ 5.5V
D305		$\overline{MCLR}$	—	—	0.2 VDD	V	
	VIH	**Input High Voltage**					
		I/O PORT:					
D320		with TTL buffer	2.0	—	—	V	4.5V ≤ VDD ≤ 5.5V
D321			0.25 VDD + 0.8	—	—	V	1.8V ≤ VDD ≤ 4.5V
D322		with Schmitt Trigger buffer	0.8 VDD	—	—	V	2.0V ≤ VDD ≤ 5.5V
D323		with I^2C levels	0.7 VDD	—	—	V	
D324		with SMBus levels	2.1	—	—	V	2.7V ≤ VDD ≤ 5.5V
D325		$\overline{MCLR}$	0.7 VDD	—	—	V	
	IIL	**Input Leakage Current(1)**					
D340		I/O Ports	—	± 5	± 125	nA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance, 85°C
D341			—	± 5	± 1000	nA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance, 125°C
D342		$\overline{MCLR}$(2)	—	± 50	± 200	nA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance, 85°C
	IPUR	**Weak Pull-up Current**					
D350			25	120	200	µA	VDD = 3.0V, VPIN = VSS
	VOL	**Output Low Voltage**					
D360		I/O ports	—	—	0.6	V	IOL = 10.0mA, VDD = 3.0V
	VOH	**Output High Voltage**					
D370		I/O ports	VDD - 0.7	—	—	V	IOH = 6.0 mA, VDD = 3.0V
D380	CIO	**All I/O pins**	—	5	50	pF	

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Negative current is defined as current sourced by the pin.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

FIGURE 37-12: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

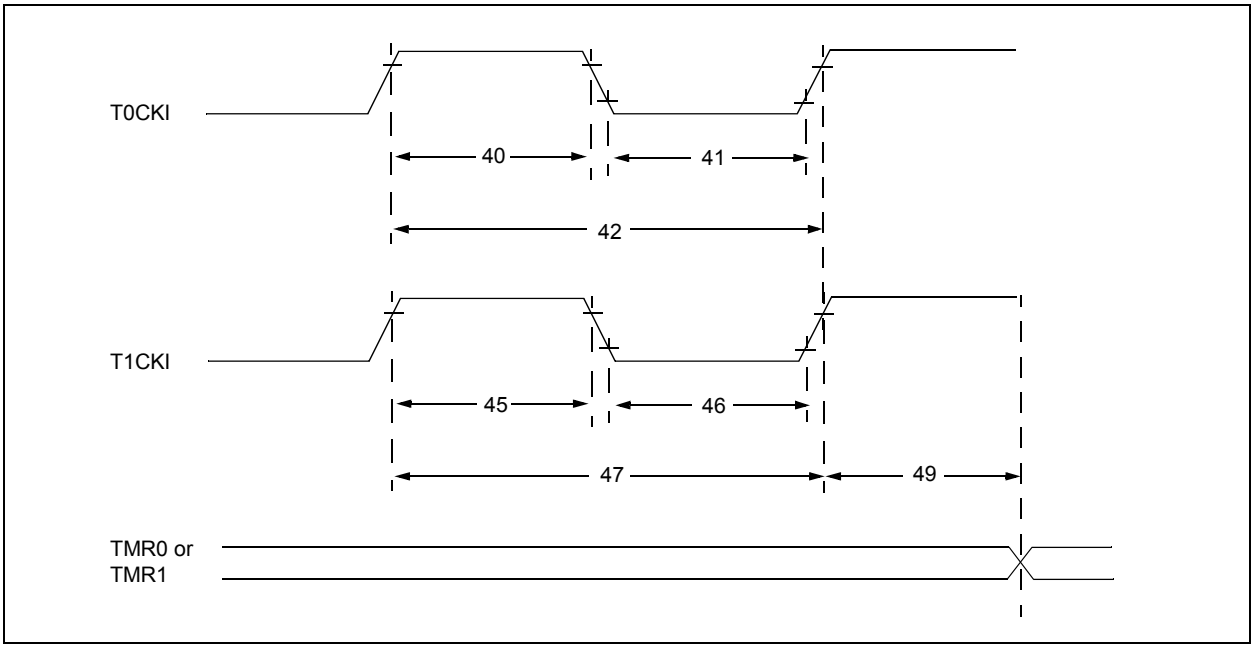


TABLE 37-19: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

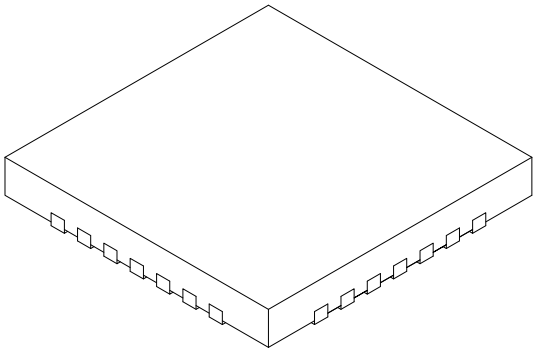
Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C									
Param No.	**Sym.**	**Characteristic**			**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
40*	TT0H	T0CKI High Pulse Width		No Prescaler	0.5 TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
41*	TT0L	T0CKI Low Pulse Width		No Prescaler	0.5 TCY + 20	—	—	ns	
				With Prescaler	10	—	—	ns	
42*	TT0P	T0CKI Period			Greater of: 20 or TCY + 40 / N	—	—	ns	N = prescale value
45*	TT1H	T1CKI High Time	Synchronous, No Prescaler		0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler		15	—	—	ns	
			Asynchronous		30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, No Prescaler		0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler		15	—	—	ns	
			Asynchronous		30	—	—	ns	
47*	TT1P	T1CKI Input Period	Synchronous		Greater of: 30 or TCY + 40 / N	—	—	ns	N = prescale value
			Asynchronous		60	—	—	ns	
49*	TCKEZTMR1	Delay from External Clock Edge to Timer Increment			2 TOSC	—	7 TOSC	—	Timers in Sync mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.55	2.65	2.75
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.55	2.65	2.75
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-152A Sheet 2 of 2