



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf24k40-e-mv

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

4.5.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed.



15.1 I/O Priorities

Each pin defaults to the PORT data latch after Reset. Other functions are selected with the peripheral pin select logic. See **Section 17.0** "**Peripheral Pin Select** (**PPS**) **Module**" for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx register. Digital output functions may continue to control the pin when it is in Analog mode.

Analog outputs, when enabled, take priority over digital outputs and force the digital output driver into a high-impedance state.

The pin function priorities are as follows:

- 1. Configuration bits
- 2. Analog outputs (disable the input buffers)
- 3. Analog inputs
- 4. Port inputs and outputs from PPS

15.2 PORTx Registers

In this section the generic names such as PORTx, LATx, TRISx, etc. can be associated with PORTA, PORTB, PORTC and PORTD. For availability of PORTD refer to Table 15-1. The functionality of PORTE is different compared to other ports and is explained in a separate section.

15.2.1 DATA REGISTER

PORTx is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISx (Register 15-2). Setting a TRISx bit ('1') will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISx bit ('0') will make the corresponding PORTx pin an output (i.e., it enables output driver and puts the contents of the output latch on the selected pin). Example 15-1 shows how to initialize PORTx.

Reading the PORTx register (Register 15-1) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATx).

The PORT data latch LATx (Register 15-3) holds the output port data and contains the latest value of a LATx or PORTx write.

EXAMPLE 15-1: INITIALIZING PORTA

;	This	code	exa	ample	e illus	strates	
;	initi	ializi	lnq	the	PORTA	register.	The

; other ports are initialized in the same

	OCHCI	POLCO	arc	INTETATIOCA	T 11	CIIC	ban
:	manne	r					

BANKSEL	PORTA	;
CLRF	PORTA	;Init PORTA
BANKSEL	LATA	;Data Latch
CLRF	LATA	;
BANKSEL	ANSELA	;
CLRF	ANSELA	;digital I/O
BANKSEL	TRISA	;
MOVLW	B'11111000'	;Set RA<7:3> as inputs
MOVWF	TRISA	;and set RA<2:0> as
		;outputs

15.2.2 DIRECTION CONTROL

The TRISx register (Register 15-2) controls the PORTx pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISx register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

15.2.3 ANALOG CONTROL

The ANSELx register (Register 15-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELx bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELx bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELx bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

15.2.4 OPEN-DRAIN CONTROL

The ODCONx register (Register 15-6) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONx bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONx bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

Note: It is not necessary to set open-drain control when using the pin for I²C; the I²C module controls the pin and makes the pin open-drain.

REGISTER 18-3: TMR0L: TIMER0 COUNT REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
			TMR)<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	oit	U = Unimpler	nented bit, read	as '0'	
u = Bit is uncha	anged	x = Bit is unkn	own	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets

bit 7-0 TMR0<7:0>:TMR0 Counter bits <7:0>

'1' = Bit is set

REGISTER 18-4: TMR0H: TIMER0 PERIOD REGISTER

'0' = Bit is cleared

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
	TMR0<15:8>						
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 When T016BIT = 0 **PR0<7:0>:**TMR0 Period Register Bits <7:0> When T016BIT = 1 **TMR0<15:8>:** TMR0 Counter bits <15:8>

TABLE 18-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
TMR0L	TMR0<7:0>								
TMR0H	TMR0<15:8>							220	
T0CON0	T0EN	—	TOOUT	T016BIT	T016BIT T0OUTPS<3:0>				218
T0CON1		T0CS<2:0>		T0ASYNC T0CKPS<3:0>				219	
T0CKIPPS	-	—	—	T0CKIPPS<4:0>					211
TMR0PPS	—	—	—		TMRC)PPS<4:0>			211
INTCON	GIE/GIEH	PEIE/GIEL	IPEN	—	—	INT2EDG	INT1EDG	INT0EDG	166
PIR0	-	—	TMR0IF	IOCIF	—	INT2IF	INT1IF	INT0IF	167
PIE0	—	—	TMR0IE	IOCIE	—	INT2IE	INT1IE	INT0IE	175
IPR0	_	_	TMR0IP	IOCIP	_	INT2IP	INT1IP	INT0IP	183
PMD1		TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	TMR0MD	65

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the Timer0 module.

© 2016-2017 Microchip Technology Inc.

20.5.3 EDGE-TRIGGERED HARDWARE LIMIT MODE

In Hardware Limit mode the timer can be reset by the TMRx_ers external signal before the timer reaches the period count. Three types of Resets are possible:

- Reset on rising or falling edge (MODE<4:0>= 00011)
- Reset on rising edge (MODE<4:0> = 00100)
- Reset on falling edge (MODE<4:0> = 00101)

FIGURE 20-6: EDGE-TRIGGERED HARDWARE LIMIT MODE TIMING DIAGRAM (MODE = 00100)



When the timer is used in conjunction with the CCP in PWM mode then an early Reset shortens the period and restarts the PWM pulse after a two clock delay. Refer to Figure 20-6.

R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1
P4TSE	L<1:0>	P3TSE	_<1:0>	C2TSE	EL<1:0>	C1TSEI	_<1:0>
bit 7				·			bit 0
Legend:							
R = Readable I	bit	W = Writable	oit	U = Unimplem	nented bit, read	as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkno	own
bit 7-6	P4TSEL<1:0> 11 = PWM4 1 10 = PWM4 1 01 = PWM4 1 00 = Reserve	 PWM4 Times based on TMR based on TMR based on TMR based on TMR 	⁻ Selection bit 6 4 2	'S			
bit 5-4	P3TSEL<1:0>: PWM3 Timer Selection bits 11 = PWM3 based on TMR6 10 = PWM3 based on TMR4 01 = PWM3 based on TMR2 00 = Reserved						
bit 3-2	C2TSEL<1:0>: CCP2 Timer Selection bits 11 = CCP2 is based off Timer5 in Capture/Compare mode and Timer6 in PWM mode 10 = CCP2 is based off Timer3 in Capture/Compare mode and Timer4 in PWM mode 01 = CCP2 is based off Timer1 in Capture/Compare mode and Timer2 in PWM mode 00 = Reserved						
bit 1-0	C1TSEL<1:0>: CCP1 Timer Selection bits 11 = CCP1 is based off Timer5 in Capture/Compare mode and Timer6 in PWM mode 10 = CCP1 is based off Timer3 in Capture/Compare mode and Timer4 in PWM mode 01 = CCP1 is based off Timer1 in Capture/Compare mode and Timer2 in PWM mode 00 = Reserved						

REGISTER 21-2: CCPTMRS: CCP TIMERS CONTROL REGISTER



FIGURE 21-4: SIMPLIFIED PWM BLOCK DIAGRAM

22.2 Register Definitions: PWM Control

Long bit name prefixes for the PWM peripherals are shown in Table 22-3. Refer to **Section 1.4.2.2 "Long Bit Names"** for more information.

TABLE 22-3:

Peripheral	Bit Name Prefix
PWM3	PWM3
PWM4	PWM4

REGISTER 22-1: PWMxCON: PWM CONTROL REGISTER

R/W-0/0	U-0	R-0/0	R/W-0/0	U-0	U-0	U-0	U-0
EN	—	OUT	POL	—	—	—	—
bit 7							bit 0

W = Writable bit	U = Unimplemented bit, read as '0'
x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'0' = Bit is cleared	
	W = Writable bit x = Bit is unknown '0' = Bit is cleared

bit 7	EN: PWM Module Enable bit
	1 = PWM module is enabled0 = PWM module is disabled
bit 6	Unimplemented: Read as '0'
bit 5	OUT: PWM Module Output Level When Bit is Read
bit 4	POL: PWM Output Polarity Select bit
	1 = PWM output is inverted0 = PWM output is normal
bit 3-0	Unimplemented: Read as '0'

In Forward Full-Bridge mode (MODE<2:0> = 010), CWG1A is driven to its active state, CWG1B and CWG1C are driven to their inactive state, and CWG1D is modulated by the input signal, as shown in Figure 24-7.

In Reverse Full-Bridge mode (MODE<2:0> = 011), CWG1C is driven to its active state, CWG1A and CWG1D are driven to their inactive states, and CWG1B is modulated by the input signal, as shown in Figure 24-7. In Full-Bridge mode, the dead-band period is used when there is a switch from forward to reverse or viceversa. This dead-band control is described in Section 24.6 "Dead-Band Control", with additional details in Section 24.7 "Rising Edge and Reverse Dead Band" and Section 24.8 "Falling Edge and Forward Dead Band". Steering modes are not used with either of the Full-Bridge modes. The mode selection may be toggled between forward and reverse toggling the MODE<0> bit of the CWG1CON0 while keeping MODE<2:1> static, without disabling the CWG module.

FIGURE 24-7: EXAMPLE OF FULL-BRIDGE OUTPUT



26.8.9 ACKNOWLEDGE SEQUENCE

The ninth SCL pulse for any transferred byte in I^2C is dedicated as an Acknowledge. It allows receiving devices to respond back to the transmitter by pulling the SDA line low. The transmitter must release control of the line during this time to shift in the response. The Acknowledge (ACK) is an active-low signal, pulling the SDA line low indicates to the transmitter that the device has received the transmitted data and is ready to receive more.

The result of an \overline{ACK} is placed in the ACKSTAT bit of the SSPxCON2 register.

Slave software, when the AHEN and DHEN bits are set, allow the user to set the ACK value sent back to the transmitter. The ACKDT bit of the SSPxCON2 register is set/cleared to determine the response.

Slave hardware will generate an ACK response if the AHEN and DHEN bits of the SSPxCON3 register are clear.

There are certain conditions where an ACK will not be sent by the slave. If the BF bit of the SSPxSTAT register or the SSPOV bit of the SSPxCON1 register are set when a byte is received.

When the module is addressed, after the eighth falling edge of SCL on the bus, the ACKTIM bit of the SSPxCON3 register is set. The ACKTIM bit indicates the acknowledge time of the active bus. The ACKTIM Status bit is only active when the AHEN bit or DHEN bit is enabled.

26.9 I²C Slave Mode Operation

The MSSP Slave mode operates in one of four modes selected by the SSPM bits of the SSPxCON1 register. The modes can be divided into 7-bit and 10-bit Addressing mode. 10-bit Addressing modes operate the same as 7-bit with some additional overhead for handling the larger addresses.

Modes with Start and Stop bit interrupts operate the same as the other modes with SSPxIF additionally getting set upon detection of a Start, Restart, or Stop condition.

26.9.1 SLAVE MODE ADDRESSES

The SSPxADD register (Register 26-5) contains the Slave mode address. The first byte received after a Start or Restart condition is compared against the value stored in this register. If the byte matches, the value is loaded into the SSPxBUF register and an interrupt is generated. If the value does not match, the module goes idle and no indication is given to the software that anything happened.

The SSP Mask register affects the address matching process. See **Section 26.9.9** "**SSP Mask Register**" for more information.

26.9.1.1 I²C Slave 7-bit Addressing Mode

In 7-bit Addressing mode, the LSb of the received data byte is ignored when determining if there is an address match.

26.9.1.2 I²C Slave 10-bit Addressing Mode

In 10-bit Addressing mode, the first received byte is compared to the binary value of '1 1 1 1 0 A9 A8 0'. A9 and A8 are the two MSb's of the 10-bit address and stored in bits 2 and 1 of the SSPxADD register.

After the acknowledge of the high byte the UA bit is set and SCL is held low until the user updates SSPxADD with the low address. The low address byte is clocked in and all eight bits are compared to the low address value in SSPxADD. Even if there is not an address match; SSPxIF and UA are set, and SCL is held low until SSPxADD is updated to receive a high byte again. When SSPxADD is updated the UA bit is cleared. This ensures the module is ready to receive the high address byte on the next communication.

A high and low address match as a write request is required at the start of all 10-bit addressing communication. A transmission can be initiated by issuing a Restart once the slave is addressed, and clocking in the high address with the R/W bit set. The slave hardware will then acknowledge the read request and prepare to clock out data. This is only valid for a slave after it has received a complete high and low address byte match.

26.9.2 SLAVE RECEPTION

When the R/W bit of a matching received address byte is clear, the R/W bit of the SSPxSTAT register is cleared. The received address is loaded into the SSPxBUF register and acknowledged.

When the overflow condition exists for a received address, then not Acknowledge is given. An overflow condition is defined as either bit BF of the SSPxSTAT register is set, or bit SSPOV of the SSPxCON1 register is set. The BOEN bit of the SSPxCON3 register modifies this operation. For more information see Register 26-3.

An MSSP interrupt is generated for each transferred data byte. Flag bit, SSPxIF, must be cleared by software.

When the SEN bit of the SSPxCON2 register is set, SCL will be held low (clock stretch) following each received byte. The clock must be released by setting the CKP bit of the SSPxCON1 register, except sometimes in 10-bit mode. See **Section 26.9.6.2 "10-bit Addressing Mode"** for more detail.

26.9.2.1 7-bit Addressing Reception

This section describes a standard sequence of events for the MSSP module configured as an I^2C slave in 7-bit Addressing mode. Figure 26-14 and Figure 26-15 is used as a visual reference for this description.

This is a step by step process of what typically must be done to accomplish I^2C communication.

- 1. Start bit detected.
- 2. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- 3. Matching address with R/\overline{W} bit clear is received.
- 4. The slave pulls SDA low sending an ACK to the master, and sets SSPxIF bit.
- 5. Software clears the SSPxIF bit.
- 6. Software reads received address from SSPxBUF clearing the BF flag.
- 7. If SEN = 1; Slave software sets CKP bit to release the SCL line.
- 8. The master clocks out a data byte.
- 9. Slave drives SDA low sending an ACK to the master, and sets SSPxIF bit.
- 10. Software clears SSPxIF.
- 11. Software reads the received byte from SSPxBUF clearing BF.
- 12. Steps 8-12 are repeated for all received bytes from the master.
- 13. Master sends Stop condition, setting P bit of SSPxSTAT, and the bus goes idle.

26.9.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the eighth falling edge of SCL. These additional interrupts allow the slave software to decide whether it wants to ACK the receive address or data byte, rather than the hardware. This functionality adds support for PMBus[™] that was not present on previous versions of this module.

This list describes the steps that need to be taken by slave software to use these options for I^2C communication. Figure 26-16 displays a module using both address and data holding. Figure 26-17 includes the operation with the SEN bit of the SSPxCON2 register set.

- 1. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- Matching address with R/W bit clear is clocked in. SSPxIF is set and CKP cleared after the eighth falling edge of SCL.
- 3. Slave clears the SSPxIF.
- Slave can look at the ACKTIM bit of the SSPxCON3 register to <u>determine</u> if the SSPxIF was after or before the ACK.
- 5. Slave reads the address value from SSPxBUF, clearing the BF flag.
- 6. Slave sets ACK value clocked out to the master by setting ACKDT.
- 7. Slave releases the clock by setting CKP.
- 8. SSPxIF is set after an ACK, not after a NACK.
- 9. If SEN = 1 the slave hardware will stretch the clock after the ACK.
- 10. Slave clears SSPxIF.

Note: SSPxIF is still set after the ninth falling edge of SCL even if there is no clock stretching and BF has been cleared. Only if NACK is sent to master is SSPxIF not set

- 11. SSPxIF set and CKP cleared after eighth falling edge of SCL for a received data byte.
- 12. Slave looks at ACKTIM bit of SSPxCON3 to determine the source of the interrupt.
- 13. Slave reads the received data from SSPxBUF clearing BF.
- 14. Steps 7-14 are the same for each received data byte.
- 15. Communication is ended by either the slave sending an ACK = 1, or the master sending a Stop condition. If a Stop is sent and Interrupt on Stop Detect is disabled, the slave will only know by polling the P bit of the SSTSTAT register.

26.9.4 SLAVE MODE 10-BIT ADDRESS RECEPTION

This section describes a standard sequence of events for the MSSP module configured as an I^2C slave in 10-bit Addressing mode.

Figure 26-20 is used as a visual reference for this description.

This is a step by step process of what must be done by slave software to accomplish I^2C communication.

- 1. Bus starts Idle.
- 2. Master sends Start condition; S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
- 3. Master sends matching high address with R/\overline{W} bit clear; UA bit of the SSPxSTAT register is set.
- 4. Slave sends ACK and SSPxIF is set.
- 5. Software clears the SSPxIF bit.
- 6. Software reads received address from SSPxBUF clearing the BF flag.
- 7. Slave loads low address into SSPxADD, releasing SCL.
- 8. Master sends matching low address byte to the slave; UA bit is set.

Note: Updates to the SSPxADD register are not allowed until after the ACK sequence.

9. Slave sends ACK and SSPxIF is set.

Note: If the low address does not match, SSPxIF and UA are still set so that the slave software can set SSPxADD back to the high address. BF is not set because there is no match. CKP is unaffected.

- 10. Slave clears SSPxIF.
- 11. Slave reads the received matching address from SSPxBUF clearing BF.
- 12. Slave loads high address into SSPxADD.
- 13. Master clocks a data byte to the slave and clocks out the slaves ACK on the ninth SCL pulse; SSPxIF is set.
- 14. If SEN bit of SSPxCON2 is set, CKP is cleared by hardware and the clock is stretched.
- 15. Slave clears SSPxIF.
- 16. Slave reads the received byte from SSPxBUF clearing BF.
- 17. If SEN is set the slave sets CKP to release the SCL.
- 18. Steps 13-17 repeat for each received byte.
- 19. Master sends Stop to end the transmission.

26.9.5 10-BIT ADDRESSING WITH ADDRESS OR DATA HOLD

Reception using 10-bit addressing with AHEN or DHEN set is the same as with 7-bit modes. The only difference is the need to update the SSPxADD register using the UA bit. All functionality, specifically when the CKP bit is cleared and SCL line is held low are the same. Figure 26-21 can be used as a reference of a slave in 10-bit addressing with AHEN set.

Figure 26-22 shows a standard waveform for a slave transmitter in 10-bit Addressing mode.



FIGURE 26-20: I²C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)

PIC18(L)F24/25K40

30.0 5-BIT DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The positive input source (VSOURCE+) of the DAC can be connected to:

- FVR Buffer
- External VREF+ pin
- VDD supply voltage

The negative input source (VSOURCE-) of the DAC can be connected to:

- External VREF- pin
- Vss

The output of the DAC (DACx_output) can be selected as a reference voltage to the following:

- · Comparator positive input
- ADC input channel
- DACxOUT1 pin
- DACxOUT2 pin

The Digital-to-Analog Converter (DAC) can be enabled by setting the DACEN bit of the DAC1CON0 register.

-000026F 8/7/2015 Reserved 11 VSOURCE+ DACR<4:0> FVR Buffer 5 10 R VREF+ 01 AVDD 00 R DACPSS R R 32-to-1 MUX DACx_output 32 To Peripherals Steps . . DACEN R DACxOUT1⁽¹⁾ R DACOE1 R DACxOUT2⁽¹⁾ **VREF-**1 VSOURCE-DACOE2 0 AVss DACNSS Note 1: The unbuffered DACx output is provided on the DACxOUT pin(s).

FIGURE 30-1: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM

REGISTER 31-11:	ADCAP: ADC ADDITIONAL	SAMPLE CAPACITOR SE	LECTION REGISTER

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0			
—	—	—	ADCAP<4:0>							
bit 7			bit C							
Legend:										
R = Readabl	e bit	W = Writable	bit	U = Unimpler	J = Unimplemented bit, read as '0'					
u = Bit is und	changed	x = Bit is unkr	nown	-n/n = Value a	at POR and BC	R/Value at all	other Resets			
'1' = Bit is se	t	'0' = Bit is clea	ared							
bit 7-5	bit 7-5 Unimplemented: Read as '0'									
bit 4-0	ADCAP<4:0>: ADC Additional Sample Capacitor Selection bits									

bit 4-0	ADCAP<4:0>: ADC Additional Sample Capacitor Selection bits
	11111 = 31 pF
	11110 = 30 pF
	11101 = 29 pF
	•
	•
	•
	00011 = 3 pF
	00010 = 2 pF
	00001 = 1 pF
	00000 = No additional capacitance

REGISTER 31-12: ADRPT: ADC REPEAT SETTING REGISTER

| R/W-0/0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| | | | ADRP | Γ<7:0> | | | |
| bit 7 | | | | | | | bit 0 |
| | | | | | | | |
| Legend: | | | | | | | |

U		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 Unimplemented: Read as '0'

bit 7-0 **ADRPT<7:0>**: ADC Repeat Threshold bits Counts the number of times that the ADC has been triggered and is used along with ADCNT to determine when the error threshold is checked when the computation is Low-pass Filter, Burst Average, or Average modes. See Table 31-3 for more details.

32.4 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the CxHYS bit of the CMxCON0 register.

See Comparator Specifications in Table 37-15 for more information.

32.5 Timer1/3/5 Gate Operation

The output resulting from a comparator operation can be used as a source for gate control of Timer1/3/5. See **Section 19.8 "Timer1/3/5 Gate"** for more information. This feature is useful for timing the duration or interval of an analog event.

It is recommended that the comparator output be synchronized to Timer1. This ensures that Timer1 does not increment while a change in the comparator is occurring.

32.5.1 COMPARATOR OUTPUT SYNCHRONIZATION

The output from a comparator can be synchronized with Timer1 by setting the SYNC bit of the CMxCON0 register.

Once enabled, the comparator output is latched on the falling edge of the Timer1 source clock. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 32-2) and the Timer1 Block Diagram (Figure 19-1) for more information.

32.6 Comparator Interrupt

An interrupt can be generated upon a change in the output value of the comparator for each comparator, a rising edge detector and a falling edge detector are present.

When either edge detector is triggered and its associated enable bit is set (CxINTP and/or CxINTN bits of the CMxCON1 register), the Corresponding Interrupt Flag bit (CxIF bit of the PIR2 register) will be set.

To enable the interrupt, you must set the following bits:

- EN and POL bits of the CMxCON0 register
- CxIE bit of the PIE2 register
- INTP bit of the CMxCON1 register (for a rising edge detection)
- INTN bit of the CMxCON1 register (for a falling edge detection)
- PEIE and GIE bits of the INTCON register

The associated interrupt flag bit, CxIF bit of the PIR2 register, must be cleared in software. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

Note: Although a comparator is disabled, an interrupt can be generated by changing the output polarity with the CxPOL bit of the CMxCON0 register, or by switching the comparator on or off with the CxEN bit of the CMxCON0 register.

32.7 Comparator Positive Input Selection

Configuring the PCH<2:0> bits of the CMxPCH register directs an internal voltage reference or an analog pin to the non-inverting input of the comparator:

- CxIN0+, CxIN1+ analog pin
- DAC output
- FVR (Fixed Voltage Reference)
- AVss (Ground)

See Section 28.0 "Fixed Voltage Reference (FVR)" for more information on the Fixed Voltage Reference module.

See Section 30.0 "5-Bit Digital-to-Analog Converter (DAC) Module" for more information on the DAC input signal.

Any time the comparator is disabled (CxEN = 0), all comparator inputs are disabled.

32.8 Comparator Negative Input Selection

The NCH<2:0> bits of the CMxNCH register direct an analog input pin and internal reference voltage or analog ground to the inverting input of the comparator:

- · CxIN0-, CxIN1-, CxIN2-, CxIN3- analog pin
- FVR (Fixed Voltage Reference)
- Analog Ground

Note: To use CxINy+ and CxINy- pins as analog input, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.



FIGURE 35-1:	General Format for Instructions	
	Byte-oriented file register operations	Example Instruction
	15 10 9 8 7 0 OPCODE d a f (FILE #) d = 0 for result destination to be WREG register d = 1 for result destination to be file register (f) a = 0 to force Access Bank a = 1 for BSR to select bank f = 8-bit file register address	ADDWF MYREG, W, B
	Byte to Byte move operations (2-word)	
	15 12 11 0 OPCODE f (Source FILE #) 15 12 11 0 1111 f (Destination FILE #) f = 12-bit file register address	MOVFF MYREG1, MYREG2
	Bit-oriented file register operations	
	15 12 11 9 8 7 0 OPCODE b (BIT #) a f (FILE #) b = 3-bit position of bit in file register (f) a = 0 to force Access Bank a = 1 for BSR to select bank f = 8-bit file register address	BSF MYREG, bit, B
	Literal operations	
	15 8 7 0 OPCODE k (literal) k = 8-bit immediate value	MOVLW 7Fh
	Control operations	
	CALL, GOTO and Branch operations	
	15 8 7 0 OPCODE n<7:0> (literal) 15 12 11 0 1111 n<19:8> (literal)	GOTO Label
	n = 20-bit immediate value	
	15 8 7 0 OPCODE S n<7:0> (literal) 15 12 11 0 1111 n<19:8> (literal) S = Fast bit	CALL MYFUNC
	15 11 10 0 OPCODE n<10:0> (literal)	BRA MYFUNC
	15 8 7 0 OPCODE n<7:0> (literal)	BC MYFUNC

PIC18(L)F24/25K40

RRN	ICF	Rota	Rotate Right f (No Carry)							
Synta	ax:	RRN	CF	f {,d {,	a}}					
Oper	ands:	0 ≤ f d ∈ [a ∈ [$0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$							
Oper	ation:	(f <n> (f<0></n>	$(\cdot) \rightarrow (\cdot)$	dest <n dest<7</n 	– 1>, '>					
Statu	is Affected:	N, Z	N, Z							
Enco	oding:	01	00	00d	la ff	ff	ffff			
Desc	ription:	The contents of register 'f' are rotated one bit to the right. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). If 'a' is '0', the Access Bank will be selected (default), overriding the BSR value. If 'a' is '1', then the bank will be selected as per the BSR value. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Sec- tion 35.2.3 "Byte-Oriented and Bit- Oriented Instructions in Indexed Lit- eral Offset Mode" for details.								
Word	ls:	1								
Cycle	es:	1								
QC	ycle Activity:									
	Q1	Q	2		Q3		Q4			
	Decode	Re regist	ad ær 'f'	Р	rocess Data	۷ de	Vrite to stination			
<u>Exan</u>	nple 1: Before Instruc REG After Instructic REG	RRNC tion = 1 on = 1	2F 101 110	REG, 0111 1011	1, 0					
Exan	nple <u>2</u> :	RRNO	F	REG,	0, 0					
	Before Instruc	tion								
	W REG After Instructio	= ? = 1 on	101	0111						
	w REG	= 1 = 1	110 101	1011 0111						

SETF	Set f						
Syntax:	SETF f{,;	a}					
Operands:	0 ≤ f ≤ 255 a ∈ [0,1]						
Operation:	$FFh\tof$						
Status Affected:	None						
Encoding:	0110	100a	ffff	ffff			
Description:	The conten are set to F If 'a' is '0', t If 'a' is '1', t GPR bank. If 'a' is '0' a set is enabl in Indexed mode when tion 35.2.3 Oriented Ir eral Offset	The contents of the specified register are set to FFh. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Sec- tion 35.2.3 "Byte-Oriented and Bit- Oriented Instructions in Indexed Lit- eral Offset Mode" for details					
Words:	1						
Cycles:	1						
Q Cycle Activity:							
Q1	Q2	Q3	1	Q4			
Decode	Read register 'f'	Proce Data	ess a re	Write egister 'f'			
Example: Before Instruc	SETF tion = 54	REG	;, 1				

REG	=	5Ah
After Instruction		
REG	=	FFh

PIC18LF24/25K40				Standard Operating Conditions (unless otherwise stated)					
PIC18F2	24/25K40			Standard Operating Conditions (unless otherwise stated) VREGPM = 1					otherwise stated)
Param.	0h.e.l	Device Oberratoriation		T 4	Max.	Max.	Unite		Conditions
No.	Symbol	Device Characteristics	Min.	Typ.†	+85°C	+125°C	Units	VDD	Note
D200	IPD	IPD Base	—	0.05	2	9	μΑ	3.0V	
D200	IPD	IPD Base		0.4	4	12	μΑ	3.0V	
D200A				20	_	_	μΑ	3.0V	VREGPM = 0
D201	IPD_WDT	Low-Frequency Internal Oscillator/ WDT	—	0.4	3	10	μA	3.0V	
D201	IPD_WDT	Low-Frequency Internal Oscillator/ WDT	_	0.6	5	13	μΑ	3.0V	
D202	IPD_SOSC	Secondary Oscillator (Sosc)	_	0.6	5	13	μΑ	3.0V	
D202	IPD_SOSC	Secondary Oscillator (SOSC)	-	0.8	8.5	15	μΑ	3.0V	
D203	IPD_FVR	FVR		31	—	—	μΑ	3.0V	FVRCON = 0X81 or 0x84
D203	IPD_FVR	FVR		32	_	—	μΑ	3.0V	FVRCON = 0X81 or 0x84
D204	IPD_BOR	Brown-out Reset (BOR)	_	9	14	18	μΑ	3.0V	
D204	IPD_BOR	Brown-out Reset (BOR)	_	14	19	21	μΑ	3.0V	
D205	IPD_LPBOR	Low-Power Brown-out Reset (LPBOR)	-	0.5	_	_	μΑ	3.0V	
D205	IPD_LPBOR	Low-Power Brown-out Reset (LPBOR)		0.7	_	_	μΑ	3.0V	
D206	IPD_HLVD	High/Low Voltage Detect (HLVD)	-	31	_	_	μΑ	3.0V	
D206	IPD_HLVD	High/Low Voltage Detect (HLVD)	-	32	_	_	μΑ	3.0V	
D207	IPD_ADCA	ADC - Active		250	_	_	μΑ	3.0V	ADC is converting (4)
D207	IPD_ADCA	ADC - Active	_	280	_	—	μΑ	3.0V	ADC is converting (4)
D208	IPD_CMP	Comparator		25	38	40	μΑ	3.0V	
D208	IPD CMP	Comparator	_	28	50	60	μA	3.0V	

TABLE 37-3: POWER-DOWN CURRENT (IPD)^(1,2)

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD and the additional current consumed when this peripheral is enabled. The peripheral △ current can be determined by subtracting the base IDD or IPD current from this limit. Max. values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode with all I/O pins in high-impedance state and tied to Vss.

3: All peripheral currents listed are on a per-peripheral basis if more than one instance of a peripheral is available.

4: ADC clock source is FRC.

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Ν	ILLIMETER	S	
Dimension	MIN	NOM	MAX	
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	С		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A