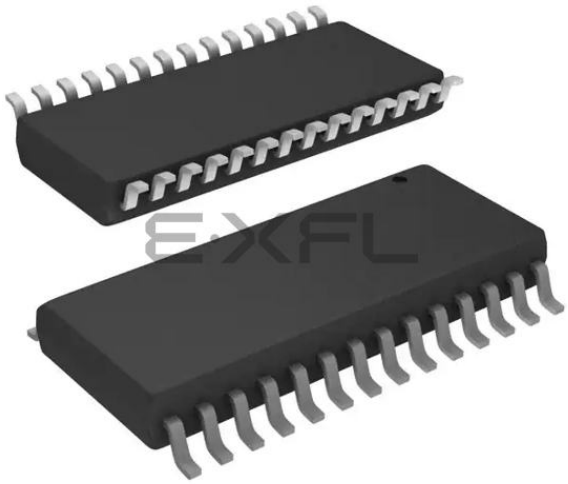

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf24k40t-i-so

REGISTER 3-4: Configuration Word 2H (30 0003h): Supervisor

R/W-1	U-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{XINST}}$	—	$\overline{\text{DEBUG}}$	STVREN	PPS1WAY	$\overline{\text{ZCD}}$	BORV<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '1'	
-n = Value for blank device	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{XINST}}$:** Extended Instruction Set Enable bit
1 = Extended Instruction Set and Indexed Addressing mode disabled (Legacy mode)
0 = Extended Instruction Set and Indexed Addressing mode enabled

bit 6 **Unimplemented:** Read as '1'

bit 5 **$\overline{\text{DEBUG}}$:** Debugger Enable bit
1 = Background debugger disabled
0 = Background debugger enabled

bit 4 **STVREN:** Stack Overflow/Underflow Reset Enable bit
1 = Stack Overflow or Underflow will cause a Reset
0 = Stack Overflow or Underflow will not cause a Reset

bit 3 **PPS1WAY:** PPSLOCKED bit One-Way Set Enable bit
1 = The PPSLOCKED bit can only be set once after an unlocking sequence is executed; once PPSLOCK is set, all future changes to PPS registers are prevented
0 = The PPSLOCKED bit can be set and cleared as needed (provided an unlocking sequence is executed)

bit 2 **$\overline{\text{ZCD}}$:** ZCD Disable bit
1 = ZCD disabled. ZCD can be enabled by setting the ZCDSEN bit of ZCDCON
0 = ZCD always enabled, ZCDMD bit is ignored

bit 1-0 **BORV<1:0>:** Brown-out Reset Voltage Selection bit(1)
PIC18F2xK40 device:
11 = Brown-out Reset Voltage (V_{BOR}) set to 2.45V
10 = Brown-out Reset Voltage (V_{BOR}) set to 2.45V
01 = Brown-out Reset Voltage (V_{BOR}) set to 2.7V
00 = Brown-out Reset Voltage (V_{BOR}) set to 2.85V

PIC18LF2xK40 device:
11 = Brown-out Reset Voltage (V_{BOR}) set to 1.90V
10 = Brown-out Reset Voltage (V_{BOR}) set to 2.45V
01 = Brown-out Reset Voltage (V_{BOR}) set to 2.7V
00 = Brown-out Reset Voltage (V_{BOR}) set to 2.85V

Note 1: The higher voltage setting is recommended for operation at or above 16 MHz.

3.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data memory are controlled independently. Internal access to the program memory is unaffected by any code protection setting.

3.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the $\overline{CP}$ bit in Configuration Words. When $\overline{CP}$ = 0, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Self-writing the program memory is dependent upon the write protection setting. See **Section 3.4 "Write Protection"** for more information.

3.3.2 DATA MEMORY PROTECTION

The entire Data EEPROM Memory space is protected from external reads and writes by the $\overline{CPD}$ bit in the Configuration Words. When $\overline{CPD}$ = 0, external reads and writes of Data EEPROM Memory are inhibited and a read will return all '0's. The CPU can continue to read Data EEPROM Memory regardless of the protection bit settings.

3.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as boot loader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Words define the size of the program memory block that is protected.

3.5 User ID

Eight words in the memory space (200000h-200000Fh) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 11.2 "User ID, Device ID and Configuration Word Access"** for more information on accessing these memory locations. For more information on checksum calculation, see the "PIC18(L)F2X/4XK40 Memory Programming Specification" (DS40001772).

4.2 Register Definitions: Oscillator Control

REGISTER 4-1: OSCCON1: OSCILLATOR CONTROL REGISTER1

U-0	R/W-f/f	R/W-f/f	R/W-f/f	R/W-q/q	R/W-q/q	R/W-q/q	R/W-q/q
—	NOSC<2:0>			NDIV<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	f = determined by fuse setting
		q = Reset value is determined by hardware

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **NOSC<2:0>:** New Oscillator Source Request bits(1,2,3)
The setting requests a source oscillator and PLL combination per Table 4-2.
POR value = RSTOSC (Register 3-1).

bit 3-0 **NDIV<3:0>:** New Divider Selection Request bits(2,3)
The setting determines the new postscaler division ratio per Table 4-2.

Note 1: The default value (f/f) is determined by the RSTOSC Configuration bits. See Table 4-1below.
2: If NOSC is written with a reserved value (Table 4-2), the operation is ignored and neither NOSC nor NDIV is written.
3: When CSWEN = 0, this register is read-only and cannot be changed from the POR value.

TABLE 4-1: DEFAULT OSCILLATOR SETTINGS USING RSTOSC BITS

RSTOSC	SFR Reset Values			Initial FOSC Frequency
	NOSC/COSC	CDIV	OSCFRQ	
111	111	1:1	4 MHz	EXTOSC per FEXTOSC
110	110	4:1		FOSC = 1 MHz (4 MHz/4)
101	101	1:1		LFINTOSC
100	100	1:1		SOSC
011	Reserved			
010	010	1:1	4 MHz	EXTOSC + 4xPLL (1)
001	Reserved			
000	110	1:1	64 MHz	FOSC = 64 MHz

Note 1: EXTOSC must meet the PLL specifications (Table 37-9).

5.5 Register Definitions: Reference Clock

Long bit name prefixes for the Reference Clock peripherals are shown in Table 5-1. Refer to **Section 1.4.2.2 "Long Bit Names"** for more information.

TABLE 5-1:

Peripheral	Bit Name Prefix
CLKR	CLKR

REGISTER 5-1: CLKRCON: REFERENCE CLOCK CONTROL REGISTER

R/W-0/0	U-0	U-0	R/W-1/1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN	—	—	DC<1:0>		DIV<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** Reference Clock Module Enable bit
- 1 = Reference clock module enabled
- 0 = Reference clock module is disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 4-3 **DC<1:0>:** Reference Clock Duty Cycle bits(1)
- 11 = Clock outputs duty cycle of 75%
- 10 = Clock outputs duty cycle of 50%
- 01 = Clock outputs duty cycle of 25%
- 00 = Clock outputs duty cycle of 0%

bit 2-0 **DIV<2:0>:** Reference Clock Divider bits
- 111 = Base clock value divided by 128
- 110 = Base clock value divided by 64
- 101 = Base clock value divided by 32
- 100 = Base clock value divided by 16
- 011 = Base clock value divided by 8
- 010 = Base clock value divided by 4
- 001 = Base clock value divided by 2
- 000 = Base clock value

Note 1: Bits are valid for reference clock divider values of two or larger, the base clock cannot be further divided.

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	166
PIE0	—	—	TMR0IE	IOCIE	—	INT2IE	INT1IE	INT0IE	175
PIE1	OSCFIE	CSWIE	—	—	—	—	ADTIE	ADIE	176
PIE2	HLVDIE	ZCDIE	—	—	—	—	C2IE	C1IE	177
PIE3	—	—	RC1IE	TX1IE	—	—	BCL1IE	SSP1IE	178
PIE4	—	—	TMR6IE	TMR5IE	TMR4IE	TMR3IE	TMR2IE	TMR1IE	179
PIE5	—	—	—	—	—	TMR5GIE	TMR3GIE	TMR1GIE	180
PIE6	—	—	—	—	—	—	CCP2IE	CCP1IE	181
PIE7	SCANIE	CRCIE	NVMIE	—	—	—	—	CWG1IE	182
PIR0	—	—	TMR0IF	IOCIF	—	INT2IF	INT1IF	INT0IF	167
PIR1	OSCFIF	CSWIF	—	—	—	—	ADTIF	ADIF	168
PIR2	HLVDIF	ZCDIF(1)	—	—	—	—	C2IF	C1IF	169
PIR3	—	—	RC1IF	TX1IF	—	—	BCL1IF	SSP1IF	170
PIR4	—	—	TMR6IF	TMR5IF	TMR4IF	TMR3IF	TMR2IF	TMR1IF	170
IOCAP	—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	206
IOCAN	—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	206
IOCAF	—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	206
IOCCP(1)	—	—	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0	206
IOCCN(1)	—	—	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	206
IOCCF(1)	—	—	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0	206
STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	114
VREGCON	—	—	—	—	—	—	VREGPM	Reserved	60
CPUDOZE	IDLEN	DOZEN	ROI	DOE	—	DOZE<2:0>			61
WDTCON0	—	—	WDTPS<4:0>					SEN	81
WDTCON1	—	WDTPS<2:0>			—	WINDOW<2:0>			82

Note 1: — = unimplemented location, read as '0'. Shaded cells are not used in Power-Down mode.

TABLE 10-5: REGISTER FILE SUMMARY FOR PIC18(L)F24/25K40 DEVICES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
FFFh	TOSU	—	—	—	Top of Stack Upper byte (TOS<20:16>)					---xxxxx
FFEh	TOSH	Top of Stack High byte (TOS<15:8>)								xxxxxxxx
FFDh	TOSL	Top of Stack Low byte (TOS<7:0>)								xxxxxxxx
FFCh	STKPTR	—	—	—	STKPTR<4:0>					--000000
FFBh	PCLATU	—	—	—	Holding Register for PC<20:16>					---00000
FFAh	PCLATH	Holding Register for PC<15:8>								00000000
FF9h	PCL	PC Low byte (PC<7:0>)								00000000
FF8h	TBLPTRU	—	—	Program Memory Table Pointer (TBLPTR<21:16>)						--000000
FF7h	TBLPTRH	Program Memory Table Pointer (TBLPTR<15:8>)								00000000
FF6h	TBLPTRL	Program Memory Table Pointer (TBLPTR<7:0>)								00000000
FF5h	TABLAT	TABLAT								00000000
FF4h	PRODH	Product Register High byte								xxxxxxxx
FF3h	PRODL	Product Register Low byte								xxxxxxxx
FF2h	INTCON	GIE/GIEH	PEIE/GIEL	IPEN	—	—	INT2EDG	INT1EDG	INT0EDG	000--111
FF1h	—	Unimplemented								—
FF0h	—	Unimplemented								—
FEFh	INDF0	Uses contents of FSR0 to address data memory – value of FSR0 not changed (not a physical register)								--------
FEEh	POSTINC0	Uses contents of FSR0 to address data memory – value of FSR0 post-incremented (not a physical register)								--------
FEDh	POSTDEC0	Uses contents of FSR0 to address data memory – value of FSR0 post-decremented (not a physical register)								--------
FECh	PREINC0	Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented (not a physical register)								--------
FEBh	PLUSW0	Uses contents of FSR0 to address data memory – value of FSR0 pre-incremented (not a physical register) – value of FSR0 offset by W								--------
FEAh	FSR0H	—	—	—	—	Indirect Data Memory Address Pointer 0 High				----xxxx
FE9h	FSR0L	Indirect Data Memory Address Pointer 0 Low								xxxxxxxx
FE8h	WREG	Working Register								xxxxxxxx
FE7h	INDF1	Uses contents of FSR0 to address data memory – value of FSR1 not changed (not a physical register)								--------
FE6h	POSTINC1	Uses contents of FSR0 to address data memory – value of FSR1 post-incremented (not a physical register)								--------
FE5h	POSTDEC1	Uses contents of FSR0 to address data memory – value of FSR1 post-decremented (not a physical register)								--------
FE4h	PREINC1	Uses contents of FSR0 to address data memory – value of FSR1 pre-incremented (not a physical register)								--------
FE3h	PLUSW1	Uses contents of FSR0 to address data memory – value of FSR1 pre-incremented (not a physical register) – value of FSR0 offset by W								--------

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition
Note 1: Not available on LF devices.

11.1.5 ERASING PROGRAM FLASH MEMORY

The minimum erase block is 32 or 64 words (refer to Table 11-3). Only through the use of an external programmer, or through ICSP™ control, can larger blocks of program memory be bulk erased. Word erase in the Flash array is not supported.

For example, when initiating an erase sequence from a microcontroller with erase row size of 32 words, a block of 32 words (64 bytes) of program memory is erased. The Most Significant 16 bits of the TBLPTR<21:6> point to the block being erased. The TBLPTR<5:0> bits are ignored.

The NVMCON1 register commands the erase operation. The NVMREG<1:0> bits must be set to point to the Program Flash Memory. The WREN bit must be set to enable write operations. The FREE bit is set to select an erase operation.

The NVM unlock sequence described in **Section 11.1.4 "NVM Unlock Sequence"** should be used to guard against accidental writes. This is sometimes referred to as a long write.

A long write is necessary for erasing the internal Flash. Instruction execution is halted during the long write cycle. The long write is terminated by the internal programming timer.

11.1.5.1 Program Flash Memory Erase Sequence

The sequence of events for erasing a block of internal program memory is:

1. NVMREG bits of the NVMCON1 register point to PFM
2. Set the FREE and WREN bits of the NVMCON1 register
3. Perform the unlock sequence as described in **Section 11.1.4 "NVM Unlock Sequence"**

If the PFM address is write-protected, the WR bit will be cleared and the erase operation will not take place, WRERR is signaled in this scenario.

The operation erases the memory row indicated by masking the LSBs of the current TBLPTR.

While erasing PFM, CPU operation is suspended and it resumes when the operation is complete. Upon completion the WR bit is cleared in hardware, the NVMIF is set and an interrupt will occur if the NVMIE bit is also set.

Write latch data is not affected by erase operations and WREN will remain unchanged.

Note 1:	If a write or erase operation is terminated by an unexpected event, WRERR bit will be set which the user can check to decide whether a rewrite of the location(s) is needed.
2:	WRERR is set if WR is written to '1' while TBLPTR points to a write-protected address.
3:	WRERR is set if WR is written to '1' while TBLPTR points to an invalid address location (Table 10-2 and Table 11-1).

11.3.6 OPERATION DURING CODE-PROTECT

Data EEPROM Memory has its own code-protect bits in Configuration Words. External read and write operations are disabled if code protection is enabled.

If the Data EEPROM is write-protected or if NVMADR points an invalid address location, the WR bit is cleared without any effect. WRERR is signaled in this scenario.

11.3.7 PROTECTION AGAINST SPURIOUS WRITE

There are conditions when the user may not want to write to the Data EEPROM Memory. To protect against spurious EEPROM writes, various mechanisms have been implemented. On power-up, the WREN bit is cleared. In addition, writes to the EEPROM are blocked during the Power-up Timer period (TPWRT).

The unlock sequence and the WREN bit together help prevent an accidental write during brown-out, power glitch or software malfunction.

11.3.8 ERASING THE DATA EEPROM MEMORY

Data EEPROM Memory can be erased by writing 0xFF to all locations in the Data EEPROM Memory that needs to be erased.

EXAMPLE 11-7: DATA EEPROM REFRESH ROUTINE

```
        CLRF      NVMADRL             ; Clear address low byte register
        CLRF      NVMADRH             ; Clear address high byte register (if applicable)
        BCF       NVMCON1, NVMREG0    ; Set access for EEPROM
        BCF       NVMCON1, NVMREG1    ; Set access for EEPROM
        SETF      NVMDAT              ; Load 0xFF to data register
        BCF       INTCON, GIE         ; Disable interrupts
        BSF       NVMCON1, WREN       ; Enable writes
Loop                                  ; Loop to refresh array
        MOVLW     0x55                ; Initiate unlock sequence
        MOVWF     NVMCON2             ;
        MOVLW     0xAA                ;
        MOVWF     NVMCON2             ;
        BSF       NVMCON1, WR         ; Set WR bit to begin write
        BTFSC     NVMCON1, WR         ; Wait for write to complete
        BRA       $-2
        INCFSZ    NVMADRL, F          ; Increment address low byte
        BRA       Loop                ; Not zero, do it again

 //The following 4 lines of code are not needed if the part doesn't have NVMADRH register
        INCF      NVMADRH, F          ; Decrement address high byte
        MOVLW     0x03                ; Move 0x03 to working register
        CPFSGT    NVMADRH             ; Compare address high byte with working register
        BRA       Loop                ; Skip if greater than working register
                                      ; Else go back to erase loop

        BCF       NVMCON1, WREN       ; Disable writes
        BSF       INTCON, GIE         ; Enable interrupts
```

20.5 Operation Examples

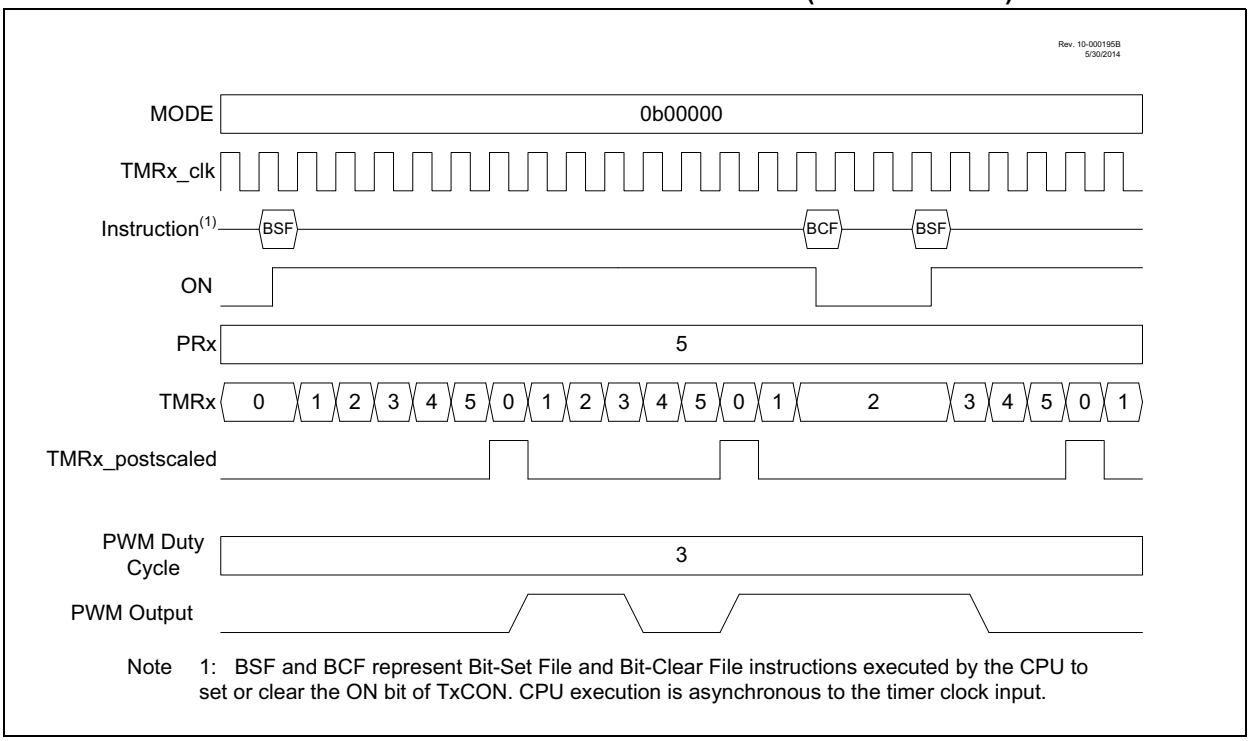
Unless otherwise specified, the following notes apply to the following timing diagrams:

- Both the prescaler and postscaler are set to 1:1 (both the CKPS and OUTPS bits in the TxCON register are cleared).
- The diagrams illustrate any clock except Fosc/4 and show clock-sync delays of at least two full cycles for both ON and Timer2_ers. When using Fosc/4, the clock-sync delay is at least one instruction period for Timer2_ers; ON applies in the next instruction period.
- The PWM Duty Cycle and PWM output are illustrated assuming that the timer is used for the PWM function of the CCP module as described in **Section 21.0 "Capture/Compare/PWM Module"**. The signals are not a part of the Timer2 module.

20.5.1 SOFTWARE GATE MODE

This mode corresponds to legacy Timer2 operation. The timer increments with each clock input when ON = 1 and does not increment when ON = 0. When the TMRx count equals the PRx period count the timer resets on the next clock and continues counting from 0. Operation with the ON bit software controlled is illustrated in Figure 20-4. With PRx = 5, the counter advances until TMRx = 5, and goes to zero with the next clock.

FIGURE 20-4: SOFTWARE GATE MODE TIMING DIAGRAM (MODE = 00000)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

REGISTER 21-3: CCPxCAP: CAPTURE INPUT SELECTION MULTIPLEXER REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/x	R/W-0/x
—	—	—	—	—	—	CTS<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **CTS<1:0>:** Capture Trigger Input Selection bits

CTS<1:0>	**Connection**	
	CCP1	**CCP2**
11	IOC_Interrupt	
10	CMP2_output	
01	CMP1_output	
00	Pin selected by CCP1PPS	Pin selected by CCP2PPS

REGISTER 21-4: CCPRxL: CCPx REGISTER LOW BYTE

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
CCPRx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 MODE = Capture Mode:
CCPRxL<7:0>: LSB of captured TMR1 value
MODE = Compare Mode:
CCPRxL<7:0>: LSB compared to TMR1 value
MODE = PWM Mode && FMT = 0:
CCPRxL<7:0>: CCPW<7:0> – Pulse-Width LS 8 bits
MODE = PWM Mode && FMT = 1:
CCPRxL<7:6>: CCPW<1:0> – Pulse-Width LS 2 bits
CCPRxL<5:0>: Not used

21.3 Capture Mode

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the capture source, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMRxH:TMRxL register pair, respectively. An event is defined as one of the following and is configured by the MODE<3:0> bits of the CCPxCON register:

- Every falling edge of CCPx input
- Every rising edge of CCPx input
- Every 4th rising edge of CCPx input
- Every 16th rising edge of CCPx input
- Every edge of CCPx input (rising or falling)

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIR6 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH:CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

Note:	If an event occurs during a 2-byte read, the high and low-byte data will be from different events. It is recommended while reading the CCPRxH:CCPRxL register pair to either disable the module or read the register pair twice for data integrity.

Figure 21-1 shows a simplified diagram of the capture operation.

21.3.1 CAPTURE SOURCES

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

Note:	If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

The capture source is selected by configuring the CTS<1:0> bits of the CCPxCAP register. The following sources can be selected:

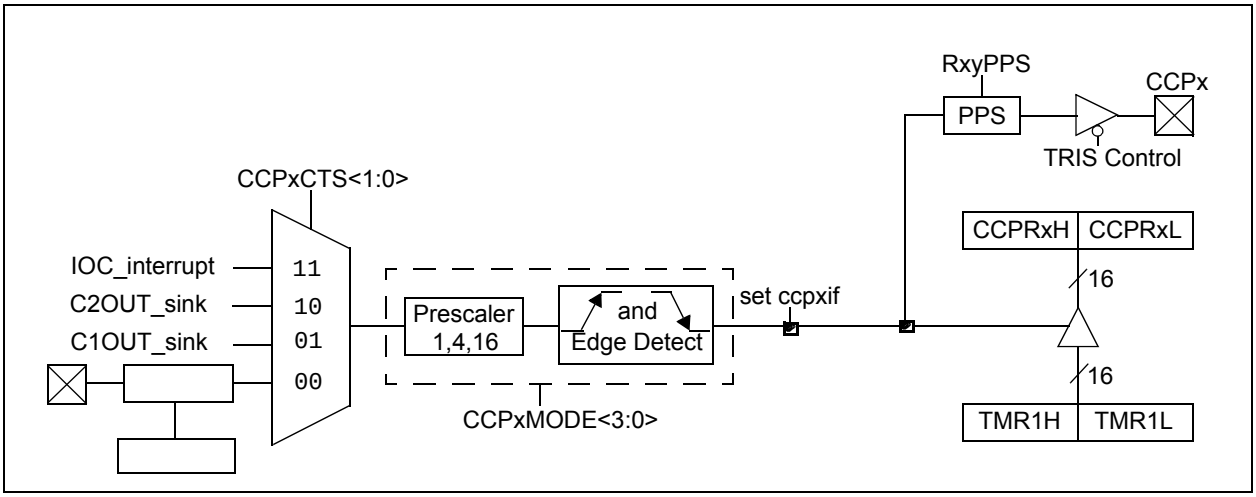
- Pin selected by CCPxPPS
- C1_output
- C2_output
- IOC_interrupt

21.3.2 TIMER1 MODE RESOURCE

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

- See **Section 19.0 "Timer1/3/5 Module with Gate Control"** for more information on configuring Timer1.

FIGURE 21-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



REGISTER 24-5: CWG1STR(1): CWG STEERING CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
OVRD	OVRC	OVRB	OVRA	STRD(2)	STRC(2)	STRB(2)	STRA(2)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **OVRD:** Steering Data D bit

bit 6 **OVRC:** Steering Data C bit

bit 5 **OVRB:** Steering Data B bit

bit 4 **OVRA:** Steering Data A bit

bit 3 **STRD:** Steering Enable bit D(2)
1 = CWG1D output has the CWG data input waveform with polarity control from POLD bit
0 = CWG1D output is assigned to value of OVRD bit

bit 2 **STRC:** Steering Enable bit C(2)
1 = CWG1C output has the CWG data input waveform with polarity control from POLC bit
0 = CWG1C output is assigned to value of OVRC bit

bit 1 **STRB:** Steering Enable bit B(2)
1 = CWG1B output has the CWG data input waveform with polarity control from POLB bit
0 = CWG1B output is assigned to value of OVRB bit

bit 0 **STRA:** Steering Enable bit A(2)
1 = CWG1A output has the CWG data input waveform with polarity control from POLA bit
0 = CWG1A output is assigned to value of OVRA bit

Note 1: The bits in this register apply only when MODE<2:0> = 00x (Register 24-1, Steering modes).
2: This bit is double-buffered when MODE<2:0> = 001.

FIGURE 26-7: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

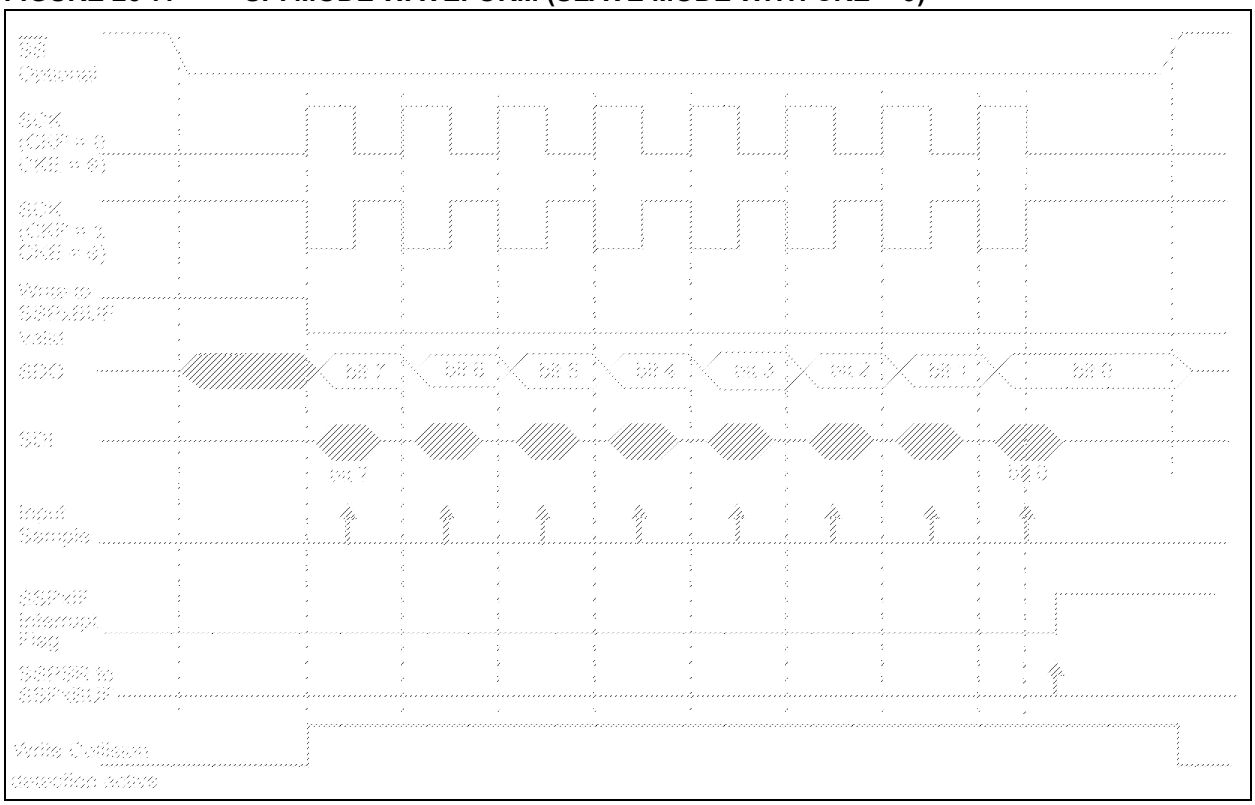
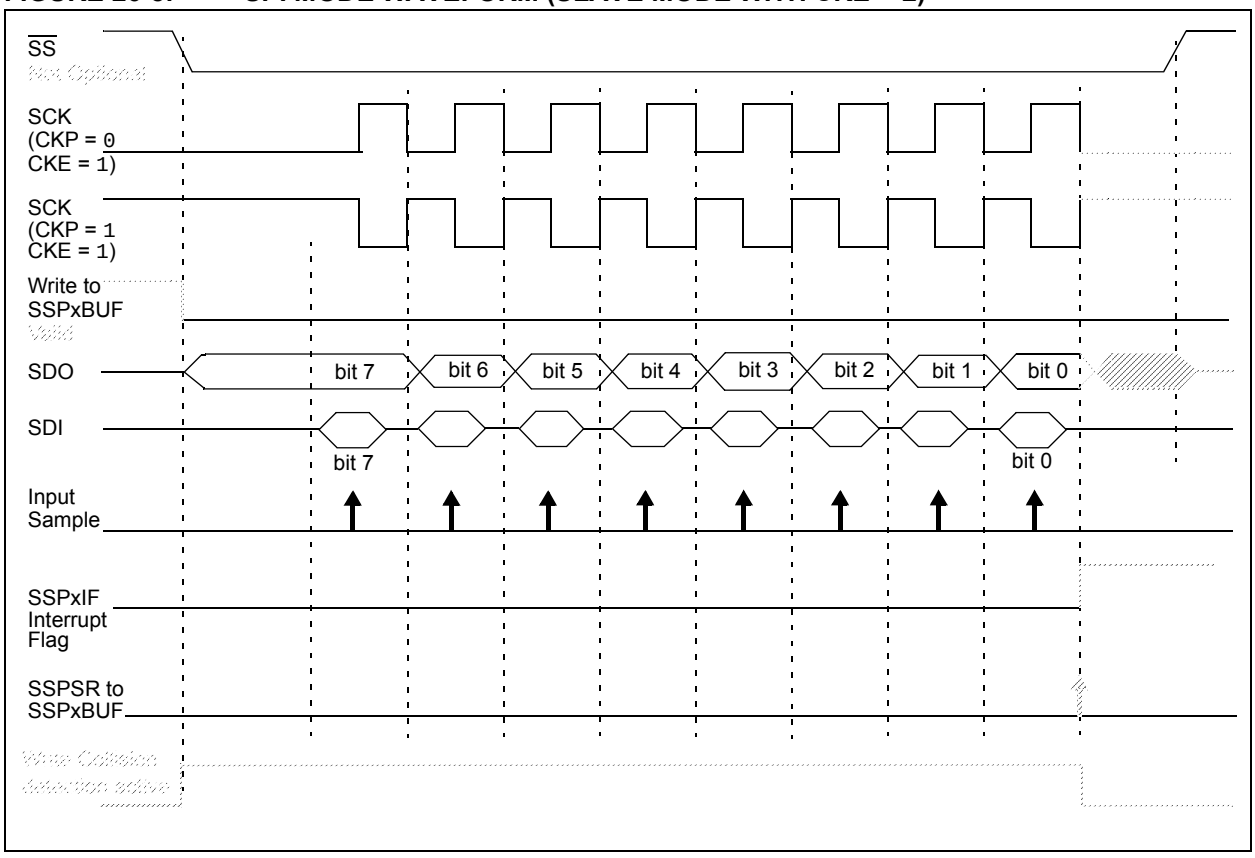


FIGURE 26-8: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



26.10.13.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDA when SCL goes from low level to high level (Case 1).

b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1' (Case 2).

When the user releases SDA and the pin is allowed to float high, the BRG is loaded with SSPxADD and counts down to zero. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 26-36). If SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high-to-low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition, see Figure 26-37.

If, at the end of the BRG time out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

FIGURE 26-36: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

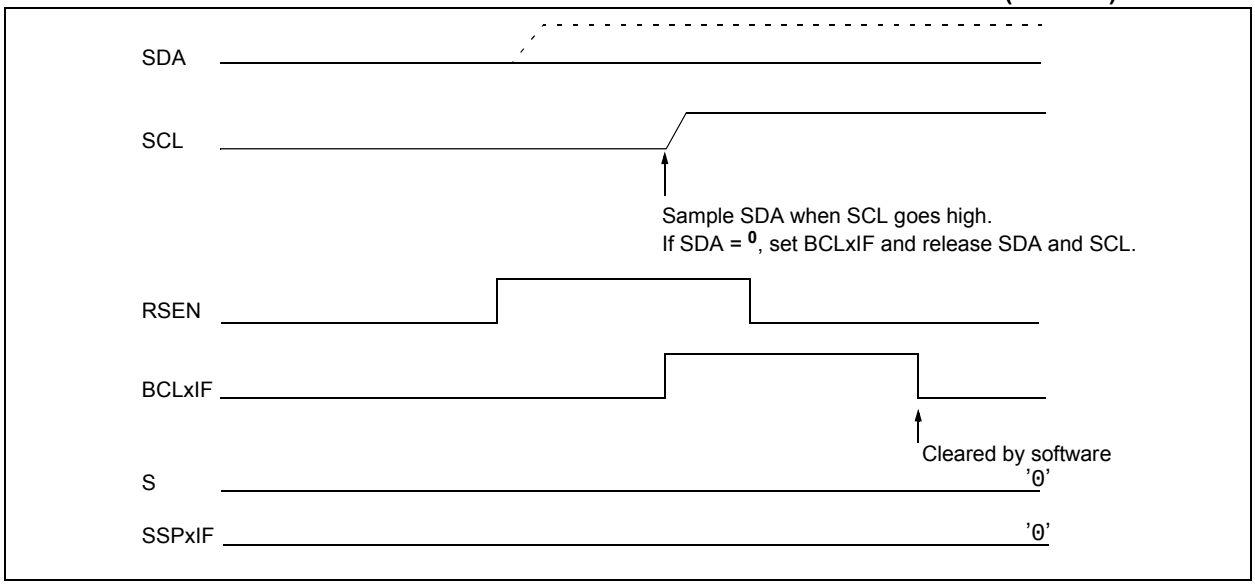
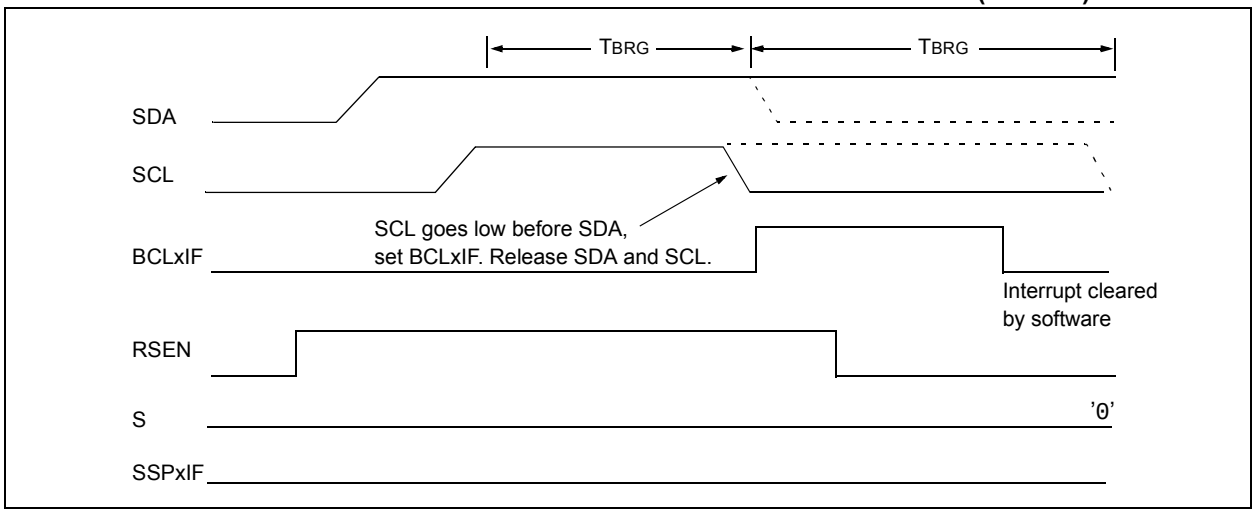


FIGURE 26-37: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)



27.5.1.5 Synchronous Master Reception

Data is received at the RXx/DTx pin. The RXx/DTx pin output driver is automatically disabled when the EUSART is configured for synchronous master receive operation.

In Synchronous mode, reception is enabled by setting either the Single Receive Enable bit (SREN of the RCxSTA register) or the Continuous Receive Enable bit (CREN of the RCxSTA register).

When SREN is set and CREN is clear, only as many clock cycles are generated as there are data bits in a single character. The SREN bit is automatically cleared at the completion of one character. When CREN is set, clocks are continuously generated until CREN is cleared. If CREN is cleared in the middle of a character the CK clock stops immediately and the partial character is discarded. If SREN and CREN are both set, then SREN is cleared at the completion of the first character and CREN takes precedence.

To initiate reception, set either SREN or CREN. Data is sampled at the RXx/DTx pin on the trailing edge of the TX/CK clock pin and is shifted into the Receive Shift Register (RSR). When a complete character is received into the RSR, the RCxIF bit is set and the character is automatically transferred to the two character receive FIFO. The Least Significant eight bits of the top character in the receive FIFO are available in RCxREG. The RCxIF bit remains set as long as there are unread characters in the receive FIFO.

Note:	If the RX/DT function is on an analog pin, the corresponding ANSEL bit must be cleared for the receiver to function.

27.5.1.6 Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TXx/CKx pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

Note:	If the device is configured as a slave and the TX/CK function is on an analog pin, the corresponding ANSEL bit must be cleared.

27.5.1.7 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RCxREG is read to access the FIFO. When this happens the OERR bit of the RCxSTA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear then the error is cleared by reading RCxREG. If the overrun occurred when the CREN bit is set then the error condition is cleared by either clearing the CREN bit of the RCxSTA register or by clearing the SPEN bit which resets the EUSART.

27.5.1.8 Receiving 9-Bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCxSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCxSTA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCxREG.

27.5.1.9 Synchronous Master Reception Setup:

1. Initialize the SPxBRGH:SPxBRGL register pair for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Clear the ANSEL bit for the RXx pin (if applicable).
3. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
4. Ensure bits CREN and SREN are clear.
5. If interrupts are desired, set the RCxIE bit of the PIE3 register and the GIE and PEIE bits of the INTCON register.
6. If 9-bit reception is desired, set bit RX9.
7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
8. Interrupt flag bit RCxIF will be set when reception of a character is complete. An interrupt will be generated if the enable bit RCxIE was set.
9. Read the RCxSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
10. Read the 8-bit received data by reading the RCxREG register.
11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCxSTA register or by clearing the SPEN bit which resets the EUSART.

28.0 FIXED VOLTAGE REFERENCE (FVR)

The Fixed Voltage Reference, or FVR, is a stable voltage reference, independent of VDD, with 1.024V, 2.048V or 4.096V selectable output levels. The output of the FVR can be configured to supply a reference voltage to the following:

- ADC input channel
- ADC positive reference
- Comparator input
- Digital-to-Analog Converter (DAC)

The FVR can be enabled by setting the FVREN bit of the FVRCON register.

Note:	Fixed Voltage Reference output cannot exceed VDD.

28.1 Independent Gain Amplifiers

The output of the FVR, which is connected to the ADC, Comparators, and DAC, is routed through two independent programmable gain amplifiers. Each amplifier can be programmed for a gain of 1x, 2x or 4x, to produce the three possible voltage levels.

The ADFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the ADC module. Reference **Section 31.0 "Analog-to-Digital Converter with Computation (ADC2) Module"** for additional information.

The CDAFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the DAC and comparator module. Reference **Section 30.0 "5-Bit Digital-to-Analog Converter (DAC) Module"** and **Section 32.0 "Comparator Module"** for additional information.

28.2 FVR Stabilization Period

When the Fixed Voltage Reference module is enabled, it requires time for the reference and amplifier circuits to stabilize. Once the circuits stabilize and are ready for use, the FVRRDY bit of the FVRCON register will be set.

FIGURE 28-1: VOLTAGE REFERENCE BLOCK DIAGRAM

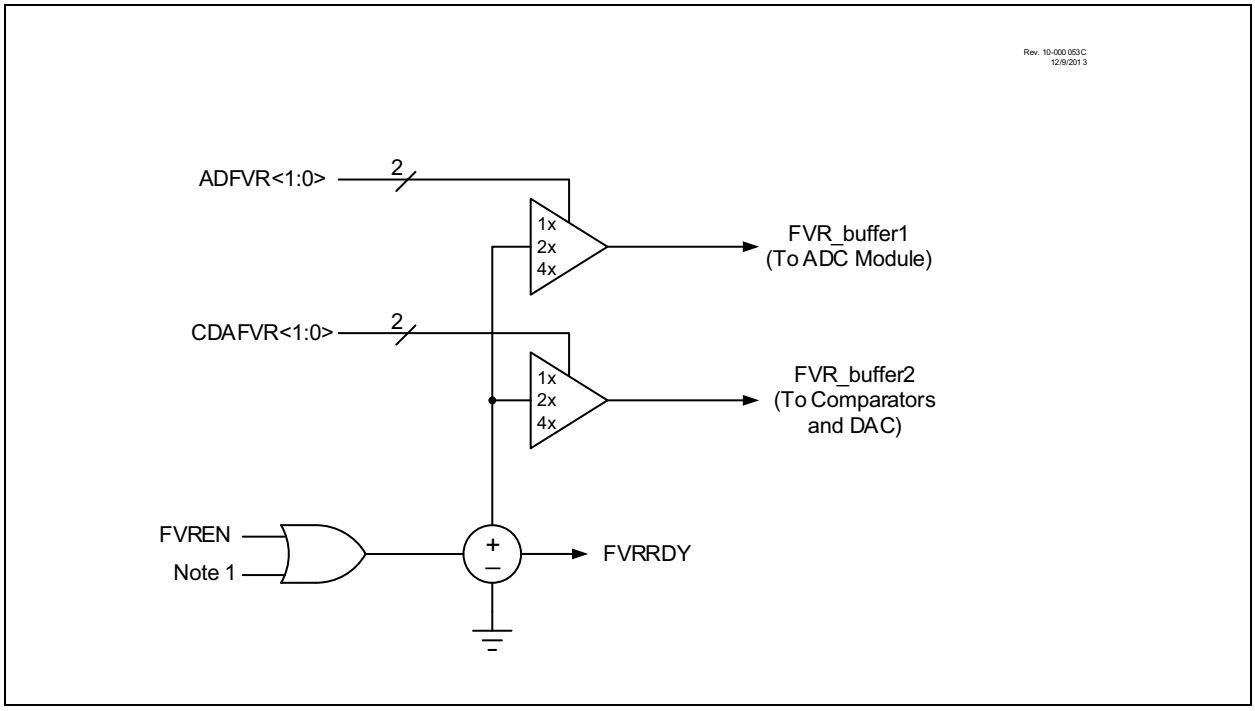


TABLE 35-1: OPCODE FIELD DESCRIPTIONS

Field	Description
a	RAM access bit a = 0: RAM location in Access RAM (BSR register is ignored) a = 1: RAM bank is specified by BSR register
bbb	Bit address within an 8-bit file register (0 to 7).
BSR	Bank Select Register. Used to select the current RAM bank.
C, DC, Z, OV, N	ALU Status bits: **C**arry, **D**igit **C**arry, **Z**ero, **Ov**erflow, **N**egative.
d	Destination select bit d = 0: store result in WREG d = 1: store result in file register f
dest	Destination: either the WREG register or the specified register file location.
f	8-bit Register file address (00h to FFh) or 2-bit FSR designator (0h to 3h).
f_s	12-bit Register file address (000h to FFFh). This is the source address.
f_d	12-bit Register file address (000h to FFFh). This is the destination address.
GIE	Global Interrupt Enable bit.
k	Literal field, constant data or label (may be either an 8-bit, 12-bit or a 20-bit value).
label	Label name.
mm * *+ *- +*	The mode of the TBLPTR register for the table read and table write instructions. Only used with table read and table write instructions: No change to register (such as TBLPTR with table reads and writes) Post-Increment register (such as TBLPTR with table reads and writes) Post-Decrement register (such as TBLPTR with table reads and writes) Pre-Increment register (such as TBLPTR with table reads and writes)
n	The relative address (2's complement number) for relative branch instructions or the direct address for CALL/BRANCH and RETURN instructions.
PC	Program Counter.
PCL	Program Counter Low Byte.
PCH	Program Counter High Byte.
PCLATH	Program Counter High Byte Latch.
PCLATU	Program Counter Upper Byte Latch.
$\overline{PD}$	Power-down bit.
PRODH	Product of Multiply High Byte.
PRODL	Product of Multiply Low Byte.
s	Fast Call/Return mode select bit s = 0: do not update into/from shadow registers s = 1: certain registers loaded into/from shadow registers (Fast mode)
TBLPTR	21-bit Table Pointer (points to a Program Memory location).
TABLAT	8-bit Table Latch.
$\overline{TO}$	Time-out bit.
TOS	Top-of-Stack.
u	Unused or unchanged.
WDT	Watchdog Timer.
WREG	Working register (accumulator).
x	Don't care ('0' or '1'). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
z_s	7-bit offset value for indirect addressing of register files (source).
z_d	7-bit offset value for indirect addressing of register files (destination).
{ }	Optional argument.
[text]	Indicates an indexed address.
(text)	The contents of text.
[expr]<n>	Specifies bit n of the register indicated by the pointer expr.
→	Assigned to.
< >	Register bit field.
∈	In the set of.
italics	User defined term (font is Courier).

TABLE 37-11: RESET, WDT, OSCILLATOR START-UP TIMER, POWER-UP TIMER, BROWN-OUT RESET AND LOW-POWER BROWN-OUT RESET SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
RST01*	TMCLR	$\overline{MCLR}$ Pulse Width Low to ensure Reset	2	—	—	µs	
RST02*	TIOZ	I/O high-impedance from Reset detection	—	—	2	µs	
RST03	TWDT	Watchdog Timer Time-out Period	—	16	—	ms	1:512 Prescaler
RST04*	TPWRT	Power-up Timer Period	—	65	—	ms	
RST05	TOST	Oscillator Start-up Timer Period(1,2)	—	1024	—	TOSC	
RST06	VBOR	Brown-out Reset Voltage(4)	2.7 2.55 2.3 2.3 1.8	2.85 2.7 2.45 2.45 1.9	3.0 2.85 2.6 2.6 2.1	V V V V V	BORV = 00 BORV = 01 BORV = 10 BORV = 11 (PIC18Fxxx) BORV = 11 (PIC18LFxxx)
RST07	VBORHYS	Brown-out Reset Hysteresis	—	40	—	mV	
RST08	TBORDC	Brown-out Reset Response Time	—	3	—	µs	
RST09	VLPBOR	Low-Power Brown-out Reset Voltage	1.8	1.9	2.5	V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: By design, the Oscillator Start-up Timer (OST) counts the first 1024 cycles, independent of frequency.

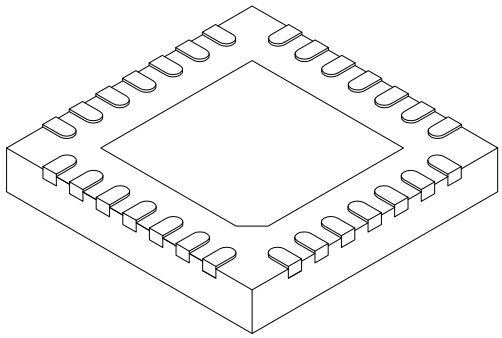
2: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

TABLE 37-12: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Symbol	Characteristic	Min.	Typ†	Max.	Units	Conditions
HLVD01	V_{DET}	Voltage Detection	—	1.90	—	V	HLVDSEL<3:0>=0000
			—	2.10	—	V	HLVDSEL<3:0>=0001
			—	2.25	—	V	HLVDSEL<3:0>=0010
			—	2.50	—	V	HLVDSEL<3:0>=0011
			—	2.60	—	V	HLVDSEL<3:0>=0100
			—	2.75	—	V	HLVDSEL<3:0>=0101
			—	2.90	—	V	HLVDSEL<3:0>=0110
			—	3.15	—	V	HLVDSEL<3:0>=0111
			—	3.35	—	V	HLVDSEL<3:0>=1000
			—	3.60	—	V	HLVDSEL<3:0>=1001
			—	3.75	—	V	HLVDSEL<3:0>=1010
			—	4.00	—	V	HLVDSEL<3:0>=1011
			—	4.20	—	V	HLVDSEL<3:0>=1100
			—	4.35	—	V	HLVDSEL<3:0>=1101
			—	4.65	—	V	HLVDSEL<3:0>=1110

28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN]
With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.50	0.55	0.70
Terminal-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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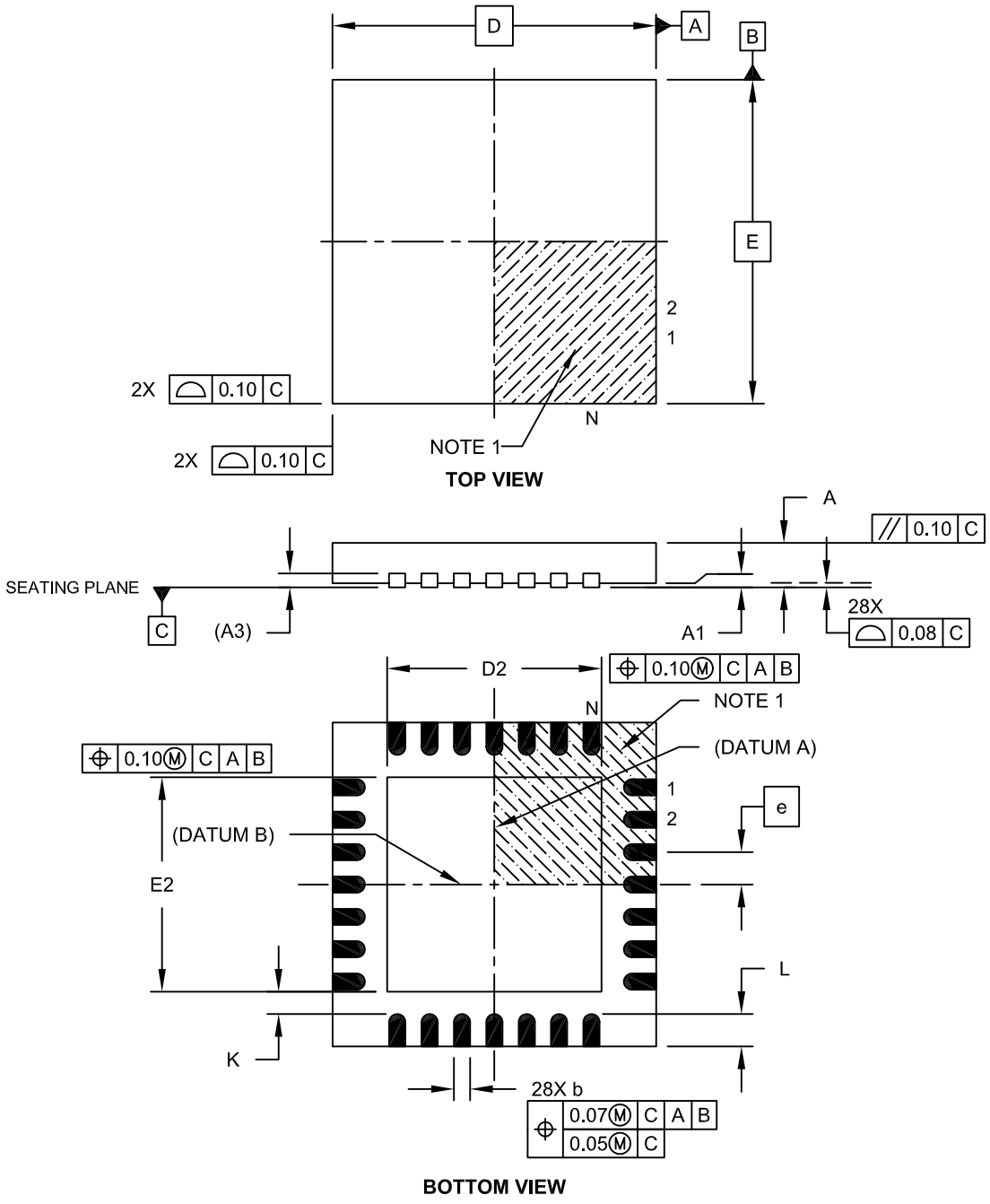
28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-152A Sheet 1 of 2