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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

•XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 35x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf25k40t-i-ml

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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U-1	U-1	R/W-1	U-1	R/W-1	U-1	U-1	R/W-1
_	—	FCMEN	_	CSWEN	_	—	CLKOUTEN
bit 7							bit 0
Legend:							
R = Readable I	oit	W = Writable	bit	U = Unimple	mented bit, read	d as '1'	
-n = Value for b	lank device	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 7-6	Unimplemente	ed: Read as '1	3				
bit 5	FCMEN: Fail-S	Safe Clock Mor	nitor Enable b	it			
	1 = FSCM time	er enabled					
bit 4			,				
Dit 4							
bit 3	CSWEN: Clock Switch Enable bit						
	\perp = writing to NOSC and NDIV is allowed 0 = The NOSC and NDIV bits cannot be changed by user software						
bit 2-1	Unimplement	ed: Read as '1	,	- <u></u>			
bit 0	CI KOUTEN: Clock Out Enable bit						
	If FEXTOSC =	HS, XT, LP, th	en this bit is id	<u>anored</u>			
	Otherwise:			-			
	1 = CLKOUT f	function is disa	bled; I/O or o	scillator function	on on OSC2		
	0 = CLKOUT f	function is enal	bled; FOSC/4	clock appears	s at OSC2		

REGISTER 3-2: Configuration Word 1H (30 0001h): Oscillators

4.3.1.5 Secondary Oscillator

The secondary oscillator is a separate oscillator block that can be used as an alternate system clock source. The secondary oscillator is optimized for 32.768 kHz, and can be used with an external crystal oscillator connected to the SOSCI and SOSCO device pins, or an external clock source connected to the SOSCIN pin. The secondary oscillator can be selected during run-time using clock switching. Refer to **Section 4.4 "Clock Switching"** for more information.

FIGURE 4-5: QUARTZ CRYSTAL OPERATION (SECONDARY OSCILLATOR)



- Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
 - **2:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.
 - **3:** For oscillator design assistance, reference the following Microchip Application Notes:
 - AN826, "Crystal Oscillator Basics and Crystal Selection for PIC[®] and PIC[®] Devices" (DS00826)
 - AN849, "Basic PIC[®] Oscillator Design" (DS00849)
 - AN943, "Practical PIC[®] Oscillator Analysis and Design" (DS00943)
 - AN949, "Making Your Oscillator Work" (DS00949)
 - TB097, "Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS" (DS91097)
 - AN1288, "Design Practices for Low-Power External Oscillators" (DS01288)

4.3.2 INTERNAL CLOCK SOURCES

The device may be configured to use the internal oscillator block as the system clock by performing one of the following actions:

- Program the RSTOSC<2:0> bits in Configuration Words to select the INTOSC clock source, which will be used as the default system clock upon a device Reset.
- Write the NOSC<2:0> bits in the OSCCON1 register to switch the system clock source to the internal oscillator during run-time. See Section 4.4 "Clock Switching" for more information.

In INTOSC mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT is available for general purpose I/O or CLKOUT.

The function of the OSC2/CLKOUT pin is determined by the CLKOUTEN bit in Configuration Words.

The internal oscillator block has two independent oscillators that can produce two internal system clock sources.

- 1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory-calibrated and operates from 1 to 64 MHz. The frequency of HFINTOSC can be selected through the OSCFRQ Frequency Selection register, and fine-tuning can be done via the OSCTUNE register.
- 2. The **LFINTOSC** (Low-Frequency Internal Oscillator) is factory-calibrated and operates at 31 kHz.

EXAMPLE 11-4: WRITING TO PROGRAM FLASH MEMORY (CONTINUED)

WRITE_BYTE_	TO_HREGS		
	MOVF	POSTINCO, W	; get low byte of buffer data
	MOVWF	TABLAT	; present data to table latch
	TBLWT+*		; write data, perform a short write
			; to internal TBLWT holding register.
	DECFSZ	COUNTER	; loop until holding registers are full
	BRA	WRITE_WORD_TO_HREGS	
PROGRAM_MEM	IORY		
	BCF	NVMCON1, NVMREG0	; point to Program Flash Memory
	BSF	NVMCON1, NVMREG1	; point to Program Flash Memory
	BSF	NVMCON1, WREN	; enable write to memory
	BCF	NVMCON1, FREE	; enable write to memory
	BCF	INTCON, GIE	; disable interrupts
	MOVLW	55h	
Required	MOVWF	NVMCON2	; write 55h
Sequence	MOVLW	0AAh	
	MOVWF	NVMCON2	; write OAAh
	BSF	NVMCON1, WR	; start program (CPU stall)
	DCFSZ	COUNTER2	; repeat for remaining write blocks
	BRA	WRITE_BYTE_TO_HREGS	
	BSF	INTCON, GIE	; re-enable interrupts
	BCF	NVMCON1, WREN	; disable write to memory

11.3 Data EEPROM Memory

The data EEPROM is a nonvolatile memory array, separate from the data RAM and program memory, which is used for long-term storage of program data. It is not directly mapped in either the register file or program memory space but is indirectly addressed through the Special Function Registers (SFRs). The EEPROM is readable and writable during normal operation over the entire VDD range.

Four SFRs are used to read and write to the data EEPROM as well as the program memory. They are:

- NVMCON1
- NVMCON2
- NVMDAT
- NVMADRL
- NVMADRH(1)

Note 1: NVMADRH register is not implemented on PIC18(L)F24/25K40.

The data EEPROM allows byte read and write. When interfacing to the data memory block, NVMDAT holds the 8-bit data for read/write and the NVMADRH:NVMADRL register pair hold the address of the EEPROM location being accessed.

The EEPROM data memory is rated for high erase/write cycle endurance. A byte write automatically erases the location and writes the new data (erase-before-write). The write time is controlled by an internal programming timer; it will vary with voltage and temperature as well as from chip-to-chip. Please refer to the Data EEPROM Memory parameters in **Section 37.0 "Electrical Specifications"** for limits.

11.3.1 NVMADRL AND NVMADRH REGISTERS

The NVMADRH:NVMADRL registers are used to address the data EEPROM for read and write operations.

11.3.2 NVMCON1 AND NVMCON2 REGISTERS

Access to the data EEPROM is controlled by two registers: NVMCON1 and NVMCON2. These are the same registers which control access to the program memory and are used in a similar manner for the data EEPROM.

The NVMCON1 register (Register 11-1) is the control register for data and program memory access. Control bits NVMREG<1:0> determine if the access will be to program, Data EEPROM Memory or the User IDs, Configuration bits, Revision ID and Device ID.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear.

The WRERR bit is set by hardware when the WR bit is set and cleared when the internal programming timer expires and the write operation is complete.

The WR control bit initiates write operations. The bit can be set but not cleared by software. It is cleared only by hardware at the completion of the write operation.

The NVMIF interrupt flag bit of the PIR7 register is set when the write is complete. It must be cleared by software.

Control bits, RD and WR, start read and erase/write operations, respectively. These bits are set by firmware and cleared by hardware at the completion of the operation.

The RD bit cannot be set when accessing program memory (NVMREG<1:0> = 0x10). Program memory is read using table read instructions. See **Section 11.1.1 "Table Reads and Table Writes"** regarding table reads.

D ALL O IS			Б Í		11.0	DAAL O/O	
R/W-0/0		R-0 BUSV		R/W-0/0	U-0	R/W-0/0	R/W-0/0
SCANEN	JUSCANGU	6031	IINVALID			MODE	51.UZ
DIC 7							DIt U
Legend:							
R = Readal	ble bit	W = Writable	bit	U = Unimplen	nented bit, read	as '0'	
u = Bit is ur	nchanged	x = Bit is unkr	nown	-n/n = Value a	at POR and BOF	R/Value at all oth	ner Resets
'1' = Bit is s	set	'0' = Bit is clea	ared	HC = Bit is cle	eared by hardwa	are	
bit 7 bit 6	SCANEN: Sc 1 = Scanner is 0 = Scanner is SCANGO: Sc 1 = When the	anner Enable b s enabled s disabled, inte anner GO bit ⁽²	_{pit} (1) rnal states are , 3)	reset		a to MDy and d	to pocoed to
bit 5	1 = When the the client 0 = Scanner of BUSY: Scann 1 = Scanner of	peripheral. perations will r er Busy Indica cycle is in proce	not occur tor bit ⁽⁴⁾ ess	atod)			ata passed to
bit 4	0 = Scanner C INVALID: Sca 1 = SCANLAE 0 = SCANLAE	 0 = Scanner cycle is complete (or never started) INVALID: Scanner Abort Signal bit 1 = SCANLADRL/H/U has incremented to an invalid address⁽⁶⁾ or the scanner was not setup correctly⁽⁷⁾ 0 = SCANLADRL/H/U points to a valid address 					
bit 3	 INTM: NVM Scanner Interrupt Management Mode Select bit If MODE = 10: This bit is ignored If MODE = 01 (CPU is stalled until all data is transferred): 1 = SCANGO is overridden (to zero) during interrupt operation; scanner resumes after returning from interrupt 0 = SCANGO is not affected by interrupts, the interrupt response will be affected If MODE = 00 or 11: 1 = SCANGO is overridden (to zero) during interrupt operation; scan operations resume after returning from interrupt 0 = Interrupts do not prevent NV/M access 						eturning from fter returning
bit 2	Unimplemen	ted: Read as 'd)'				
bit 1-0	MODE<1:0>: 11 = Triggere 10 = Peek mo 01 = Burst mo 00 = Concurre	Memory Acces d mode ode ode ent mode	ss Mode bits ⁽⁵⁾				
Note 1: 2: 3: 4: 5: 6: 7:	Setting SCANEN = This bit is cleared v If INTM = 1, this bi BUSY = 1 when th See Table 13-2 for An invalid address invalid address can mapped in the men CRCEN and CRCC Scan Configuratio	0 (SCANCON when LADR > I t is overridden e NVM is being more detailed i can occur whe n also occur if t mory map of th GO bits must be n".	I0 register) doe HADR (and a c (to zero, but no accessed, or information. n the entire ran he value in the e device. e set before set	es not affect any lata cycle is not ot cleared) durir when the CRC nge of PFM is so Scan Low add tting SCANGO b	y other register of occurring). Ing an interrupt ro sends a ready s canned and the ress registers p bit. Refer to Sec	content. esponse. signal. value of LADR r oints to a locatic tion 13.9 "Prog i	olls over. An on that is not ram Memory

REGISTER 13-11: SCANCONO: SCANNER ACCESS CONTROL REGISTER 0

R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0	R/W-1/1
SCANIP	CRCIP	NVMIP	_	_		_	CWG1IP
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 7	SCANIP: SCA 1 = High prior 0 = Low prior	AN Interrupt Pri rity ity	ority bit				
bit 6	CRCIP: CRC 1 = High prior 0 = Low prior	Interrupt Priorit rity ity	ty bit				
bit 5	bit 5 NVMIP: NVM Interrupt Priority bit 1 = High priority 0 = Low priority						
bit 4-1	Unimplement	ted: Read as 'd)'				
bit 0	CWG1IP: CW 1 = High prior 0 = Low prior	/G Interrupt Prio rity ity	ority bit				

REGISTER 14-25: IPR7: PERIPHERAL INTERRUPT PRIORITY REGISTER 7

16.0 INTERRUPT-ON-CHANGE

PORTA, PORTB, PORTC and pin RE3 of PORTE can be configured to operate as Interrupt-on-Change (IOC) pins on PIC18(L)F2x/4xK40 family devices. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual port pin, or combination of port pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- · Rising and falling edge detection
- Individual pin interrupt flags

Figure 16-1 is a block diagram of the IOC module.

16.1 Enabling the Module

To allow individual port pins to generate an interrupt, the IOCIE bit of the PIE0 register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

16.2 Individual Pin Configuration

For each port pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting both associated bits of the IOCxP and IOCxN registers, respectively.

16.3 Interrupt Flags

The IOCAFx, IOCBFx, IOCCFx and IOCEF3 bits located in the IOCAF, IOCBF, IOCCF and IOCEF registers respectively, are status flags that correspond to the interrupt-on-change pins of the associated port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the PIRO register reflects the status of all IOCAFx, IOCBFx, IOCCFx and IOCEF3 bits.

16.4 Clearing Interrupt Flags

The individual status flags, (IOCAFx, IOCBFx, IOCCFx and IOCEF3 bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 16-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

MOVLW	0xff	
XORWF	IOCAF,	W
ANDWF	IOCAF,	F

16.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the IOCxF register will be updated prior to the first instruction executed out of Sleep.

20.5.3 EDGE-TRIGGERED HARDWARE LIMIT MODE

In Hardware Limit mode the timer can be reset by the TMRx_ers external signal before the timer reaches the period count. Three types of Resets are possible:

- Reset on rising or falling edge (MODE<4:0>= 00011)
- Reset on rising edge (MODE<4:0> = 00100)
- Reset on falling edge (MODE<4:0> = 00101)

FIGURE 20-6: EDGE-TRIGGERED HARDWARE LIMIT MODE TIMING DIAGRAM (MODE = 00100)



When the timer is used in conjunction with the CCP in PWM mode then an early Reset shortens the period and restarts the PWM pulse after a two clock delay. Refer to Figure 20-6.

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PSYNC	CPOL	CSYNC			MODE<4:0>		
bit 7	÷						bit 0
Legend:							
R = Reada	ble bit	W = Writable	bit	U = Unimpler	nented bit, read	d as '0'	
u = Bit is u	nchanged	x = Bit is unkr	nown	-n/n = Value a	at POR and BC	R/Value at all	other Resets
'1' = Bit is	set	'0' = Bit is cle	ared				
bit 7	PSYNC: Tim	erx Prescaler S	Synchronization	n Enable bit ^{(1, 2}	:)		
	1 = TMRx P	rescaler Output	is synchroniz	ed to Fosc/4	4		
1.11.0		rescaler Output		DNIZED TO FOSC/4	4		
bit 6	1 - Falling e	rx Clock Polarit	y Selection bit	or/prescaler			
	0 = Rising e	dge of input clo	ck clocks time	r/prescaler			
bit 5	CSYNC: Tim	erx Clock Sync	hronization Er	nable bit ^(4, 5)			
	1 = ON regis	ster bit is synch	ronized to TM	R2_clk input			
	0 = ON regis	ster bit is not sy	nchronized to	TMR2_clk inpu	it		
bit 4-0	MODE<4:0>	: Timerx Contro	Mode Select	ion bits ^(6, 7)			
	See Table 20	-1 for all operation	ng modes.				
Note 1:	Setting this bit er	nsures that read	ding TMRx will	return a valid o	data value.		
2:	When this bit is '	1', Timer2 canr	ot operate in S	Sleep mode.			
3:	3: CKPOL should not be changed while ON = 1.						
4:	Setting this bit er	nsures glitch-fre	e operation w	hen the ON is e	enabled or disa	bled.	
5:	When this bit is s	et then the time	r operation will	be delayed by	two TMRx input	t clocks after th	e ON bit is set.
6:	Unless otherwise affecting the value	e indicated, all ie of TMRx).	modes start u	upon ON = 1 a	nd stop upon (ON = 0 (stops	occur without
7.	When TMRx = P	Ry the next clo	ock clears TMF	Rx renardless (of the operation	ımode	

REGISTER 20-2: TxHLT: TIMERx HARDWARE LIMIT CONTROL REGISTER

When IMRx PRx, the next clock clears TMRx, regardless of the operating mode. 7:

22.2 Register Definitions: PWM Control

Long bit name prefixes for the PWM peripherals are shown in Table 22-3. Refer to **Section 1.4.2.2 "Long Bit Names"** for more information.

TABLE 22-3:

Peripheral	Bit Name Prefix
PWM3	PWM3
PWM4	PWM4

REGISTER 22-1: PWMxCON: PWM CONTROL REGISTER

R/W-0/0	U-0	R-0/0	R/W-0/0	U-0	U-0	U-0	U-0
EN	—	OUT	POL	—	—	—	—
bit 7							bit 0

W = Writable bit	U = Unimplemented bit, read as '0'
x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'0' = Bit is cleared	
	W = Writable bit x = Bit is unknown '0' = Bit is cleared

bit 7	EN: PWM Module Enable bit
	1 = PWM module is enabled0 = PWM module is disabled
bit 6	Unimplemented: Read as '0'
bit 5	OUT: PWM Module Output Level When Bit is Read
bit 4	POL: PWM Output Polarity Select bit
	1 = PWM output is inverted0 = PWM output is normal
bit 3-0	Unimplemented: Read as '0'



24.2.2 PUSH-PULL MODE

In Push-Pull mode, two output signals are generated, alternating copies of the input as illustrated in Figure 24-4. This alternation creates the push-pull effect required for driving some transformer-based power supply designs. Steering modes are not used in Push-Pull mode. A basic block diagram for the Push-Pull mode is shown in Figure 24-3.

The push-pull sequencer is reset whenever EN = 0 or if an auto-shutdown event occurs. The sequencer is clocked by the first input pulse, and the first output appears on CWG1A.

The unused outputs CWG1C and CWG1D drive copies of CWG1A and CWG1B, respectively, but with polarity controlled by the POLC and POLD bits of the CWG1CON1 register, respectively.

24.7 Rising Edge and Reverse Dead Band

In Half-Bridge mode, the rising edge dead band delays the turn-on of the CWG1A output after the rising edge of the CWG data input. In Full-Bridge mode, the reverse dead-band delay is only inserted when changing directions from Forward mode to Reverse mode, and only the modulated output CWG1B is affected.

The CWG1DBR register determines the duration of the dead-band interval on the rising edge of the input source signal. This duration is from 0 to 64 periods of the CWG clock.

Dead band is always initiated on the edge of the input source signal. A count of zero indicates that no dead band is present.

If the input source signal reverses polarity before the dead-band count is completed, then no signal will be seen on the respective output.

The CWG1DBR register value is double-buffered. When EN = 0 (Register 24-1), the buffer is loaded when CWG1DBR is written. If EN = 1, then the buffer will be loaded at the rising edge following the first falling edge of the data input, after the LD bit (Register 24-1) is set. Refer to Figure 24-12 for an example.

24.8 Falling Edge and Forward Dead Band

In Half-Bridge mode, the falling edge dead band delays the turn-on of the CWG1B output at the falling edge of the CWG data input. In Full-Bridge mode, the forward dead-band delay is only inserted when changing directions from Reverse mode to Forward mode, and only the modulated output CWG1D is affected.

The CWG1DBF register determines the duration of the dead-band interval on the falling edge of the input source signal. This duration is from zero to 64 periods of CWG clock.

Dead-band delay is always initiated on the edge of the input source signal. A count of zero indicates that no dead band is present.

If the input source signal reverses polarity before the dead-band count is completed, then no signal will be seen on the respective output.

The CWG1DBF register value is double-buffered. When EN = 0 (Register 24-1), the buffer is loaded when CWG1DBF is written. If EN = 1, then the buffer will be loaded at the rising edge following the first falling edge of the data input after the LD (Register 24-1) is set. Refer to Figure 24-13 for an example.

26.5 SPI Mode Operation

Transmissions involve two shift registers, eight bits in size, one in the master and one in the slave. With either the master or the slave device, data is always shifted out one bit at a time, with the Most Significant bit (MSb) shifted out first. At the same time, a new Least Significant bit (LSb) is shifted into the same register.

Figure 26-3 shows a typical connection between two processors configured as master and slave devices.

Data is shifted out of both shift registers on the programmed clock edge and latched on the opposite edge of the clock.

The master device transmits information out on its SDO output pin which is connected to, and received by, the slave's SDI input pin. The slave device transmits information out on its SDO output pin, which is connected to, and received by, the master's SDI input pin.

To begin communication, the master device first sends out the clock signal. Both the master and the slave devices should be configured for the same clock polarity.

The master device starts a transmission by sending out the MSb from its shift register. The slave device reads this bit from that same line and saves it into the LSb position of its shift register.

During each SPI clock cycle, a full-duplex data transmission occurs. This means that while the master device is sending out the MSb from its shift register (on its SDO pin) and the slave device is reading this bit and saving it as the LSb of its shift register, that the slave device is also sending out the MSb from its shift register (on its SDO pin) and the master device is reading this bit and saving it as the LSb of its shift register.

After eight bits have been shifted out, the master and slave have exchanged register values.

If there is more data to exchange, the shift registers are loaded with new data and the process repeats itself.

Whether the data is meaningful or not (dummy data), depends on the application software. This leads to three scenarios for data transmission:

- Master sends useful data and slave sends dummy data.
- Master sends useful data and slave sends useful data.
- Master sends dummy data and slave sends useful data.

Transmissions may involve any number of clock cycles. When there is no more data to be transmitted, the master stops sending the clock signal and it deselects the slave.

Every slave device connected to the bus that has not been selected through its slave select line must disregard the clock and transmission signals and must not transmit out any data of its own. When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPxCON1<5:0> and SSPxSTAT<7:6>). These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- · Slave Select mode (Slave mode only)

To enable the serial port, SSP Enable bit, SSPEN of the SSPxCON1 register, must be set. To reset or reconfigure SPI mode, clear the SSPEN bit, re-initialize the SSPxCONx registers and then set the SSPEN bit. This configures the SDI, SDO, SCK and SS pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed as follows:

- · SDI must have corresponding TRIS bit set
- SDO must have corresponding TRIS bit cleared
- SCK (Master mode) must have corresponding
 TRIS bit cleared
- SCK (Slave mode) must have corresponding TRIS bit set
- SS must have corresponding TRIS bit set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

The MSSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPxBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPxBUF holds the data that was written to the SSPSR until the received data is ready. Once the eight bits of data have been received, that byte is moved to the SSPxBUF register. Then, the Buffer Full Detect bit, BF of the SSPxSTAT register, and the interrupt flag bit, SSPxIF, are set. This double-buffering of the received data (SSPxBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPxBUF register during transmission/reception of data will be ignored and the write collision detect bit, WCOL of the SSPxCON1 register, will be set. User software must clear the WCOL bit to allow the following write(s) to the SSPxBUF register to complete successfully.

R/HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	nented bit, read	d as '0'		
-n = Value at	POR	'1' = Bit is set	y hardware				
x = Bit is unki	nown	'0' = Bit is clea	ared				
bit 7	ACKTIM: Ack	knowledge Time	e Status bit				
	Unused in Ma	aster mode.					
bit 6	PCIE: Stop C	ondition Interru	pt Enable bit ⁽¹)			
	1 = Enable in	nterrupt on dete	ction of Stop of	condition			
	0 = Stop dete	ection interrupts	s are disabled	、			
bit 5	SCIE: Start C	ondition Interru	pt Enable bit ⁽¹)			
	1 = Enable interrupt on detection of Start or Restart conditions						
bit 4	BOEN: Buffer Overwrite Enable bit						
	1 = SSPxBUF is updated every time a new data byte is available, ignoring the SSPOV effect						POV effect on
	updating the buffer						
	0 = SSPxBUF	is only update	d when SSPO	V is clear			
bit 3	SDAHT: SDA Hold Time Selection bit						
	1 = Minimum of 300ns hold time on SDA after the falling edge of SCL						
1.1.0		of Toons hold t	ime on SDA a	tter the failing e	age of SCL		
DIT 2	SECDE: Slave Mode Bus Collision Detect Enable bit						
bit 1	bit 1 AHEN: Address Hold Enable bit						
	Unused in Ma	aster mode.					
bit 0	DHEN: Data I	Hold Enable bit					
	Unused in Ma	aster mode.					
							LOTOD

REGISTER 26-9: SSPxCON3: MSSPx CONTROL REGISTER 3 (I²C MASTER MODE)

Note 1: This bit has no effect when SSPM<3:0> = 1111 or 1110.In these Slave modes the START and STOP condition interrupts are always enabled.

REGISTER 26-10: SSPxBUF: MSSP DATA BUFFER REGISTER (I²C MASTER MODE)

					•		
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			BUF	<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit	t	W = Writable bit		U = Unimpler	mented bit, read	as '0'	

R = Readable bit	vv = vvritable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 BUF<7:0>: MSSP Buffer bits

26.10.10 SLEEP OPERATION

While in Sleep mode, the I²C slave module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

26.10.11 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

26.10.12 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit of the SSPxSTAT register is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCLxIF bit.

The states where arbitration can be lost are:

- · Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

26.10.13 MULTI -MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA, by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin is '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLxIF and reset the I²C port to its Idle state (Figure 26-32).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are deasserted and the SSPxBUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I²C bus is free, the user can resume communication by asserting a Start condition.

If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are deasserted and the respective control bits in the SSPxCON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I^2C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDA and SCL pins. If a Stop condition occurs, the SSPxIF bit will be set.

A write to the SSPxBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I^2C bus can be taken when the P bit is set in the SSPxSTAT register, or the bus is Idle and the S and P bits are cleared.

FIGURE 26-32: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE



27.2.1.5 TSR Status

The TRMT bit of the TXxSTA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TXxREG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user has to poll this bit to determine the TSR status.

Note:	The TSR register is not mapped in data					
	memory, so it is not available to the user.					

27.2.1.6 Transmitting 9-Bit Characters

The EUSART supports 9-bit character transmissions. When the TX9 bit of the TXxSTA register is set, the EUSART will shift nine bits out for each character transmitted. The TX9D bit of the TXxSTA register is the ninth, and Most Significant data bit. When transmitting 9-bit data, the TX9D data bit must be written before writing the eight Least Significant bits into the TXxREG. All nine bits of data will be transferred to the TSR shift register immediately after the TXxREG is written.

A special 9-bit Address mode is available for use with multiple receivers. See **Section 27.2.2.7 "Address Detection"** for more information on the Address mode.

27.2.1.7 Asynchronous Transmission Setup:

- Initialize the SPxBRGH, SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 27.4 "EUSART Baud Rate Generator (BRG)").
- 2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
- 3. If 9-bit transmission is desired, set the TX9 control bit. A set ninth data bit will indicate that the eight Least Significant data bits are an address when the receiver is set for address detection.
- 4. Set SCKP bit if inverted transmit is desired.
- 5. Enable the transmission by setting the TXEN control bit. This will cause the TXxIF interrupt bit to be set.
- If interrupts are desired, set the TXxIE interrupt enable bit of the PIE3 register. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
- 7. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
- 8. Load 8-bit data into the TXxREG register. This will start the transmission.



FIGURE 27-3: ASYNCHRONOUS TRANSMISSION

31.4.1 CVD OPERATION

A CVD operation begins with the ADC's internal and hold capacitor sample (С_{НОГD}) being disconnected from the path which connects it to the external capacitive sensor node. While disconnected, CHOLD is precharged to VDD or Vss, while the path to the sensor node is also discharged to VDD or VSS. Typically, this node is discharged to the level opposite that of CHOLD. When the precharge phase is complete, the VDD/VSS bias paths for the two nodes are shut off and CHOLD and the path to the external sensor node are re-connected, at which time the acquisition phase of the CVD operation begins. During acquisition, a capacitive voltage divider is formed between the precharged CHOLD and sensor nodes, which results in a final voltage level setting on CHOLD which is determined by the capacitances and precharge levels of the two nodes. After acquisition, the ADC converts the voltage level on CHOLD. This process is then repeated with the selected precharge levels for both the CHOLD and the inverted sensor nodes. Figure 31-7 shows the waveform for two inverted CVD measurements, which is known as differential CVD measurement.





Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word				Status	N. /
		Description		MSb			LSb	Affected	Notes
BIT-ORIENTED OPERATIONS									
BCF	f, b, a	Bit Clear f	1	1001	bbba	ffff	ffff	None	1, 2
BSF	f, b, a	Bit Set f	1	1000	bbba	ffff	ffff	None	1, 2
BTFSC	f, b, a	Bit Test f, Skip if Clear	1 (2 or 3)	1011	bbba	ffff	ffff	None	3, 4
BTFSS	f, b, a	Bit Test f, Skip if Set	1 (2 or 3)	1010	bbba	ffff	ffff	None	3, 4
BTG	f, b, a	Bit Toggle f	1	0111	bbba	ffff	ffff	None	1, 2
CONTROL	OPERA	TIONS							
BC	n	Branch if Carry	1 (2)	1110	0010	nnnn	nnnn	None	
BN	n	Branch if Negative	1 (2)	1110	0110	nnnn	nnnn	None	
BNC	n	Branch if Not Carry	1 (2)	1110	0011	nnnn	nnnn	None	
BNN	n	Branch if Not Negative	1 (2)	1110	0111	nnnn	nnnn	None	
BNOV	n	Branch if Not Overflow	1 (2)	1110	0101	nnnn	nnnn	None	
BNZ	n	Branch if Not Zero	1 (2)	1110	0001	nnnn	nnnn	None	
BOV	n	Branch if Overflow	1 (2)	1110	0100	nnnn	nnnn	None	
BRA	n	Branch Unconditionally	2	1101	0nnn	nnnn	nnnn	None	
BZ	n	Branch if Zero	1 (2)	1110	0000	nnnn	nnnn	None	
CALL	k, s	Call subroutine 1st word	2	1110	110s	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk		
CLRWDT	—	Clear Watchdog Timer	1	0000	0000	0000	0100	TO, PD	
DAW	—	Decimal Adjust WREG	1	0000	0000	0000	0111	С	
GOTO	k	Go to address 1st word	2	1110	1111	kkkk	kkkk	None	
		2nd word		1111	kkkk	kkkk	kkkk		
NOP	—	No Operation	1	0000	0000	0000	0000	None	
NOP	—	No Operation	1	1111	XXXX	XXXX	XXXX	None	4
POP	—	Pop top of return stack (TOS)	1	0000	0000	0000	0110	None	
PUSH	—	Push top of return stack (TOS)	1	0000	0000	0000	0101	None	
RCALL	n	Relative Call	2	1101	1nnn	nnnn	nnnn	None	
RESET		Software device Reset	1	0000	0000	1111	1111	All	
RETFIE	S	Return from interrupt enable	2	0000	0000	0001	000s	GIE/GIEH,	
								PEIE/GIEL	
RETLW	k	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None	
RETURN	S	Return from Subroutine	2	0000	0000	0001	001s	None	
SLEEP	_	Go into Standby mode	1	0000	0000	0000	0011	TO, PD	

TABLE 35-2: INSTRUCTION SET (CONTINUED)

Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, 'd' = 1), the prescaler will be cleared if assigned.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

4: Some instructions are two-word instructions. The second word of these instructions will be executed as a NOP unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

TABLE 37-14: ANALOG-TO-DIGITAL CONVERTER (ADC) CONVERSION TIMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)								
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions	
AD20	Tad	ADC Clock Period	1		9	μS	Using Fosc as the ADC clock source ADOCS = 0	
AD21				2		μS	Using FRC as the ADC clock source ADOCS = 1	
AD22	TCNV	Conversion Time ⁽¹⁾		11 + Зтсү		Tad	Set of GO/DONE bit to Clear of GO/ DONE bit	
AD23	TACQ	Acquisition Time	_	2	_	μS		
AD24	THCD	Sample and Hold Capacitor Disconnect Time		_		μS	Fosc-based clock source Frc-based clock source	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Does not apply for the ADCRC oscillator.

FIGURE 37-10: ADC CONVERSION TIMING (ADC CLOCK Fosc-BASED)

