Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Xstormy16
Core Size	16-Bit
Speed	12MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc88fc2h0avute-2h

Function Details

■ Xstromy16 CPU

- 4G-byte address space
- General-purpose registers : 16 bits × 16 registers

■ Flash ROM

- Programming voltage level : 2.7 to 3.6 V.
- Block-erasable in 2K byte units.
- Data written in 2-byte units.
- 524288 × 8 bits

■ RAM

- 24576 × 8 bits

■ Minimum instruction cycle time (tCYC)

- 83.3 ns (12 MHz), V_{DD} = 3.0 to 3.6 V
- 100 ns (10 MHz), V_{DD} = 2.7 to 3.6 V

■ Ports

- Normal withstand voltage I/O ports
  Ports whose I/O direction can be designated in 1 bit units : 86 (P0n P1n, P2n, P3n, P4n, P5n, P6n, P7n, PAn, PB0 to PB6, PC2, PD0 to PD5)
- Oscillation/normal with stand voltage I/O ports : 4 (PC0, PC1, PC3, PC4)
- Reset pins : 1 (RESB)
- TEST pins : 1 (TEST)
- Power pins : 8 (V_{SS}1 to 4, V_{DD}1 to 4)

■ Timers

- Timer 0 : 16-bit timer that supports PWM/toggle outputs
  <1> 5-bit prescaler
  <2> 8-bit PWM × 2, 8-bit timer + 8-bit PWM mode selectable
  <3> Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator.
- Timer 1 : 16-bit timer with capture registers
  <1> 5-bit prescaler
  <2> May be divided into 2 channels of 8-bit timer
  <3> Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 2 : 16-bit timer with capture registers
  <1> 4-bit prescaler
  <2> May be divided into 2 channels of 8-bit timer
  <3> Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 3 : 16-bit timer that shpports PWM/toggle outputs
  <1> 8-bit prescaler
  <2> 8-bit timer × 2 ch or 8-bit timer + 8-bit PWM mode selectable
  <3> Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 4 : 16-bit timer that supports toggle outputs
  <1> Clock source selectable from system clock and prescaler 0
- Timer 5 : 16-bit timer that supports toggle output
  <1> Clock source selectable from system clock and prescaler 0
- Timer 6 : 16-bit timer that supports toggle outputs
  <1> Clock source selectable from system clock and prescaler 1
- Timer 7 : 16-bit timer that supports toggle output
  <1> Clock source selectable from system clock and prescaler 1

* Prescaler 0 and 1 are consisted of 4bits and can choose their clock source from OSC0 or OSC1.

■ Oscillator circuits

- RC oscillator circuit (internal) : For system clock
- CF oscillator circuit (built-in Rf circuit) : For system clock(OSC1)
- Crystal oscillator circuit (built-in Rf circuit) : For low-speed system clock (OSC0)
- SLRC oscillator circuit (internal) : For system clock (In the case of exception processing)
- VCO oscillator circuit : For timer3,4,5,6,7 clock

■ System clock divider function

- Can run on low current.
- 1/1 to 1/128 of the system clock frequency can be set.

■ Standby function

- HALT mode : Halts instruction execution while allowing the peripheral circuits to continue operation.
  <1> Oscillation is not stopped automatically.
  <2> Released by a system reset or occurrence of an interrupt.
- HOLD mode : Suspends instruction execution and the operation of the peripheral circuits.
  <1> OSC1, RC, and OSC0 oscillations automatically stop.
  <2> There are six ways of releasing the HOLD mode:
  (1) Setting the reset pin to the low level
  (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 pins to the specified level
  (3) Having an interrupt source established at port 0
  (4) Having an interrupt source established at port 5
  (5) Having an interrupt established at SIO0, SIO1 or SIO4
  (6) Having an interrupt established at UART2 or UART3
- HOLDX mode : Suspends instruction execution and the operation of the peripheral circuits except those which run on OSC0.
  <1> OSC1 and RC oscillations automatically stop.
  <2> OSC0 maintains the state that is established when the HOLDX mode is entered.
  <3> There are nine ways of releasing the HOLDX mode.
  (1) Setting the reset pin to the low level
  (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6,and INT7 pins to the specified level
  (3) Having an interrupt source established at port 0
  (4) Having an interrupt source established at port 5
  (5) Having an interrupt source established at the base timer circuit
  (6) Having an interrupt established at SIO0, SIO1 or SIO4
  (7) Having an interrupt established at UART2 or UATR3
  (8) Having an interrupt established at Infared remote control receiver.
  (9) Having an interrupt source established at the real time clock circuit

■ On-chip debugger function

- Supports software debugging with the IC mounted on the target board.
- Supports source line debugging and tracing functions, and breakpoint setting and real time display.
- Single-wire communication

■ Package form

- TQFP100 (14 × 14) : Pb-Free and Halogen Free type

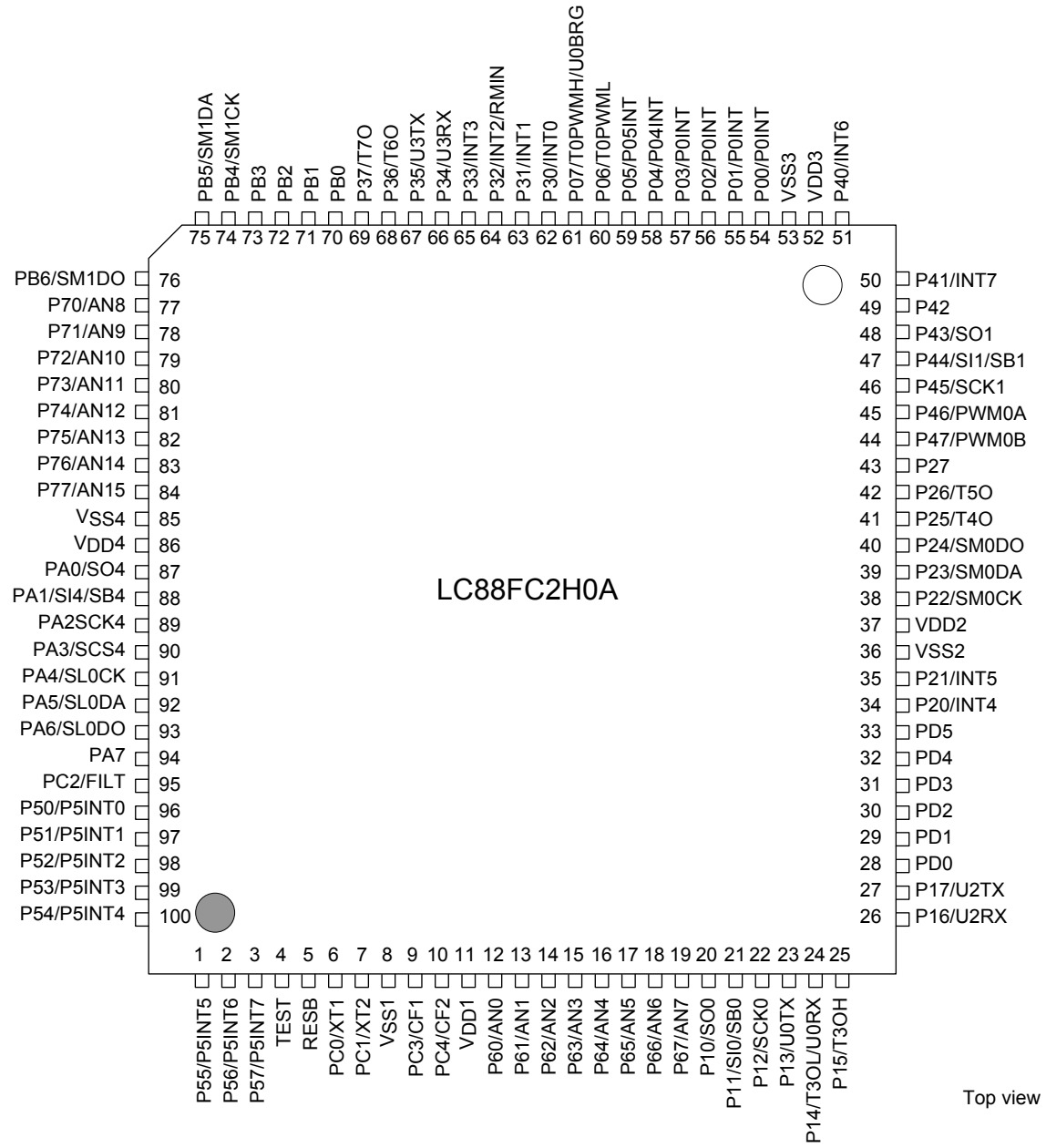
■ Development tools

- On-chip debugger: EOCUIF1 or EOCUIF2 + LC88FC2H0A

■ Programming board

Package	Programming Board
TQFP100 (14 × 14)	W88F52TQ

Pinout



Top view

TQFP100 (14×14) (Pb-Free and Halogen free type)

Continued from preceding page.

Pin Name	I/O	Description
Port 3 P30 to P37	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions P30 : INT0 input/HOLD release/timer 2L capture input P31 : INT1 input/HOLD release/timer 2H capture input P32 : INT2 input/HOLD release/timer 2 event input/timer 2L capture input/ Infrared Remote Controller Receiver input P33 : INT3 input/HOLD release/timer 2 event input/timer 2H capture input P34 : UART3 receive P35 : UART3 transmit P36 : Timer 6 output P37 : Timer 7 output Interrupt acknowledge type INT0 to INT3 : H level, L level, H edge, L edge, both edges
Port 4 P40 to P47	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions P40 : INT6 input/HOLD release input P41 : INT7 input/HOLD release input P43 : SIO1 data output P44 : SIO1 data input/bus input/output P45 : SIO1 clock input/output P46 : PWM0A output P47 : PWM0Boutput Interrupt acknowledge type INT6, INT7 : H level, L level, H edge, L edge, both edges
Port 5 P50 to P57	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • HOLD release input • Port 0 interrupt input
Port 6 P60 to P67	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions AN0 (P60) to AN7 (P67) : AD converter input port
Port 7 P70 to P77	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Pin functions AN8 (P70) to AN15 (P77) : AD converter input port

Continued from preceding page.

Pin Name	I/O	Description
Port A PA0 to PA7	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units • Multiplexed pin functions PA0 : SIO4 data output PA1 : SIO4 data input/pulse input/output PA2 : SIO4 clock input/output PA3 : SIO4 chip select input PA4 : SLIIC0 clock input PA5 : SLIIC0 bus input/output/data input PA6 : SLIIC0 data output (used in 3-wire SIO mode)
Port B PB0 to PB6	I/o	• 7-bit I/O port • I/O specifiable in 1-bit units •Pull-up resistors can be turned on and off in 1 bit units • Multiplexed pin functions PB4 : SMIIC1 clock input/output PB5 : SMIIC1 bus input/output/data input PB6 : SMIIC1 data output (used in 3-wire SIO mode)
Port C PC0 to PC4	I/O	• 5-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units(PC2) • Pin functions PC0 : 32.768 kHz crystal oscillator input PC1 : 32.768 kHz crystal oscillator output PC2 : FILT of VCO PC3 : Ceramic oscillator input PC4 : Ceramic oscillator output/VCO output
Port D PD0 to PD5	I/O	• 6-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1 bit units
TEST	I/O	• TEST pin • Used to communicate with on-chip debugger. • Connects an external 100 kΩ pull-down resistor.
RESB	I/O	Reset pin

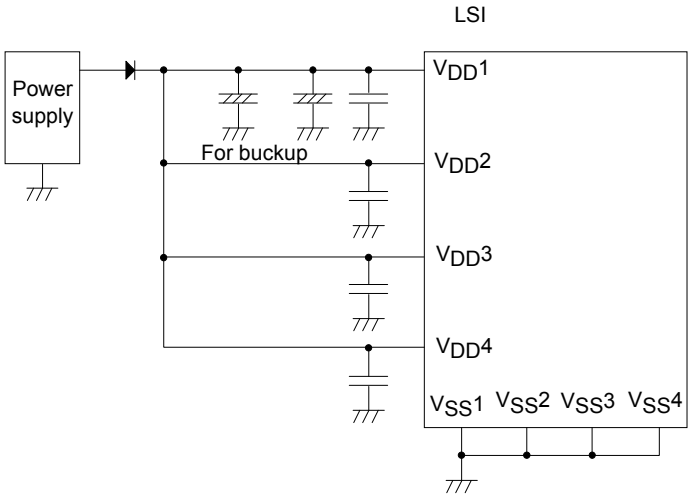
Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

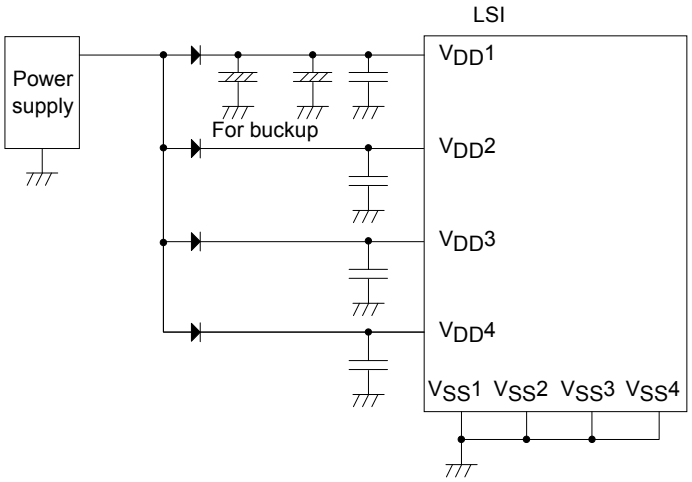
Port Name	Option Selected in Units of	Output Type	Pull-up Resistor
P00 to P07	1 bit	CMOS	Programmable
P10 to P17 P20 to P27 P30 to P37 P40 to P47 P50 to P57 P60 to P67 P70 to P77 PA0 to PA7 PB0 to PB6		Able to program special functions'output type from CMOS output or Nch-opendrain	
P60 to P67 P70 to p77 PD0 to PD5 PC2		CMOS	
PC0	–	N-channel open drain (32.768 kHz crystal oscillator input)	None
PC1	–	Nch-open drain (32.768k kHz crystal oscillator output)	None
PC3	–	CMOS (ceramic oscillator input)	None
PC4	–	CMOS (ceramic oscillator output)	None

* Make the following connection to minimize the noise input to the VDD1 pin and prolong the backup time.
  Be sure to electrically short the VSS1, VSS2, VSS3 and VSS4 pins.

Example 1 : When data is being backed up in the HOLD mode, the H level signals to the output ports are fed by the backup capacitors.



Example 2 : When data is being backed up in the HOLD mode, the H level output at any ports is not sustained and is unpredictable.



2-1. SIO1 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-3-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK (4)	SCK1 (P45)	• See Fig. 6.	2.7 to 3.6	4			tCYC
		Low level pulse width	tSCKL (4)				2			
		High level pulse width	tSCKH (4)				2			
			tSCKHA (4)		• Automatic communication mode • See Fig. 6.		6			
			tSCKHBSY (4a)		• Automatic communication mode • See Fig. 6.		23			
			tSCKHBSY (4b)		• Mode other than automatic communication mode • See Fig. 6.		4			
	Output clock	Period	tSCK (5)	SCK1 (P45)	• CMOS output selected • See Fig. 6.		4			
		Low level pulse width	tSCKL (5)				1/2			tSCK
		High level pulse width	tSCKH (5)				1/2			
			tSCKHA (5)		• Automatic communication mode • CMOS output selected • See Fig. 6.		6			tCYC
			tSCKHBSY (5a)		• Automatic communication mode • CMOS output selected • See Fig. 6.		4		23	
			tSCKHBSY (5b)		• Mode other than automatic communication mode • See Fig. 6.		4			
Serial input	Data setup time		tsDI (3)	SI1 (P44), SB1 (P44)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (3)				0.03			
Serial output	Input clock	Output delay time	tdD0 (4)	SO1 (P43), SB1 (P44)	• (Note 4-3-2)	2.7 to 3.6			1tCYC +0.05	
	Output clock		tdDO (5)		• (Note 4-3-2)				1tCYC +0.05	

Note 4-3-1 : These specifications are theoretical values. Add margin depending on its use.
Note 4-3-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

2-2. SIO1 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-4-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	Specification				
						V_{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (6)	SCK1 (P45)	• See Fig. 6.	2.7 to 3.6	2			tCYC
		Low level pulse width	tSCKL (6)				1			
		High level pulse width	tSCKH (6)				1			
			tSCKHBSY (6)				2			
Serial input	Data setup time		tsDI (4)	SI1 (P44), SB1 (P44)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (4)				0.03			
Serial output	Input clock	Output delay time	tdD0 (6)	SO1 (P43), SB1 (P44)	• (Note 4-4-2)	2.7 to 3.6			1tCYC +0.05	

Note 4-4-1 : These specifications are theoretical values. Add margin depending on its use.
Note 4-4-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

3-1. SIO4 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-5-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Serial clock	Input clock	Period	tSCK (7)	SCK4 (PA2)	• See Fig. 6.	2.7 to 3.6	4			tCYC
		Low level pulse width	tSCKL (7)				2			
		High level pulse width	tSCKH (7)				2			
			tSCKHA (7)		• Automatic communication mode • See Fig. 6.		6			
			tSCKHBSY (7a)		• Automatic communication mode • See Fig. 6.		23			
			tSCKHBSY (7b)		• Mode other than automatic communication mode • See Fig. 6.		4			
	Output clock	Period	tSCK (8)	SCK4 (PA2)	• CMOS output selected • See Fig. 6.		4			
		Low level pulse width	tSCKL (8)				1/2			tSCK
		High level pulse width	tSCKH (8)				1/2			
			tSCKHA (8)		• Automatic communication mode • CMOS output selected • See Fig. 6.		6			tCYC
			tSCKHBSY (8a)		• Automatic communication mode • CMOS output selected • See Fig. 6.		4		23	
			tSCKHBSY (8b)		• Mode other than automatic communication mode • See Fig. 6.		4			
Serial input	Data setup time		tsDI (5)	SI4 (PA1), SB4 (PA1)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (5)				0.03			
Serial output	Input clock	Output delay time	tdD0 (7)	SO4 (PA0), SB14(PA1)	• (Note 4-5-2)	2.7 to 3.6			1tCYC +0.05	
	Output clock		tdDO (8)		• (Note 4-5-2)				1tCYC +0.05	

Note 4-5-1 : These specifications are theoretical values. Add margin depending on its use.
Note 4-5-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

3-2. SIO4 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-6-1)

Parameter			Symbol	Applicable Pin/Remarks	Conditions		Specification			
						V_{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (9)	SCK4 (P45)	• See Fig. 6.	2.7 to 3.6	2			tCYC
		Low level pulse width	tSCKL (9)				1			
		High level pulse width	tSCKH (9)				1			
			tSCKHBSY (9)				2			
Serial input	Data setup time		tsDI (6)	SI4 (P44), SB4 (P44)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (6)				0.03			
Serial output	Input clock	Output delay time	tdD0 (9)	SO4 (P43), SB4(P44)	• (Note 4-6-2)	2.7 to 3.6			1tCYC +0.05	

Note 4-6-1 : These specifications are theoretical values. Add margin depending on its use.
Note 4-6-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

4-2. SMIIC0 I²C Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions	Specification				
						V_{DD} [V]	min	typ	max	unit
Clock	Input clock	Period	tSCL	SM0CK (P22)	• See Fig. 8.	2.7 to 3.6	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
	Output clock	Period	tSCLx	SM0CK (P22)	• Specified as interval up to time when output state starts changing.	2.7 to 3.6	10			
		Low level pulse width	tSCLLx				1/2			tSCL
		High level pulse width	tSCLHx				1/2			
SM0CK and SM0DA pins input spike suppression time			tsp	SM0CK (P22) SM0DA (P23)	• See Fig. 8.	2.7 to 3.6			1	Tfilt
Bus release time between start and stop	Input		tBUF	SM0CK (P22) SM0DA (P23)	• See Fig. 8.	2.7 to 3.6	2.5			Tfilt
	Output		tBUFx	SM0CK (P22) SM0DA (P23)	• Standard clock mode • Specified as interval up to time when output state starts changing.		5.5			µsec
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			
Start/restart condition hold time	Input		tHD;STA	SM0CK (P22) SM0DA (P23)	• When SMIIC register control bit, I2CSHDS = 0 • See Fig. 8.	2.7 to 3.6	2.0			Tfilt
					• When SMIIC register control bit I2CSHDS = 1 • See Fig. 8.		2.5			
	Output		tHD;STAx	SM0CK (P22) SM0DA (P23)	• Standard clock mode • Specified as interval up to time when output state starts changing.		4.1			µsec
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.0			
Restart condition setup time	Input		tSU;STA	SM0CK (P22) SM0DA (P23)	• See Fig. 8.	2.7 to 3.6	1.0			Tfilt
	Output		tSU;STAx	SM0CK (P22) SM0DA (P23)	• Standard clock mode • Specified as interval up to time when output state starts changing.		5.5			µsec
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			

5-1. SMIIC1 Simple SIO Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions		Specification			
						V_{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (12)	SM0CK (PB4)	See Fig. 6.	2.7 to 3.6	4			tCYC
		Low level pulse width	tSCKL (12)				2			
		High level pulse width	tSCKH (12)				2			
	Output clock	Period	tSCK (13)	SM0CK (PB4)	• CMOS output selected • See Fig. 6.	2.7 to 3.6	4			tSCK
		Low level pulse width	tSCKL (13)				1/2			
		High level pulse width	tSCKH (13)				1/2			
Serial input	Data setup time		tsDI (8)	SM0DA (PB5)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (8)				0.03			
Serial output	Output delay time		tdD0 (12)	SM0DO (PB6), SM0DA (PB5)	• Specified with respect to falling edge of SIOCLK • Specified as interval up to time when output state starts changing. • See Fig. 6.	2.7 to 3.6			1tCYC +0.05	

Note 4-9-1 : These specifications are theoretical values. Add margin depending on its use.

6-1. SLIIC0 Simple SIO Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions	Specification				
						V_{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (13)	SL0CK (PA4)	See Fig. 6.	2.7 to 3.6	4			tCYC
		Low level pulse width	tSCKL (13)				2			
		High level pulse width	tSCKH (13)				2			
Serial input	Data setup time		tsDI (9)	SL0DA (PA5)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.7 to 3.6	0.03			µs
	Data hold time		thDI (9)				0.03			
Serial output	Output delay time		tdD0 (13)	SL0DO (PA6), SL0DA (PA5)	• Specified with respect to falling edge of SIOCLK • Specified as interval up to time when output state starts changing. • See Fig. 6.	2.7 to 3.6			1tCYC +0.05	

Note 4-11-1 : These specifications are theoretical values. Add margin depending on its use.

6-2. SLIIC1 I2C Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions		Specification			
						V_{DD} [V]	min	typ	max	unit
Clock	Input clock	Period	tSCL	SL0CK (PA4)	• See Fig. 8.	2.7 to 3.6	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
SL0CK and SL0DA pins input spike suppression time			tsp	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.	2.7 to 3.6			1	Tfilt
Bus release time between start and stop	Input		tBUF	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.	2.7 to 3.6	2.5			Tfilt
Start/restart condition hold time	Input		tHD;STA	SL0CK (PA4) SL0DA (PA5)	• When SMIIC register control bit, I2CSHDS = 0 • See Fig. 8.	2.7 to 3.6	2.0			Tfilt
					• When SMIIC register control bit I2CSHDS = 1 • See Fig. 8.		2.5			
Restart condition setup time	Input		tSU;STA	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.	2.7 to 3.6	1.0			Tfilt
Stop condition setup time	Input		tSU;STO	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.	2.7 to 3.6	1.0			Tfilt
Data hold time	Input		tHD;DAT	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.	2.7 to 3.6	0			Tfilt
	Output		tHD;DATx	SL0CK (PA4) SL0DA (PA5)	• Specified as interval up to time when output state starts changing.		1		1.5	
Data setup time	Input		tSU;DAT	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.	2.7 to 3.6	1			Tfilt
	Output		tSU;DATx	SL0CK (PA4) SL0DA (PA5)	• Specified as interval up to time when output state starts changing.		1tSCL-1.5Tfilt			

■ Consumption Current Characteristics at Ta = –40 to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = V_{SS}4 = 0$ V

typ : 3.3 V

Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	Typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP (1)	VDD1 =VDD2 =VDD3 =VDD4	• FmCF = 12 MHz ceramic oscillator mode • FmX'tal = 32.768 kHz crystal oscillation mode • System clock set to 12 MHz • Internal RC oscillation stopped • 1/1 frequency division mode	3.0 to 3.6		5.5	13.0	mA
	IDDOP (2)		• FmCF = 10 MHz ceramic oscillator mode • FmX'tal = 32.768 kHz crystal oscillator mode • System clock set to 10 MHz • Internal RC oscillation stopped • 1/1 frequency division mode	2.7 to 3.6		5.0	12.0	
	IDDOP (3)		• FmCF = 0 Hz (oscillation stopped) • FmX'tal = 32.768 kHz crystal oscillator mode • System clock set to internal RC oscillation • 1/1 frequency division mode	2.7 to 3.6		0.75	1.8	
	IDDOP (4)		• FmCF = 0 Hz (oscillation stopped) • FmX'tal = 32.768 kHz crystal oscillator mode • System clock set to 32.768 kHz • Internal RC oscillation stopped • 1/1 frequency division mode	2.7 to 3.6		30	120	μA

Continued on next page.

Continued from preceding page.

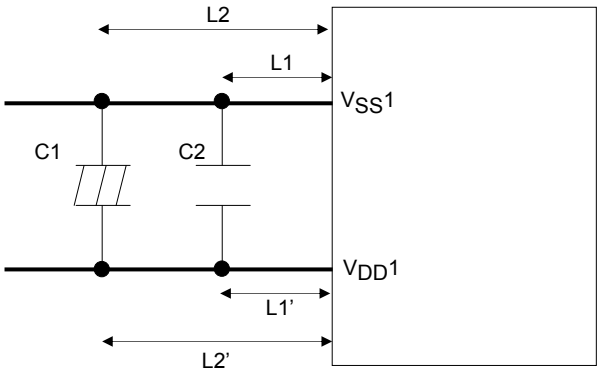
Parameter	Symbol	Applicable Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT (1)	VDD1 =VDD2 =VDD3 =VDD4	• HALT mode • FmCF =12 MHz ceramic oscillator mode • FmX'tal = 32.768 kHz crystal oscillation mode • System clock set to 12 MHz • Internal RC oscillation stopped • 1/1 frequency division mode	3.0 to 3.6		1.7	3.5	mA
	IDDHALT (2)		• HALT mode • FmCF = 10 MHz ceramic oscillator mode • FmX'tal = 32.768 kHz crystal oscillator mode • System clock set to 10 MHz • Internal RC oscillation stopped • 1/1 frequency division mode	2.7 to 3.6		1.5	3.2	
	IDDHALT (3)		• HALT mode • FmCF = 0 Hz (oscillation stopped) • FmX'tal = 32.768 kHz crystal oscillator mode • System clock set to internal RC oscillation • 1/1 frequency division mode	2.7 to 3.6		0.2	0.8	
	IDDHALT (4)		• HALT mode • FmCF = 0 Hz (oscillation stopped) • FmX'tal = 32.768 kHz crystal oscillator mode • System clock set to 32.768 kHz • Internal RC oscillation stopped • 1/1 frequency division mode	2.7 to 3.6		8.5	65	μA

Continued on next page.

■ Power Pin Treatment Conditions 1 (VDD1, VSS1)

Connect capacitors that meet the following conditions between the $V_{DD}1$ and $V_{SS}1$ pins :

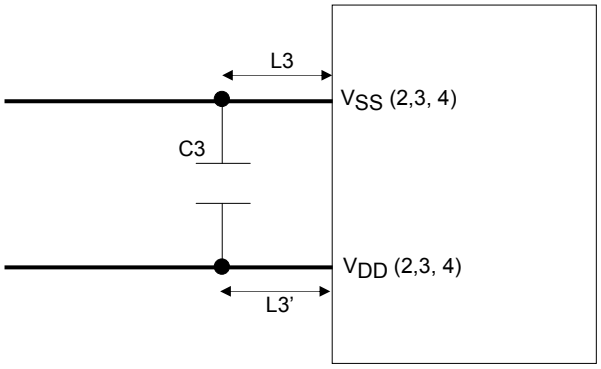
- Connect among the $V_{DD}1$ and $V_{SS}1$ pins and the capacitors C1 and C2 with the shortest possible lead wires, of the same length (L1=L1', L2=L2') wherever possible.
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel. The capacitance of C2 should be approximately 0.1 μF or larger.
- The $V_{DD}1$ and $V_{SS}1$ traces must be thicker than the other traces.



■ Power Pin Treatment Conditions 2 (VDD(2, 3, 4), VSS(2, 3, 4))

Connect capacitors that meet the following condition between the VDD(2, 3, 4) and VSS(2, 3, 4) pins :

- Connect among the VDD(2, 3, 4) and VSS(2, 3, 4) pins and the capacitor C3 with the shortest possible lead wires, of the same length (L3=L3') wherever possible.
- The capacitance of C3 should be approximately 0.1 μF or larger.
- The VDD(2, 3, 4) and VSS(2, 3, 4) traces must be thicker than the other traces.



■ Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a ON Semiconductor-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

■ Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

Nominal Frequency	Vendor Name	Resonator	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [ms]	max [ms]	
12 MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	OPEN	330	2.2 to 3.6	0.02	0.2	C1, C2 integrated type
10 MHz		CSTCE10M0G52-R0	(10)	(10)	OPEN	680	2.2 to 3.6	0.02	0.2	C1, C2 integrated type
		CSTLS10M0G53-B0	(15)	(15)	OPEN	680	2.2 to 3.6	0.02	0.2	C1, C2 integrated type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after VDD goes above the lower limit level of the operating voltage range (see Figure 4)

■ Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a ON Semiconductor-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

■ Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Resonator

Nominal Frequency	Vendor Name	Resonator	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768 kHz	EPSON TOYOCOM	MC-306	10	10	Open	330K	2.2 to 3.6	1.0	3.0	CL=7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillator circuit is executed plus the time interval that is required for the oscillation to get stabilized after the HOLD mode is released (see Figure 4).

Note : The traces to and from the components that are involved in oscillation should be kept as short as possible as the oscillation characteristics are affected by their trace pattern.

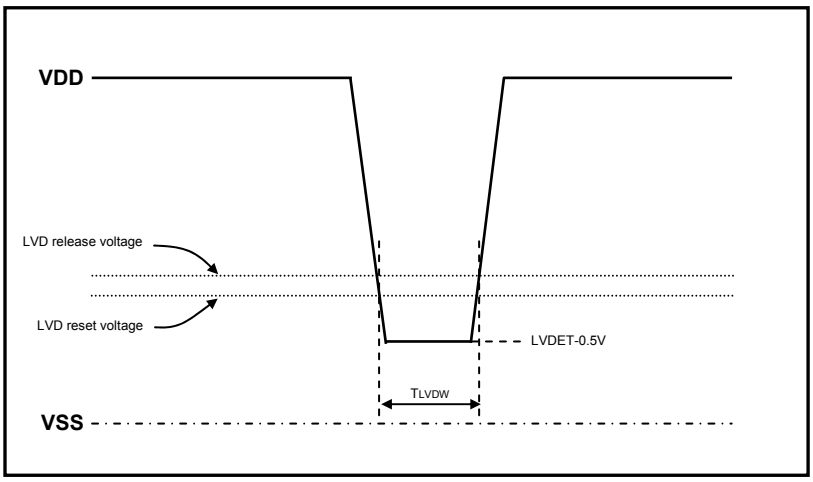


Figure 12 Low voltage detection minimum width (Example of momentary power loss / Voltage variation waveform)

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC88FC2H0AVUTE-2H	TQFP100(14X14) (Pb-Free / Halogen Free)	450 / Tray JEDEC