Renesas Electronics America Inc - R5F524UBADFB#30 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	110
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 22x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524ubadfb-30

1.3 Block Diagram

Figure 1.2 shows a block diagram.

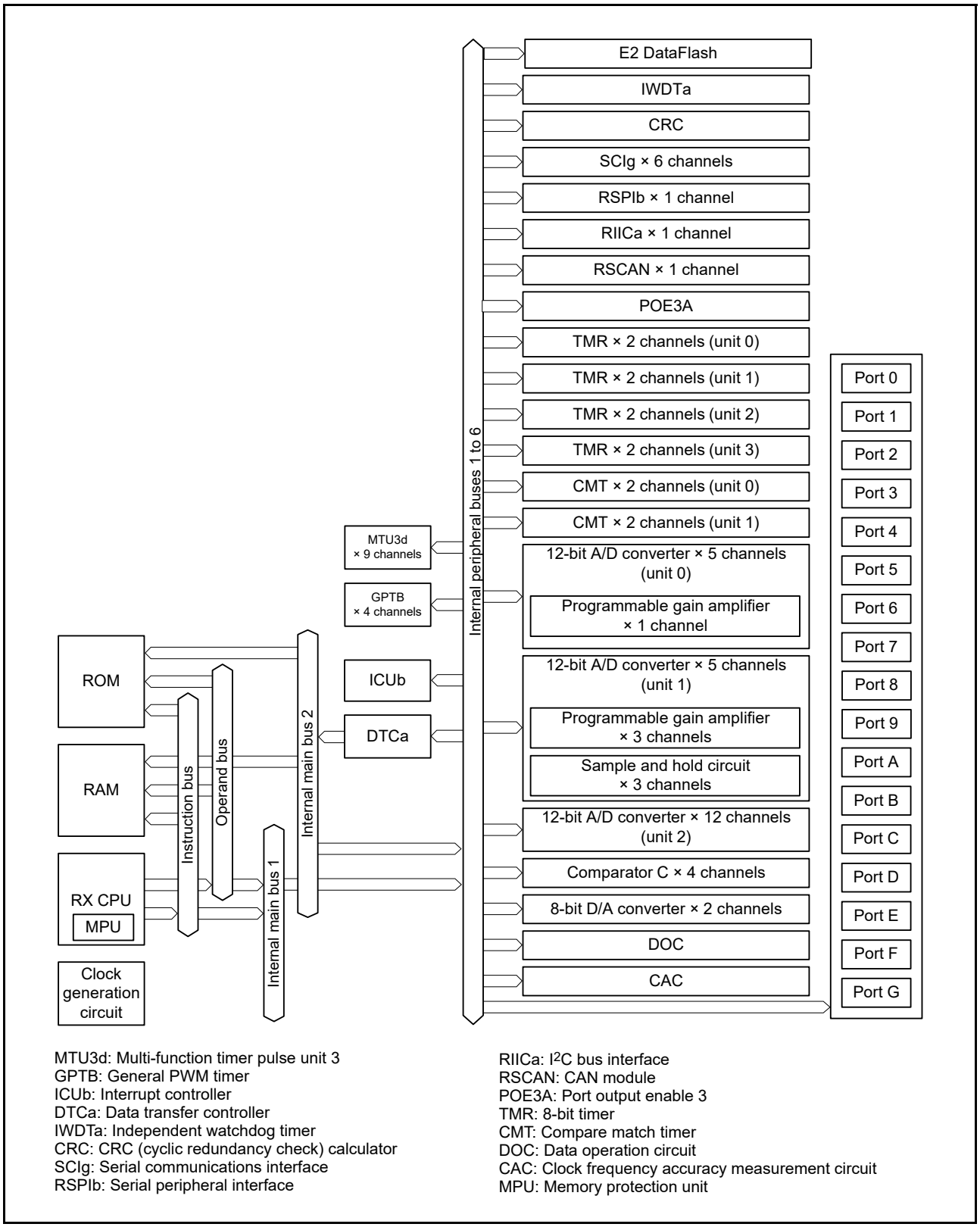


Figure 1.2 Block Diagram

Table 1.4 Pin Functions (2/4)

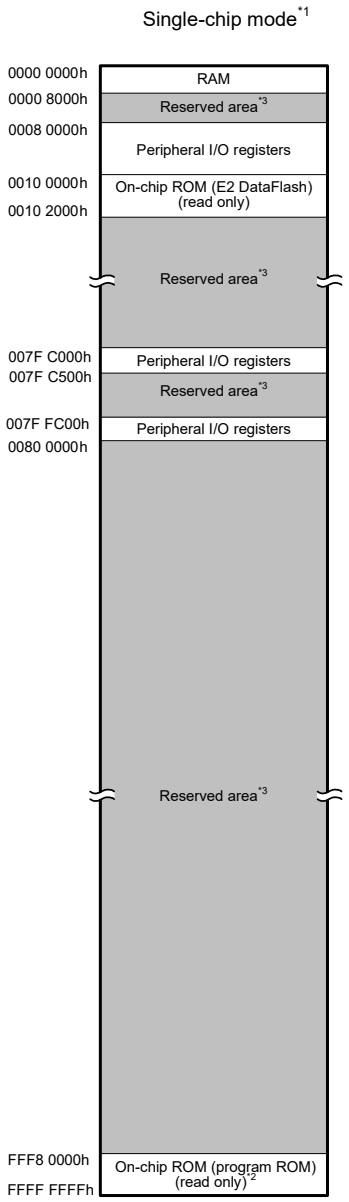
Classifications	Pin Name	I/O	Description
Multi-function timer pulse unit 3 (MTU3d)	MTIOC9A#, MTIOC9B#, MTIOC9C#, MTIOC9D#	I/O	The TGRA9 to TGRD9 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
	MTCLKA#, MTCLKB#, MTCLKC#, MTCLKD#	Input	Inverted input pins for the external clock.
	ADSM0, ADSM1	Output	A/D trigger output pins.
General PWM timer (GPTB)	GTIOC0A, GTIOC0B	I/O	The GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins
	GTIOC0A#, GTIOC0B#	I/O	The GPT0.GTGRA and GPT0.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTIOC1A, GTIOC1B	I/O	The GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins
	GTIOC1A#, GTIOC1B#	I/O	The GPT1.GTGRA and GPT1.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTIOC2A, GTIOC2B	I/O	The GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins
	GTIOC2A#, GTIOC2B#	I/O	The GPT2.GTGRA and GPT2.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTIOC3A, GTIOC3B	I/O	The GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins
	GTIOC3A#, GTIOC3B#	I/O	The GPT3.GTGRA and GPT3.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTETRG	Input	External trigger input pin for GPT0 to GPT3
	GTECLKA, GTECLKB, GTECLKC, GTECLKD	Input	Input pins A to D for the external clock
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
8-bit timer (TMR)	TMO0 to TMO7	Output	Compare match output pins.
	TMCI0 to TMCI7	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI7	Input	Counter reset input pins.
Port output enable 3 (POE3A)	POE0#, POE4#, POE8#, POE10#, POE11#, POE12#	Input	Input pins for request signals to switch the MTU and GPT pins between the high impedance state or operation as general I/O port pins
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5, SCK6, SCK8, SCK9, SCK11	I/O	Input/output pins for the clock.
	RXD1, RXD5, RXD6, RXD8, RXD9, RXD11	Input	Input pins for received data.
	TXD1, TXD5, TXD6, TXD8, TXD9, TXD11	Output	Output pins for transmitted data.
	CTS1#, CTS5#, CTS6#, CTS8#, CTS9#, CTS11#	Input	Input pins for controlling the start of transmission and reception.
	RTS1#, RTS5#, RTS6#, RTS8#, RTS9#, RTS11#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL1, SSCL5, SSCL6, SSCL8, SSCL9, SSCL11	I/O	Input/output pins for the I^2C clock.
	SSDA1, SSDA5, SSDA6, SSDA8, SSDA9, SSDA11	I/O	Input/output pins for the I^2C data.
	• Simple SPI mode		
	SCK1, SCK5, SCK6, SCK8, SCK9, SCK11	I/O	Input/output pins for the clock.

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU3, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
1		PE5			IRQ0
2		P02	MTIOC9D, MTIOC9D#	CTS1#, RTS1#, SS1#	IRQ5, ADST0
3	VSS				
4		P00			IRQ2, ADST1
5	VCL				
6	MD				FINED
7		P01	POE12#		IRQ4, ADST2
8		PE4	MTCLKC, MTCLKC#, POE10#		IRQ1
9		PE3	MTCLKD, MTCLKD#, POE11#		IRQ2
10	RES#				
11	XTAL	P37			
12	VSS				
13	EXTAL	P36			
14	VCC				
15		PE2	POE10#		NMI
16		PE1	MTIOC9D, MTIOC9D#, TMO5	CTS5#, RTS5#, SS5#, SSLA3	
17		PE0	MTIOC9B, MTIOC9B#, TMCI1, TMCI5	RXD5, SMISO5, SSCL5, SSLA2	
18		PD7	MTIOC9A, MTIOC9A#, TMRI1, TMRI5, GTIOC3A, GTIOC3A#	TXD5, SMOSI5, SSDA5, SSLA1	
19		PD6	MTIOC9C, MTIOC9C#, TMO1, GTIOC3B, GTIOC3B#	CTS1#, RTS1#, SS1#, CTS11#, RTS11#, SS11#, SSLA0	IRQ5, ADST0
20		PD5	TMRI0, TMRI6, GTECLKA	RXD1, SMISO1, SSCL1, RXD11, SMISO11, SSCL11	IRQ3
21		PD4	TMCI0, TMCI6, GTECLKB	SCK1, SCK11	IRQ2
22		PD3	TMO0, GTECLKC	TXD1, SMOSI1, SSDA1, TXD11, SMOSI11, SSDA11	
23		PD2	TMCI1, TMO4, GTIOC0A, GTIOC0A#	SCK5, MOSIA	
24		PD1	TMO2, GTIOC0B, GTIOC0B#	MISOA	
25		PD0	TMO6, GTIOC1A, GTIOC1A#	RSPCKA	
26		PB7	GTIOC1B, GTIOC1B#	SCK5	
27		PB6	GTIOC2A, GTIOC2A#	RXD5, SMISO5, SSCL5	IRQ5
28		PB5	GTIOC2B, GTIOC2B#	TXD5, SMOSI5, SSDA5	
29	VCC				
30		PB4	POE8#, GTETRG, GTECLKD	CTS5#, RTS5#, SS5#	IRQ3
31	VSS				
32		PB3	MTIOC0A, MTIOC0A#, CACREF	SCK6, RSPCKA	
33		PB2	MTIOC0B, MTIOC0B#, TMRI0, ADSM0	TXD6, SMOSI6, SSDA6, SDA0	
34		PB1	MTIOC0C, MTIOC0C#, TMCI0, ADSM1	RXD6, SMISO6, SSCL6, SCL0	
35		PB0	MTIOC0D, MTIOC0D#, TMO0	TXD6, SMOSI6, SSDA6, MOSIA	ADTRG2#
36		PA5	MTIOC1A, MTIOC1A#, TMCI3	RXD6, SMISO6, SSCL6, MISOA	IRQ1, ADTRG1#
37		PA4	MTIOC1B, MTIOC1B#, TMCI7	SCK6, RSPCKA	ADTRG0#
38		PA3	MTIOC2A, MTIOC2A#, TMRI7, GTADSM0	SSLA0	
39		PA2	MTIOC2B, MTIOC2B#, TMO7, GTADSM1	CTS6#, RTS6#, SS6#, SSLA1	
40		PA1	MTIOC6A, MTIOC6A#, TMO4	SSLA2, CRXD0	ADTRG0#
41		PA0	MTIOC6C, MTIOC6C#, TMO2	SSLA3, CTXD0	
42	VCC				
43		P96	POE4#		IRQ4
44	VSS				
45		P95	MTIOC6B, MTIOC6B#		
46		P94	MTIOC7A, MTIOC7A#		
47		P93	MTIOC7B, MTIOC7B#		
48		P92	MTIOC6D, MTIOC6D#		
49		P91	MTIOC7C, MTIOC7C#		
50		P90	MTIOC7D, MTIOC7D#		

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU3, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
92	AVCC1				
93	AVCC0				
94	AVSS0				
95	AVSS1				
96		P82	MTIC5U, MTIC5U#, TMO4	SCK6	
97		P81	MTIC5V, MTIC5V#, TMCI4	TXD6, SMOSI6, SSDA6	
98		P80	MTIC5W, MTIC5W#, TMRI4	RXD6, SMISO6, SSCL6	
99		P11	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3		IRQ1
100		P10	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0



Note 1. The address space in boot mode is the same as the address space in single-chip mode.

Note 2. The capacity of ROM differs depending on the products.

ROM (bytes)		RAM (bytes)		E2 DataFlash (bytes)	
Capacity	**Address**	**Capacity**	**Address**	**Capacity**	**Address**
512 K	FFF8 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh	8 K	0010 0000h to 0010 1FFFh
384 K	FFFA 0000h to FFFF FFFFh				
256 K	FFFC 0000h to FFFF FFFFh				

Note: See Table 1.3 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 4.1, List of I/O Registers (Address Order).
The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided clock synchronization cycles +
Number of bus cycles for internal peripheral bus 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.
When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.
In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the bus access from the different bus master (DTC).

(4) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

(5) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by ‘SYSTEM’ in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

Table 4.1 List of I/O Registers (Address Order) (2/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8	2 ICLK
0008 7017h	ICU	Interrupt Request Register 023	IR023	8	8	2 ICLK
0008 701Bh	ICU	Interrupt Request Register 027	IR027	8	8	2 ICLK
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8	2 ICLK
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8	2 ICLK
0008 701Eh	ICU	Interrupt Request Register 030	IR030	8	8	2 ICLK
0008 701Fh	ICU	Interrupt Request Register 031	IR031	8	8	2 ICLK
0008 7020h	ICU	Interrupt Request Register 032	IR032	8	8	2 ICLK
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8	2 ICLK
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8	2 ICLK
0008 7028h	ICU	Interrupt Request Register 040	IR040	8	8	2 ICLK
0008 7029h	ICU	Interrupt Request Register 041	IR041	8	8	2 ICLK
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK
0008 7030h	ICU	Interrupt Request Register 048	IR048	8	8	2 ICLK
0008 7031h	ICU	Interrupt Request Register 049	IR049	8	8	2 ICLK
0008 7032h	ICU	Interrupt Request Register 050	IR050	8	8	2 ICLK
0008 7033h	ICU	Interrupt Request Register 051	IR051	8	8	2 ICLK
0008 7034h	ICU	Interrupt Request Register 052	IR052	8	8	2 ICLK
0008 7035h	ICU	Interrupt Request Register 053	IR053	8	8	2 ICLK
0008 7036h	ICU	Interrupt Request Register 054	IR054	8	8	2 ICLK
0008 7037h	ICU	Interrupt Request Register 055	IR055	8	8	2 ICLK
0008 7038h	ICU	Interrupt Request Register 056	IR056	8	8	2 ICLK
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK
0008 703Bh	ICU	Interrupt Request Register 059	IR059	8	8	2 ICLK
0008 703Ch	ICU	Interrupt Request Register 060	IR060	8	8	2 ICLK
0008 703Dh	ICU	Interrupt Request Register 061	IR061	8	8	2 ICLK
0008 703Eh	ICU	Interrupt Request Register 062	IR062	8	8	2 ICLK
0008 703Fh	ICU	Interrupt Request Register 063	IR063	8	8	2 ICLK
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 7322h	ICU	Interrupt Source Priority Register 034	IPR034	8	8	2 ICLK
0008 7328h	ICU	Interrupt Source Priority Register 040	IPR040	8	8	2 ICLK
0008 7329h	ICU	Interrupt Source Priority Register 041	IPR041	8	8	2 ICLK
0008 732Ch	ICU	Interrupt Source Priority Register 044	IPR044	8	8	2 ICLK
0008 7330h	ICU	Interrupt Source Priority Register 048	IPR048	8	8	2 ICLK
0008 7331h	ICU	Interrupt Source Priority Register 049	IPR049	8	8	2 ICLK
0008 7332h	ICU	Interrupt Source Priority Register 050	IPR050	8	8	2 ICLK
0008 7333h	ICU	Interrupt Source Priority Register 051	IPR051	8	8	2 ICLK
0008 7334h	ICU	Interrupt Source Priority Register 052	IPR052	8	8	2 ICLK
0008 7335h	ICU	Interrupt Source Priority Register 053	IPR053	8	8	2 ICLK
0008 7336h	ICU	Interrupt Source Priority Register 054	IPR054	8	8	2 ICLK
0008 7337h	ICU	Interrupt Source Priority Register 055	IPR055	8	8	2 ICLK
0008 7338h	ICU	Interrupt Source Priority Register 056	IPR056	8	8	2 ICLK
0008 7339h	ICU	Interrupt Source Priority Register 057	IPR057	8	8	2 ICLK
0008 733Bh	ICU	Interrupt Source Priority Register 059	IPR059	8	8	2 ICLK
0008 733Ch	ICU	Interrupt Source Priority Register 060	IPR060	8	8	2 ICLK
0008 733Dh	ICU	Interrupt Source Priority Register 061	IPR061	8	8	2 ICLK
0008 733Eh	ICU	Interrupt Source Priority Register 062	IPR062	8	8	2 ICLK
0008 733Fh	ICU	Interrupt Source Priority Register 063	IPR063	8	8	2 ICLK
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8	2 ICLK
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8	2 ICLK
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8	2 ICLK
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8	2 ICLK
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8	2 ICLK
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8	2 ICLK
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8	2 ICLK
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8	2 ICLK
0008 7358h	ICU	Interrupt Source Priority Register 088	IPR088	8	8	2 ICLK
0008 7359h	ICU	Interrupt Source Priority Register 089	IPR089	8	8	2 ICLK
0008 7362h	ICU	Interrupt Source Priority Register 098	IPR098	8	8	2 ICLK
0008 7363h	ICU	Interrupt Source Priority Register 099	IPR099	8	8	2 ICLK
0008 7364h	ICU	Interrupt Source Priority Register 100	IPR100	8	8	2 ICLK
0008 7365h	ICU	Interrupt Source Priority Register 101	IPR101	8	8	2 ICLK
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK
0008 7368h	ICU	Interrupt Source Priority Register 104	IPR104	8	8	2 ICLK
0008 7369h	ICU	Interrupt Source Priority Register 105	IPR105	8	8	2 ICLK
0008 736Ah	ICU	Interrupt Source Priority Register 106	IPR106	8	8	2 ICLK
0008 736Bh	ICU	Interrupt Source Priority Register 107	IPR107	8	8	2 ICLK
0008 736Ch	ICU	Interrupt Source Priority Register 108	IPR108	8	8	2 ICLK
0008 736Dh	ICU	Interrupt Source Priority Register 109	IPR109	8	8	2 ICLK
0008 736Eh	ICU	Interrupt Source Priority Register 110	IPR110	8	8	2 ICLK
0008 736Fh	ICU	Interrupt Source Priority Register 111	IPR111	8	8	2 ICLK
0008 7370h	ICU	Interrupt Source Priority Register 112	IPR112	8	8	2 ICLK
0008 7371h	ICU	Interrupt Source Priority Register 113	IPR113	8	8	2 ICLK
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK
0008 7376h	ICU	Interrupt Source Priority Register 118	IPR118	8	8	2 ICLK
0008 7379h	ICU	Interrupt Source Priority Register 121	IPR121	8	8	2 ICLK
0008 737Bh	ICU	Interrupt Source Priority Register 123	IPR123	8	8	2 ICLK
0008 737Dh	ICU	Interrupt Source Priority Register 125	IPR125	8	8	2 ICLK
0008 737Fh	ICU	Interrupt Source Priority Register 127	IPR127	8	8	2 ICLK
0008 7381h	ICU	Interrupt Source Priority Register 129	IPR129	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (12/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8219h	TMR3	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8220h	TMR4	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8221h	TMR5	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8222h	TMR4	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8223h	TMR5	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8224h	TMR4	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8225h	TMR5	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8226h	TMR4	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8227h	TMR5	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8228h	TMR4	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8229h	TMR5	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 822Ah	TMR4	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 822Bh	TMR5	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8230h	TMR6	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8231h	TMR7	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8232h	TMR6	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8233h	TMR7	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8234h	TMR6	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8235h	TMR7	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8236h	TMR6	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8237h	TMR7	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8238h	TMR6	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8239h	TMR7	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 823Ah	TMR6	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 823Bh	TMR7	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB
0008 8300h	RIIC0	I^2C-bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB
0008 8301h	RIIC0	I^2C-bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB
0008 8302h	RIIC0	I^2C-bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB
0008 8303h	RIIC0	I^2C-bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB
0008 8304h	RIIC0	I^2C-bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB
0008 8305h	RIIC0	I^2C-bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB
0008 8306h	RIIC0	I^2C-bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB
0008 8307h	RIIC0	I^2C-bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB
0008 8308h	RIIC0	I^2C-bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB
0008 8309h	RIIC0	I^2C-bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (19/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 C068h	PORT8	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C069h	PORT9	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Fh	PORTF	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C070h	PORTG	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C080h	PORT0	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C08Eh	PORT7	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C08Fh	PORT7	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C090h	PORT8	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C091h	PORT8	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C092h	PORT9	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C093h	PORT9	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C09Bh	PORTD	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C09Eh	PORTF	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C0A0h	PORTG	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C4h	PORT4	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C6h	PORT6	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C7h	PORT7	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C8h	PORT8	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C9h	PORT9	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CCh	PORTC	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CDh	PORTD	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CFh	PORTF	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0D0h	PORTG	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0E0h	PORT0	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (20/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E3h	PORT3	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E7h	PORT7	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E8h	PORT8	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E9h	PORT9	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0ECh	PORTC	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EFh	PORTF	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0F0h	PORTG	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 or 3 PCLKB
0008 C140h	MPC	P00 Pin Function Control Register	P00PFS	8	8	2 or 3 PCLKB
0008 C141h	MPC	P01 Pin Function Control Register	P01PFS	8	8	2 or 3 PCLKB
0008 C142h	MPC	P02 Pin Function Control Register	P02PFS	8	8	2 or 3 PCLKB
0008 C148h	MPC	P10 Pin Function Control Register	P10PFS	8	8	2 or 3 PCLKB
0008 C149h	MPC	P11 Pin Function Control Register	P11PFS	8	8	2 or 3 PCLKB
0008 C14Ah	MPC	P12 Pin Function Control Register	P12PFS	8	8	2 or 3 PCLKB
0008 C14Bh	MPC	P13 Pin Function Control Register	P13PFS	8	8	2 or 3 PCLKB
0008 C14Ch	MPC	P14 Pin Function Control Register	P14PFS	8	8	2 or 3 PCLKB
0008 C14Dh	MPC	P15 Pin Function Control Register	P15PFS	8	8	2 or 3 PCLKB
0008 C14Eh	MPC	P16 Pin Function Control Register	P16PFS	8	8	2 or 3 PCLKB
0008 C14Fh	MPC	P17 Pin Function Control Register	P17PFS	8	8	2 or 3 PCLKB
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2 or 3 PCLKB
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2 or 3 PCLKB
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2 or 3 PCLKB
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2 or 3 PCLKB
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2 or 3 PCLKB
0008 C155h	MPC	P25 Pin Function Control Register	P25PFS	8	8	2 or 3 PCLKB
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2 or 3 PCLKB
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2 or 3 PCLKB
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2 or 3 PCLKB
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2 or 3 PCLKB
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2 or 3 PCLKB
0008 C15Bh	MPC	P33 Pin Function Control Register	P33PFS	8	8	2 or 3 PCLKB
0008 C15Ch	MPC	P34 Pin Function Control Register	P34PFS	8	8	2 or 3 PCLKB
0008 C15Dh	MPC	P35 Pin Function Control Register	P35PFS	8	8	2 or 3 PCLKB
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2 or 3 PCLKB
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2 or 3 PCLKB
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2 or 3 PCLKB
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2 or 3 PCLKB
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2 or 3 PCLKB
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2 or 3 PCLKB
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2 or 3 PCLKB
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2 or 3 PCLKB
0008 C168h	MPC	P50 Pin Function Control Register	P50PFS	8	8	2 or 3 PCLKB
0008 C169h	MPC	P51 Pin Function Control Register	P51PFS	8	8	2 or 3 PCLKB
0008 C16Ah	MPC	P52 Pin Function Control Register	P52PFS	8	8	2 or 3 PCLKB
0008 C16Bh	MPC	P53 Pin Function Control Register	P53PFS	8	8	2 or 3 PCLKB
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (25/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000A 83B2h	RSCAN	Receive Buffer Register 1AH	RMIDH1	16	16	2 or 3 PCLKB
000A 83B4h	RSCAN	Receive Rule Entry Register 1CL	GAFLPL1	16	16	2 or 3 PCLKB
000A 83B4h	RSCAN	Receive Buffer Register 1BL	RMTS1	16	16	2 or 3 PCLKB
000A 83B6h	RSCAN	Receive Rule Entry Register 1CH	GAFLPH1	16	16	2 or 3 PCLKB
000A 83B6h	RSCAN	Receive Buffer Register 1BH	RMPTR1	16	16	2 or 3 PCLKB
000A 83B8h	RSCAN	Receive Rule Entry Register 2AL	GAFLIDL2	16	16	2 or 3 PCLKB
000A 83B8h	RSCAN	Receive Buffer Register 1CL	RMDF01	16	16	2 or 3 PCLKB
000A 83BAh	RSCAN	Receive Rule Entry Register 2AH	GAFLIDH2	16	16	2 or 3 PCLKB
000A 83BAh	RSCAN	Receive Buffer Register 1CH	RMDF11	16	16	2 or 3 PCLKB
000A 83BCh	RSCAN	Receive Rule Entry Register 2BL	GAFLML2	16	16	2 or 3 PCLKB
000A 83BCh	RSCAN	Receive Buffer Register 1DL	RMDF21	16	16	2 or 3 PCLKB
000A 83BEh	RSCAN	Receive Rule Entry Register 2BH	GAFLMH2	16	16	2 or 3 PCLKB
000A 83BEh	RSCAN	Receive Buffer Register 1DH	RMDF31	16	16	2 or 3 PCLKB
000A 83C0h	RSCAN	Receive Rule Entry Register 2CL	GAFLPL2	16	16	2 or 3 PCLKB
000A 83C0h	RSCAN	Receive Buffer Register 2AL	RMIDL2	16	16	2 or 3 PCLKB
000A 83C2h	RSCAN	Receive Rule Entry Register 2CH	GAFLPH2	16	16	2 or 3 PCLKB
000A 83C2h	RSCAN	Receive Buffer Register 2AH	RMIDH2	16	16	2 or 3 PCLKB
000A 83C4h	RSCAN	Receive Rule Entry Register 3AL	GAFLIDL3	16	16	2 or 3 PCLKB
000A 83C4h	RSCAN	Receive Buffer Register 2BL	RMTS2	16	16	2 or 3 PCLKB
000A 83C6h	RSCAN	Receive Rule Entry Register 3AH	GAFLIDH3	16	16	2 or 3 PCLKB
000A 83C6h	RSCAN	Receive Buffer Register 2BH	RMPTR2	16	16	2 or 3 PCLKB
000A 83C8h	RSCAN	Receive Rule Entry Register 3BL	GAFLML3	16	16	2 or 3 PCLKB
000A 83C8h	RSCAN	Receive Buffer Register 2CL	RMDF02	16	16	2 or 3 PCLKB
000A 83CAh	RSCAN	Receive Rule Entry Register 3BH	GAFLMH3	16	16	2 or 3 PCLKB
000A 83CAh	RSCAN	Receive Buffer Register 2CH	RMDF12	16	16	2 or 3 PCLKB
000A 83CCh	RSCAN	Receive Rule Entry Register 3CL	GAFLPL3	16	16	2 or 3 PCLKB
000A 83CCh	RSCAN	Receive Buffer Register 2DL	RMDF22	16	16	2 or 3 PCLKB
000A 83CEh	RSCAN	Receive Rule Entry Register 3CH	GAFLPH3	16	16	2 or 3 PCLKB
000A 83CEh	RSCAN	Receive Buffer Register 2DH	RMDF32	16	16	2 or 3 PCLKB
000A 83D0h	RSCAN	Receive Rule Entry Register 4AL	GAFLIDL4	16	16	2 or 3 PCLKB
000A 83D0h	RSCAN	Receive Buffer Register 3AL	RMIDL3	16	16	2 or 3 PCLKB
000A 83D2h	RSCAN	Receive Rule Entry Register 4AH	GAFLIDH4	16	16	2 or 3 PCLKB
000A 83D2h	RSCAN	Receive Buffer Register 3AH	RMIDH3	16	16	2 or 3 PCLKB
000A 83D4h	RSCAN	Receive Rule Entry Register 4BL	GAFLML4	16	16	2 or 3 PCLKB
000A 83D4h	RSCAN	Receive Buffer Register 3BL	RMTS3	16	16	2 or 3 PCLKB
000A 83D6h	RSCAN	Receive Rule Entry Register 4BH	GAFLMH4	16	16	2 or 3 PCLKB
000A 83D6h	RSCAN	Receive Buffer Register 3BH	RMPTR3	16	16	2 or 3 PCLKB
000A 83D8h	RSCAN	Receive Rule Entry Register 4CL	GAFLPL4	16	16	2 or 3 PCLKB
000A 83D8h	RSCAN	Receive Buffer Register 3CL	RMDF03	16	16	2 or 3 PCLKB
000A 83DAh	RSCAN	Receive Rule Entry Register 4CH	GAFLPH4	16	16	2 or 3 PCLKB
000A 83DAh	RSCAN	Receive Buffer Register 3CH	RMDF13	16	16	2 or 3 PCLKB
000A 83DCh	RSCAN	Receive Rule Entry Register 5AL	GAFLIDL5	16	16	2 or 3 PCLKB
000A 83DCh	RSCAN	Receive Buffer Register 3DL	RMDF23	16	16	2 or 3 PCLKB
000A 83DEh	RSCAN	Receive Rule Entry Register 5AH	GAFLIDH5	16	16	2 or 3 PCLKB
000A 83DEh	RSCAN	Receive Buffer Register 3DH	RMDF33	16	16	2 or 3 PCLKB
000A 83E0h	RSCAN	Receive Rule Entry Register 5BL	GAFLML5	16	16	2 or 3 PCLKB
000A 83E0h	RSCAN	Receive Buffer Register 4AL	RMIDL4	16	16	2 or 3 PCLKB
000A 83E2h	RSCAN	Receive Rule Entry Register 5BH	GAFLMH5	16	16	2 or 3 PCLKB
000A 83E2h	RSCAN	Receive Buffer Register 4AH	RMIDH4	16	16	2 or 3 PCLKB
000A 83E4h	RSCAN	Receive Rule Entry Register 5CL	GAFLPL5	16	16	2 or 3 PCLKB
000A 83E4h	RSCAN	Receive Buffer Register 4BL	RMTS4	16	16	2 or 3 PCLKB
000A 83E6h	RSCAN	Receive Rule Entry Register 5CH	GAFLPH5	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (27/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000A 841Ah	RSCAN	Receive Buffer Register 7CH	RMDF17	16	16	2 or 3 PCLKB
000A 841Ch	RSCAN	Receive Rule Entry Register 10BL	GAFLML10	16	16	2 or 3 PCLKB
000A 841Ch	RSCAN	Receive Buffer Register 7DL	RMDF27	16	16	2 or 3 PCLKB
000A 841Eh	RSCAN	Receive Rule Entry Register 10BH	GAFLMH10	16	16	2 or 3 PCLKB
000A 841Eh	RSCAN	Receive Buffer Register 7DH	RMDF37	16	16	2 or 3 PCLKB
000A 8420h	RSCAN	Receive Rule Entry Register 10CL	GAFLPL10	16	16	2 or 3 PCLKB
000A 8420h	RSCAN	Receive Buffer Register 8AL	RMIDL8	16	16	2 or 3 PCLKB
000A 8422h	RSCAN	Receive Rule Entry Register 10CH	GAFLPH10	16	16	2 or 3 PCLKB
000A 8422h	RSCAN	Receive Buffer Register 8AH	RMIDH8	16	16	2 or 3 PCLKB
000A 8424h	RSCAN	Receive Rule Entry Register 11AL	GAFLIDL11	16	16	2 or 3 PCLKB
000A 8424h	RSCAN	Receive Buffer Register 8BL	RMTS8	16	16	2 or 3 PCLKB
000A 8426h	RSCAN	Receive Rule Entry Register 11AH	GAFLIDH11	16	16	2 or 3 PCLKB
000A 8426h	RSCAN	Receive Buffer Register 8BH	RMPTR8	16	16	2 or 3 PCLKB
000A 8428h	RSCAN	Receive Rule Entry Register 11BL	GAFLML11	16	16	2 or 3 PCLKB
000A 8428h	RSCAN	Receive Buffer Register 8CL	RMDF08	16	16	2 or 3 PCLKB
000A 842Ah	RSCAN	Receive Rule Entry Register 11BH	GAFLMH11	16	16	2 or 3 PCLKB
000A 842Ah	RSCAN	Receive Buffer Register 8CH	RMDF18	16	16	2 or 3 PCLKB
000A 842Ch	RSCAN	Receive Rule Entry Register 11CL	GAFLPL11	16	16	2 or 3 PCLKB
000A 842Ch	RSCAN	Receive Buffer Register 8DL	RMDF28	16	16	2 or 3 PCLKB
000A 842Eh	RSCAN	Receive Rule Entry Register 11CH	GAFLPH11	16	16	2 or 3 PCLKB
000A 842Eh	RSCAN	Receive Buffer Register 8DH	RMDF38	16	16	2 or 3 PCLKB
000A 8430h	RSCAN	Receive Rule Entry Register 12AL	GAFLIDL12	16	16	2 or 3 PCLKB
000A 8430h	RSCAN	Receive Buffer Register 9AL	RMIDL9	16	16	2 or 3 PCLKB
000A 8432h	RSCAN	Receive Rule Entry Register 12AH	GAFLIDH12	16	16	2 or 3 PCLKB
000A 8432h	RSCAN	Receive Buffer Register 9AH	RMIDH9	16	16	2 or 3 PCLKB
000A 8434h	RSCAN	Receive Rule Entry Register 12BL	GAFLML12	16	16	2 or 3 PCLKB
000A 8434h	RSCAN	Receive Buffer Register 9BL	RMTS9	16	16	2 or 3 PCLKB
000A 8436h	RSCAN	Receive Rule Entry Register 12BH	GAFLMH12	16	16	2 or 3 PCLKB
000A 8436h	RSCAN	Receive Buffer Register 9BH	RMPTR9	16	16	2 or 3 PCLKB
000A 8438h	RSCAN	Receive Rule Entry Register 12CL	GAFLPL12	16	16	2 or 3 PCLKB
000A 8438h	RSCAN	Receive Buffer Register 9CL	RMDF09	16	16	2 or 3 PCLKB
000A 843Ah	RSCAN	Receive Rule Entry Register 12CH	GAFLPH12	16	16	2 or 3 PCLKB
000A 843Ah	RSCAN	Receive Buffer Register 9CH	RMDF19	16	16	2 or 3 PCLKB
000A 843Ch	RSCAN	Receive Rule Entry Register 13AL	GAFLIDL13	16	16	2 or 3 PCLKB
000A 843Ch	RSCAN	Receive Buffer Register 9DL	RMDF29	16	16	2 or 3 PCLKB
000A 843Eh	RSCAN	Receive Rule Entry Register 13AH	GAFLIDH13	16	16	2 or 3 PCLKB
000A 843Eh	RSCAN	Receive Buffer Register 9DH	RMDF39	16	16	2 or 3 PCLKB
000A 8440h	RSCAN	Receive Rule Entry Register 13BL	GAFLML13	16	16	2 or 3 PCLKB
000A 8440h	RSCAN	Receive Buffer Register 10AL	RMIDL10	16	16	2 or 3 PCLKB
000A 8442h	RSCAN	Receive Rule Entry Register 13BH	GAFLMH13	16	16	2 or 3 PCLKB
000A 8442h	RSCAN	Receive Buffer Register 10AH	RMIDH10	16	16	2 or 3 PCLKB
000A 8444h	RSCAN	Receive Rule Entry Register 13CL	GAFLPL13	16	16	2 or 3 PCLKB
000A 8444h	RSCAN	Receive Buffer Register 10BL	RMTS10	16	16	2 or 3 PCLKB
000A 8446h	RSCAN	Receive Rule Entry Register 13CH	GAFLPH13	16	16	2 or 3 PCLKB
000A 8446h	RSCAN	Receive Buffer Register 10BH	RMPTR10	16	16	2 or 3 PCLKB
000A 8448h	RSCAN	Receive Rule Entry Register 14AL	GAFLIDL14	16	16	2 or 3 PCLKB
000A 8448h	RSCAN	Receive Buffer Register 10CL	RMDF010	16	16	2 or 3 PCLKB
000A 844Ah	RSCAN	Receive Rule Entry Register 14AH	GAFLIDH14	16	16	2 or 3 PCLKB
000A 844Ah	RSCAN	Receive Buffer Register 10CH	RMDF110	16	16	2 or 3 PCLKB
000A 844Ch	RSCAN	Receive Rule Entry Register 14BL	GAFLML14	16	16	2 or 3 PCLKB
000A 844Ch	RSCAN	Receive Buffer Register 10DL	RMDF210	16	16	2 or 3 PCLKB
000A 844Eh	RSCAN	Receive Rule Entry Register 14BH	GAFLMH14	16	16	2 or 3 PCLKB

Table 5.10 DC Characteristics (8)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

The ripple voltage must meet the allowable ripple frequency $f_{r\,(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (2.7 V). When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 5.3 $V_{r\,(VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 5.3 $V_{r\,(VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 5.3 $V_{r\,(VCC)} \leq VCC \times 0.06$
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

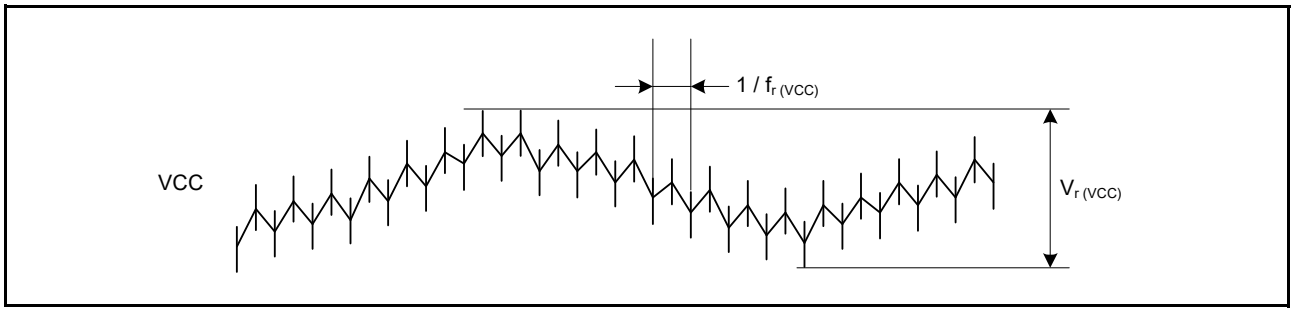


Figure 5.3 Ripple Waveform

Table 5.11 DC Characteristics (9)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C_{VCL}	3.3	4.7	6.1	µF	

Note: The recommended capacitance is 4.7 µF. Variations in connected capacitors should be within the above range.

Table 5.16 Clock Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 5.20
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rise time	t_{Xr}	—	—	5	ns	
EXTAL external clock fall time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2	$t_{MAINOSC}$	—	3	—	ms	Figure 5.21
Main clock oscillation stabilization time (ceramic resonator)*2	$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency	f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	0.5	μs	Figure 5.22
HOCO clock oscillation frequency	f_{HOCO} (32 MHz)	31.52	32	32.48	MHz	T_a = –40 to –20°C
		31.68	32	32.32	MHz	T_a = –20 to +75°C
		31.52	32	32.48	MHz	T_a = +75 to +85°C
	f_{HOCO} (64 MHz)	63.04	64	64.96	MHz	T_a = –40 to –20°C
		63.36	64	64.64	MHz	T_a = –20 to +75°C
		63.04	64	64.96	MHz	T_a = +75 to +85°C
HOCO clock oscillation stabilization time	t_{HOCO} (32 MHz)	—	—	37.1	μs	Figure 5.24
	t_{HOCO} (64 MHz)	—	—	80.6	μs	Figure 5.24
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time	t_{ILOCO}	—	—	50	μs	Figure 5.25
PLL circuit oscillation frequency	f_{PLL}	40	—	80	MHz	
PLL clock oscillation stabilization time	t_{PLL}	—	—	50	μs	Figure 5.26
PLL free-running oscillation frequency	f_{PLLFR}	—	8	—	MHz	

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8 MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

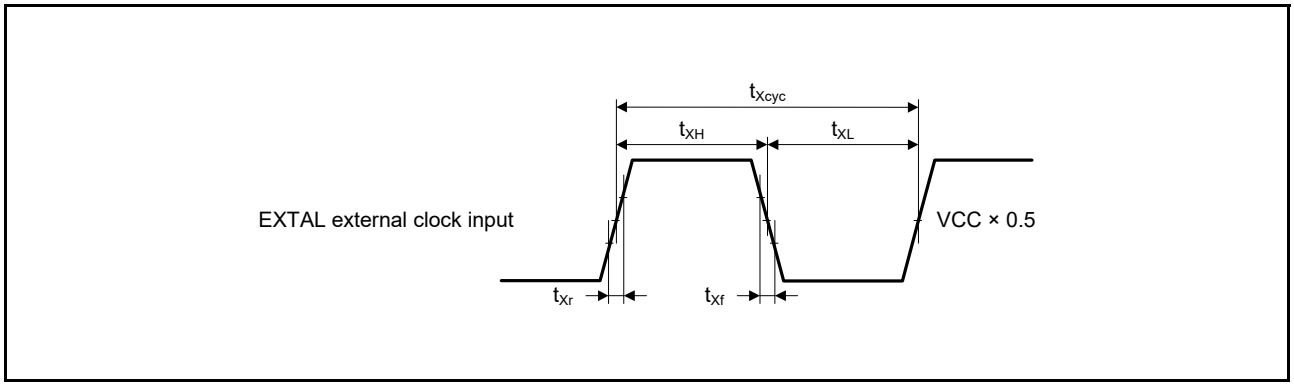


Figure 5.20 EXTAL External Clock Input Timing

5.3.5 Timing of On-Chip Peripheral Modules

Table 5.23 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width			t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.34
MTU3	Input capture input pulse width		Single-edge setting	t_{TICW}	1.5	—	t_{PAcyc}	Figure 5.35
			Both-edge setting		2.5	—		
	Timer clock pulse width		Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{PAcyc}	Figure 5.36
			Both-edge setting		2.5	—		
			Phase counting mode		2.5	—		
POE3	POE# input pulse width			t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.37
GPT	Input capture input pulse width		Single-edge setting	t_{GTICW}	1.5	—	t_{PAcyc}	Figure 5.38
			Both-edge setting		2.5	—		
	External trigger input pulse width		Single-edge setting	t_{GTETW}	1.5	—	t_{PAcyc}	Figure 5.39
			Both-edge setting		2.5	—		
	Timer clock pulse width			t_{GTCKWH}	1.5	—	t_{PAcyc}	Figure 5.40
				t_{GTCKWL}				
TMR	Timer clock pulse width		Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.41
			Both-edge setting		2.5	—		
SCI1, SCI5, SCI6, SCI8, SCI9	Input clock cycle		Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.42
			Clock synchronous		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle		Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	Figure 5.43
			Clock synchronous		4	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	VCC = 4.0 V or above		—	40	ns	
			VCC = 2.7 V or above		—	65	ns	
	Receive data setup time (master)	Clock synchronous	VCC = 4.0 V or above	t_{RXS}	40	—	ns	
			VCC = 2.7 V or above		65	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	
A/D converter	Trigger input pulse width			t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.44
CAC	CACREF input pulse width		$t_{Pcyc} \le t_{cac}$ *2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
			$t_{Pcyc} > t_{cac}$ *2		5 t_{cac} + 6.5 t_{Pcyc}			

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcyc}: PCLKA cycle
Note 2. t_{cac}: CAC count clock source cycle

Table 5.25 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 =AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C, C = 30 pF

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 5.45
		Slave			6	—		
	RSPCK clock high pulse width	Master	VCC = 4.0 V or above	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	VCC = 4.0 V or above	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	VCC = 4.0 V or above	t_{SPCKr}, t_{SPCKf}	—	6	ns	
			VCC = 2.7 V or above		—	10		
		Input			—	0.1	μs/V	
	Data input setup time	Master	VCC = 4.0 V or above	t_{SU}	10	—	ns	Figure 5.46 to Figure 5.49
			VCC = 2.7 V or above		26	—		
		Slave			20	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	0	—		
	SSL setup time	Master		t_{LEAD}	$–30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			6	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$–30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			6	—	t_{Pcyc}	
	Data output delay time	Master	VCC = 4.0 V or above	t_{OD}	—	10	ns	
			VCC = 2.7 V or above		—	14		
		Slave			—	65		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$6 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	10	ns	
		Input			—	1	μs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	10	ns	
		Input			—	1	μs	
	Slave access time			t_{SA}	—	6	t_{Pcyc}	Figure 5.48, Figure 5.49
	Slave output release time			t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

Table 5.28 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 5.50
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	1000	—	ns	
	STOP condition setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 5.50
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	300	—	ns	
	STOP condition setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle

Note 2. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit is 1.

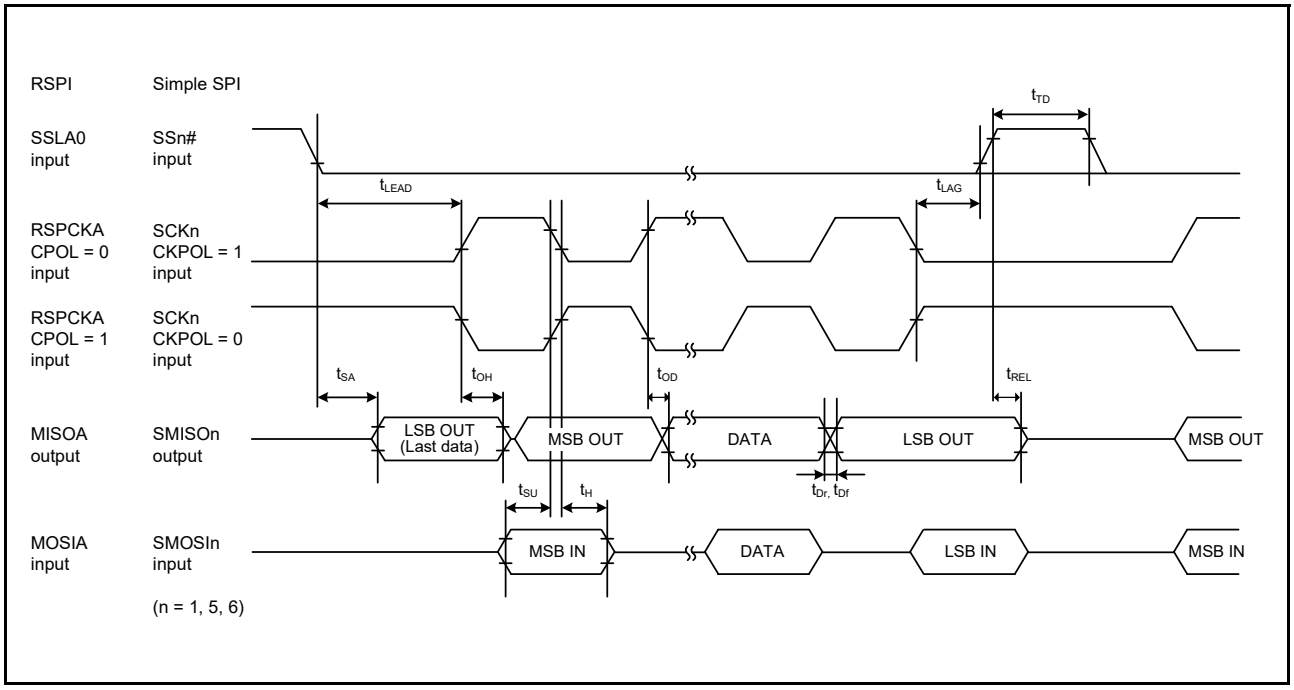
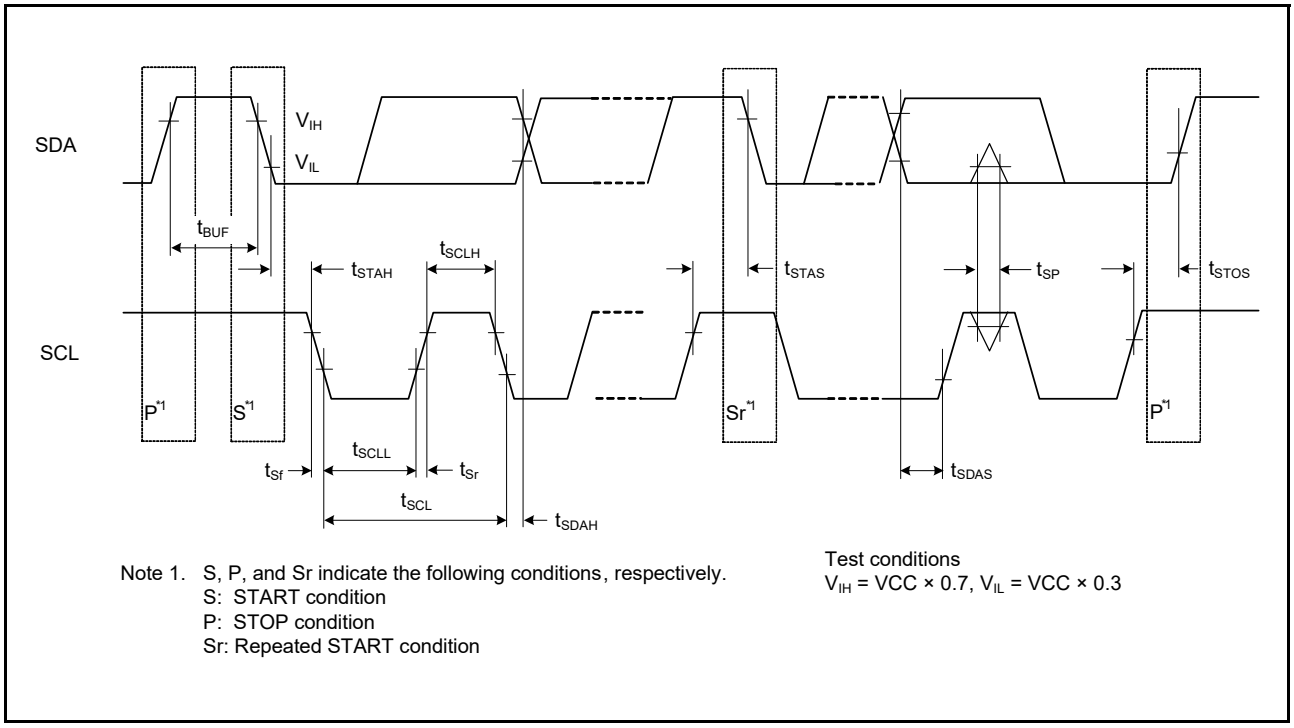


Figure 5.49 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3

Figure 5.50 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

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