Renesas Electronics America Inc - R5F524UBADFP#30 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

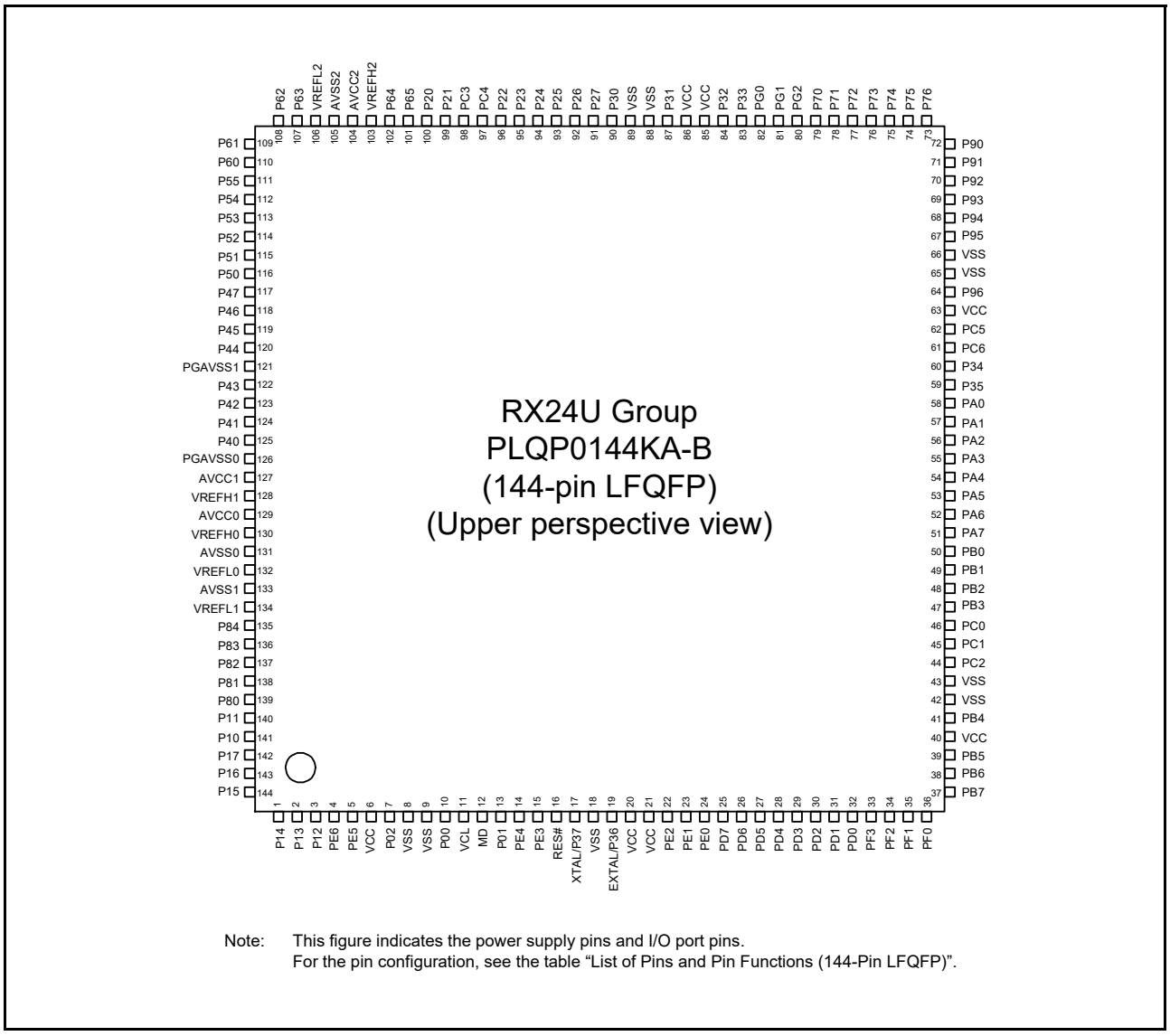
Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524ubadfp-30

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX24U Group	
		144 Pins	100 Pins
Memory	ROM	512 Kbytes	
	RAM	32 Kbytes	
	E2 Data Flash	8 Kbytes	
Interrupts	External interrupts	NMI, IRQ0 to IRQ7	
DTC	Data transfer controller (DTCa)	Available	
Timers	Multi-function timer pulse unit 3 (MTU3d)	9 channels	
	General PWM timer (GPTB)	4 channels	
	Port output enable 3 (POE3A)	POE0#, POE4#, POE8#, POE10#, POE11#, POE12#	
	8-bit timer (TMR)	2 channels × 4 units	
	Compare match timer (CMT)	2 channels × 2 units	
	Independent watchdog timer (IWDTa)	Available	
Communication functions	Serial communications interfaces (SCIg) [including simple I^2C and simple SPI]	6 channels (SCI1, 5, 6, 8, 9, 11)	4 channels (SCI1, 5, 6, 11)
	I^2C bus interface (RIICa)	1 channel	
	Serial peripheral interface (RSPIb)	1 channel	
	CAN module (RSCAN)	1 channel	
12-bit A/D converter (including high-precision channels) (S12ADF)		5 channels × 2 units, 12 channels × 1 unit (4 channels × 2 units, 12 channels × 1 unit)	5 channels × 2 units, 10 channels × 1 unit (4 channels × 2 units, 10 channels × 1 unit)
	3 channels simultaneous sampling function	3 channels/unit 1	
	Programmable gain amplifier	1 channel/unit 0, 3 channels/unit 1	
Comparator C (CMPC)		4 channels	
D/A converter (DAa)		2 channels	
CRC calculator (CRC)		Available	
Packages		144-pin LFQFP	100-pin LFQFP

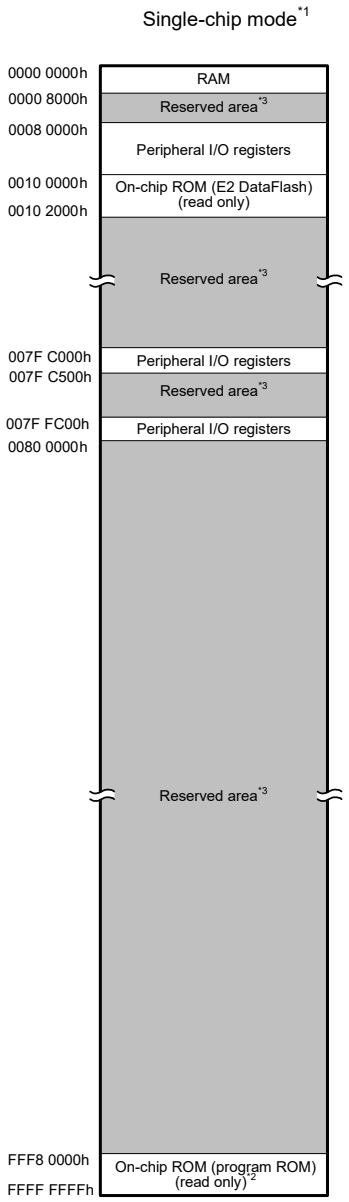
1.5 Pin Assignments

Figure 1.3 and Figure 1.4 show the pin assignments. Table 1.5 and Table 1.6 show the lists of pins and pin functions.



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (144-Pin LFQFP)”.

Figure 1.3 Pin Assignments of the 144-Pin LFQFP



Note 1. The address space in boot mode is the same as the address space in single-chip mode.

Note 2. The capacity of ROM differs depending on the products.

ROM (bytes)		RAM (bytes)		E2 DataFlash (bytes)	
Capacity	**Address**	**Capacity**	**Address**	**Capacity**	**Address**
512 K	FFF8 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh	8 K	0010 0000h to 0010 1FFFh
384 K	FFFA 0000h to FFFF FFFFh				
256 K	FFFC 0000h to FFFF FFFFh				

Note: See Table 1.3 List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map in Each Operating Mode

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK
0008 0031h	SYSTEM	Memory Wait Cycle Setting Register	MEMWAIT	8	8	3 ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK
0008 0037h	SYSTEM	High-Speed On-Chip Oscillator Control Register 2	HOCOCR2	8	8	3 ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK
0008 00A5h	SYSTEM	High-Speed On-Chip Oscillator Wait Control Register	HOCOWTCR	8	8	3 ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK
0008 1000h	FLASH	ROM Cache Enable Register	ROMCE	16	16	3 ICLK
0008 1004h	FLASH	ROM Cache Invalidate Register	ROMCIV	16	16	3 ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK

Table 4.1 List of I/O Registers (Address Order) (19/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 C068h	PORT8	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C069h	PORT9	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C06Fh	PORTF	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C070h	PORTG	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C080h	PORT0	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C08Eh	PORT7	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C08Fh	PORT7	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C090h	PORT8	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C091h	PORT8	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C092h	PORT9	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C093h	PORT9	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C09Bh	PORTD	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C09Eh	PORTF	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C0A0h	PORTG	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C4h	PORT4	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C6h	PORT6	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C7h	PORT7	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C8h	PORT8	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C9h	PORT9	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CCh	PORTC	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CDh	PORTD	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CFh	PORTF	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0D0h	PORTG	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0E0h	PORT0	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (20/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E3h	PORT3	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E7h	PORT7	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E8h	PORT8	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E9h	PORT9	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0ECh	PORTC	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EFh	PORTF	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0F0h	PORTG	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 or 3 PCLKB
0008 C140h	MPC	P00 Pin Function Control Register	P00PFS	8	8	2 or 3 PCLKB
0008 C141h	MPC	P01 Pin Function Control Register	P01PFS	8	8	2 or 3 PCLKB
0008 C142h	MPC	P02 Pin Function Control Register	P02PFS	8	8	2 or 3 PCLKB
0008 C148h	MPC	P10 Pin Function Control Register	P10PFS	8	8	2 or 3 PCLKB
0008 C149h	MPC	P11 Pin Function Control Register	P11PFS	8	8	2 or 3 PCLKB
0008 C14Ah	MPC	P12 Pin Function Control Register	P12PFS	8	8	2 or 3 PCLKB
0008 C14Bh	MPC	P13 Pin Function Control Register	P13PFS	8	8	2 or 3 PCLKB
0008 C14Ch	MPC	P14 Pin Function Control Register	P14PFS	8	8	2 or 3 PCLKB
0008 C14Dh	MPC	P15 Pin Function Control Register	P15PFS	8	8	2 or 3 PCLKB
0008 C14Eh	MPC	P16 Pin Function Control Register	P16PFS	8	8	2 or 3 PCLKB
0008 C14Fh	MPC	P17 Pin Function Control Register	P17PFS	8	8	2 or 3 PCLKB
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2 or 3 PCLKB
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2 or 3 PCLKB
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2 or 3 PCLKB
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2 or 3 PCLKB
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2 or 3 PCLKB
0008 C155h	MPC	P25 Pin Function Control Register	P25PFS	8	8	2 or 3 PCLKB
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2 or 3 PCLKB
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2 or 3 PCLKB
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2 or 3 PCLKB
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2 or 3 PCLKB
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2 or 3 PCLKB
0008 C15Bh	MPC	P33 Pin Function Control Register	P33PFS	8	8	2 or 3 PCLKB
0008 C15Ch	MPC	P34 Pin Function Control Register	P34PFS	8	8	2 or 3 PCLKB
0008 C15Dh	MPC	P35 Pin Function Control Register	P35PFS	8	8	2 or 3 PCLKB
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2 or 3 PCLKB
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2 or 3 PCLKB
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2 or 3 PCLKB
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2 or 3 PCLKB
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2 or 3 PCLKB
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2 or 3 PCLKB
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2 or 3 PCLKB
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2 or 3 PCLKB
0008 C168h	MPC	P50 Pin Function Control Register	P50PFS	8	8	2 or 3 PCLKB
0008 C169h	MPC	P51 Pin Function Control Register	P51PFS	8	8	2 or 3 PCLKB
0008 C16Ah	MPC	P52 Pin Function Control Register	P52PFS	8	8	2 or 3 PCLKB
0008 C16Bh	MPC	P53 Pin Function Control Register	P53PFS	8	8	2 or 3 PCLKB
0008 C16Ch	MPC	P54 Pin Function Control Register	P54PFS	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (21/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 C16Dh	MPC	P55 Pin Function Control Register	P55PFS	8	8	2 or 3 PCLKB
0008 C170h	MPC	P60 Pin Function Control Register	P60PFS	8	8	2 or 3 PCLKB
0008 C171h	MPC	P61 Pin Function Control Register	P61PFS	8	8	2 or 3 PCLKB
0008 C172h	MPC	P62 Pin Function Control Register	P62PFS	8	8	2 or 3 PCLKB
0008 C173h	MPC	P63 Pin Function Control Register	P63PFS	8	8	2 or 3 PCLKB
0008 C174h	MPC	P64 Pin Function Control Register	P64PFS	8	8	2 or 3 PCLKB
0008 C175h	MPC	P65 Pin Function Control Register	P65PFS	8	8	2 or 3 PCLKB
0008 C178h	MPC	P70 Pin Function Control Register	P70PFS	8	8	2 or 3 PCLKB
0008 C179h	MPC	P71 Pin Function Control Register	P71PFS	8	8	2 or 3 PCLKB
0008 C17Ah	MPC	P72 Pin Function Control Register	P72PFS	8	8	2 or 3 PCLKB
0008 C17Bh	MPC	P73 Pin Function Control Register	P73PFS	8	8	2 or 3 PCLKB
0008 C17Ch	MPC	P74 Pin Function Control Register	P74PFS	8	8	2 or 3 PCLKB
0008 C17Dh	MPC	P75 Pin Function Control Register	P75PFS	8	8	2 or 3 PCLKB
0008 C17Eh	MPC	P76 Pin Function Control Register	P76PFS	8	8	2 or 3 PCLKB
0008 C180h	MPC	P80 Pin Function Control Register	P80PFS	8	8	2 or 3 PCLKB
0008 C181h	MPC	P81 Pin Function Control Register	P81PFS	8	8	2 or 3 PCLKB
0008 C182h	MPC	P82 Pin Function Control Register	P82PFS	8	8	2 or 3 PCLKB
0008 C183h	MPC	P83 Pin Function Control Register	P83PFS	8	8	2 or 3 PCLKB
0008 C184h	MPC	P84 Pin Function Control Register	P84PFS	8	8	2 or 3 PCLKB
0008 C188h	MPC	P90 Pin Function Control Register	P90PFS	8	8	2 or 3 PCLKB
0008 C189h	MPC	P91 Pin Function Control Register	P91PFS	8	8	2 or 3 PCLKB
0008 C18Ah	MPC	P92 Pin Function Control Register	P92PFS	8	8	2 or 3 PCLKB
0008 C18Bh	MPC	P93 Pin Function Control Register	P93PFS	8	8	2 or 3 PCLKB
0008 C18Ch	MPC	P94 Pin Function Control Register	P94PFS	8	8	2 or 3 PCLKB
0008 C18Dh	MPC	P95 Pin Function Control Register	P95PFS	8	8	2 or 3 PCLKB
0008 C18Eh	MPC	P96 Pin Function Control Register	P96PFS	8	8	2 or 3 PCLKB
0008 C190h	MPC	PA0 Pin Function Control Register	PA0PFS	8	8	2 or 3 PCLKB
0008 C191h	MPC	PA1 Pin Function Control Register	PA1PFS	8	8	2 or 3 PCLKB
0008 C192h	MPC	PA2 Pin Function Control Register	PA2PFS	8	8	2 or 3 PCLKB
0008 C193h	MPC	PA3 Pin Function Control Register	PA3PFS	8	8	2 or 3 PCLKB
0008 C194h	MPC	PA4 Pin Function Control Register	PA4PFS	8	8	2 or 3 PCLKB
0008 C195h	MPC	PA5 Pin Function Control Register	PA5PFS	8	8	2 or 3 PCLKB
0008 C196h	MPC	PA6 Pin Function Control Register	PA6PFS	8	8	2 or 3 PCLKB
0008 C197h	MPC	PA7 Pin Function Control Register	PA7PFS	8	8	2 or 3 PCLKB
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2 or 3 PCLKB
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2 or 3 PCLKB
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2 or 3 PCLKB
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2 or 3 PCLKB
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2 or 3 PCLKB
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2 or 3 PCLKB
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2 or 3 PCLKB
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2 or 3 PCLKB
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2 or 3 PCLKB
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2 or 3 PCLKB
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2 or 3 PCLKB
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2 or 3 PCLKB
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2 or 3 PCLKB
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2 or 3 PCLKB
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2 or 3 PCLKB
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2 or 3 PCLKB
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2 or 3 PCLKB
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (27/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000A 841Ah	RSCAN	Receive Buffer Register 7CH	RMDF17	16	16	2 or 3 PCLKB
000A 841Ch	RSCAN	Receive Rule Entry Register 10BL	GAFLML10	16	16	2 or 3 PCLKB
000A 841Ch	RSCAN	Receive Buffer Register 7DL	RMDF27	16	16	2 or 3 PCLKB
000A 841Eh	RSCAN	Receive Rule Entry Register 10BH	GAFLMH10	16	16	2 or 3 PCLKB
000A 841Eh	RSCAN	Receive Buffer Register 7DH	RMDF37	16	16	2 or 3 PCLKB
000A 8420h	RSCAN	Receive Rule Entry Register 10CL	GAFLPL10	16	16	2 or 3 PCLKB
000A 8420h	RSCAN	Receive Buffer Register 8AL	RMIDL8	16	16	2 or 3 PCLKB
000A 8422h	RSCAN	Receive Rule Entry Register 10CH	GAFLPH10	16	16	2 or 3 PCLKB
000A 8422h	RSCAN	Receive Buffer Register 8AH	RMIDH8	16	16	2 or 3 PCLKB
000A 8424h	RSCAN	Receive Rule Entry Register 11AL	GAFLIDL11	16	16	2 or 3 PCLKB
000A 8424h	RSCAN	Receive Buffer Register 8BL	RMTS8	16	16	2 or 3 PCLKB
000A 8426h	RSCAN	Receive Rule Entry Register 11AH	GAFLIDH11	16	16	2 or 3 PCLKB
000A 8426h	RSCAN	Receive Buffer Register 8BH	RMPTR8	16	16	2 or 3 PCLKB
000A 8428h	RSCAN	Receive Rule Entry Register 11BL	GAFLML11	16	16	2 or 3 PCLKB
000A 8428h	RSCAN	Receive Buffer Register 8CL	RMDF08	16	16	2 or 3 PCLKB
000A 842Ah	RSCAN	Receive Rule Entry Register 11BH	GAFLMH11	16	16	2 or 3 PCLKB
000A 842Ah	RSCAN	Receive Buffer Register 8CH	RMDF18	16	16	2 or 3 PCLKB
000A 842Ch	RSCAN	Receive Rule Entry Register 11CL	GAFLPL11	16	16	2 or 3 PCLKB
000A 842Ch	RSCAN	Receive Buffer Register 8DL	RMDF28	16	16	2 or 3 PCLKB
000A 842Eh	RSCAN	Receive Rule Entry Register 11CH	GAFLPH11	16	16	2 or 3 PCLKB
000A 842Eh	RSCAN	Receive Buffer Register 8DH	RMDF38	16	16	2 or 3 PCLKB
000A 8430h	RSCAN	Receive Rule Entry Register 12AL	GAFLIDL12	16	16	2 or 3 PCLKB
000A 8430h	RSCAN	Receive Buffer Register 9AL	RMIDL9	16	16	2 or 3 PCLKB
000A 8432h	RSCAN	Receive Rule Entry Register 12AH	GAFLIDH12	16	16	2 or 3 PCLKB
000A 8432h	RSCAN	Receive Buffer Register 9AH	RMIDH9	16	16	2 or 3 PCLKB
000A 8434h	RSCAN	Receive Rule Entry Register 12BL	GAFLML12	16	16	2 or 3 PCLKB
000A 8434h	RSCAN	Receive Buffer Register 9BL	RMTS9	16	16	2 or 3 PCLKB
000A 8436h	RSCAN	Receive Rule Entry Register 12BH	GAFLMH12	16	16	2 or 3 PCLKB
000A 8436h	RSCAN	Receive Buffer Register 9BH	RMPTR9	16	16	2 or 3 PCLKB
000A 8438h	RSCAN	Receive Rule Entry Register 12CL	GAFLPL12	16	16	2 or 3 PCLKB
000A 8438h	RSCAN	Receive Buffer Register 9CL	RMDF09	16	16	2 or 3 PCLKB
000A 843Ah	RSCAN	Receive Rule Entry Register 12CH	GAFLPH12	16	16	2 or 3 PCLKB
000A 843Ah	RSCAN	Receive Buffer Register 9CH	RMDF19	16	16	2 or 3 PCLKB
000A 843Ch	RSCAN	Receive Rule Entry Register 13AL	GAFLIDL13	16	16	2 or 3 PCLKB
000A 843Ch	RSCAN	Receive Buffer Register 9DL	RMDF29	16	16	2 or 3 PCLKB
000A 843Eh	RSCAN	Receive Rule Entry Register 13AH	GAFLIDH13	16	16	2 or 3 PCLKB
000A 843Eh	RSCAN	Receive Buffer Register 9DH	RMDF39	16	16	2 or 3 PCLKB
000A 8440h	RSCAN	Receive Rule Entry Register 13BL	GAFLML13	16	16	2 or 3 PCLKB
000A 8440h	RSCAN	Receive Buffer Register 10AL	RMIDL10	16	16	2 or 3 PCLKB
000A 8442h	RSCAN	Receive Rule Entry Register 13BH	GAFLMH13	16	16	2 or 3 PCLKB
000A 8442h	RSCAN	Receive Buffer Register 10AH	RMIDH10	16	16	2 or 3 PCLKB
000A 8444h	RSCAN	Receive Rule Entry Register 13CL	GAFLPL13	16	16	2 or 3 PCLKB
000A 8444h	RSCAN	Receive Buffer Register 10BL	RMTS10	16	16	2 or 3 PCLKB
000A 8446h	RSCAN	Receive Rule Entry Register 13CH	GAFLPH13	16	16	2 or 3 PCLKB
000A 8446h	RSCAN	Receive Buffer Register 10BH	RMPTR10	16	16	2 or 3 PCLKB
000A 8448h	RSCAN	Receive Rule Entry Register 14AL	GAFLIDL14	16	16	2 or 3 PCLKB
000A 8448h	RSCAN	Receive Buffer Register 10CL	RMDF010	16	16	2 or 3 PCLKB
000A 844Ah	RSCAN	Receive Rule Entry Register 14AH	GAFLIDH14	16	16	2 or 3 PCLKB
000A 844Ah	RSCAN	Receive Buffer Register 10CH	RMDF110	16	16	2 or 3 PCLKB
000A 844Ch	RSCAN	Receive Rule Entry Register 14BL	GAFLML14	16	16	2 or 3 PCLKB
000A 844Ch	RSCAN	Receive Buffer Register 10DL	RMDF210	16	16	2 or 3 PCLKB
000A 844Eh	RSCAN	Receive Rule Entry Register 14BH	GAFLMH14	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (31/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000A 8638h	RSCAN	RAM Test Register 92	RPGACC92	16	16	2 or 3 PCLKB
000A 863Ah	RSCAN0	Transmit Buffer Register 3CH	TMDF13	16	16	2 or 3 PCLKB
000A 863Ah	RSCAN	RAM Test Register 93	RPGACC93	16	16	2 or 3 PCLKB
000A 863Ch	RSCAN0	Transmit Buffer Register 3DL	TMDF23	16	16	2 or 3 PCLKB
000A 863Ch	RSCAN	RAM Test Register 94	RPGACC94	16	16	2 or 3 PCLKB
000A 863Eh	RSCAN0	Transmit Buffer Register 3DH	TMDF33	16	16	2 or 3 PCLKB
000A 863Eh	RSCAN	RAM Test Register 95	RPGACC95	16	16	2 or 3 PCLKB
000A 8640h to 000A 867Eh	RSCAN	RAM Test Register 96 to 127	RPGACC96 to 127	16	16	2 or 3 PCLKB
000A 8680h	RSCAN0	Transmit History Buffer Access Register	THLACC0	16	16	2 or 3 PCLKB
000C 1200h	MTU3	Timer Control Register	TCR	8	8, 16, 32	4 or 5 PCLKA
000C 1201h	MTU4	Timer Control Register	TCR	8	8	4 or 5 PCLKA
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8, 16	4 or 5 PCLKA
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8, 16, 32	4 or 5 PCLKA
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8, 16	4 or 5 PCLKA
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8, 16	4 or 5 PCLKA
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	4 or 5 PCLKA
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	4 or 5 PCLKA
000C 120Dh	MTU	Timer Gate Control Register	TGCRA	8	8	4 or 5 PCLKA
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8, 16	4 or 5 PCLKA
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	4 or 5 PCLKA
000C 1210h	MTU3	Timer Counter	TCNT	16	16, 32	4 or 5 PCLKA
000C 1212h	MTU4	Timer Counter	TCNT	16	16	4 or 5 PCLKA
000C 1214h	MTU	Timer Period Data Register A	TCDRA	16	16, 32	4 or 5 PCLKA
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	4 or 5 PCLKA
000C 1218h	MTU3	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	4 or 5 PCLKA
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	4 or 5 PCLKA
000C 1220h	MTU	Timer Subcounters A	TCNTSA	16	16, 32	4 or 5 PCLKA
000C 1222h	MTU	Timer Period Buffer Register A	TCBRA	16	16	4 or 5 PCLKA
000C 1224h	MTU3	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	4 or 5 PCLKA
000C 1228h	MTU4	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA
000C 122Ah	MTU4	Timer General Register D	TGRD	16	16	4 or 5 PCLKA
000C 122Ch	MTU3	Timer Status Register	TSR	8	8, 16	4 or 5 PCLKA
000C 122Dh	MTU4	Timer Status Register	TSR	8	8	4 or 5 PCLKA
000C 1230h	MTU	Timer Interrupt Skipping Set Register 1A	TITCR1A	8	8, 16	4 or 5 PCLKA
000C 1231h	MTU	Timer Interrupt Skipping Counters 1A	TITCNT1A	8	8	4 or 5 PCLKA
000C 1232h	MTU	Timer Buffer Transfer Set Register A	TBTERA	8	8	4 or 5 PCLKA
000C 1234h	MTU	Timer Dead Time Enable Register A	TDERA	8	8	4 or 5 PCLKA
000C 1236h	MTU	Timer Output Level Buffer Register A	TOLBRA	8	8	4 or 5 PCLKA
000C 1238h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8, 16	4 or 5 PCLKA
000C 1239h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4 or 5 PCLKA
000C 123Ah	MTU	Timer Interrupt Skipping Mode Register A	TITMRA	8	8	4 or 5 PCLKA
000C 123Bh	MTU	Timer Interrupt Skipping Set Register 2A	TITCR2A	8	8	4 or 5 PCLKA
000C 123Ch	MTU	Timer Interrupt Skipping Counters 2A	TITCNT2A	8	8	4 or 5 PCLKA
000C 1240h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	4 or 5 PCLKA
000C 1244h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16, 32	4 or 5 PCLKA

Table 5.8 DC Characteristics (6)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0V, T_a = –40 to +85°C

Item			Symbol	Min.	Typ.*2	Max.	Unit	Test Conditions
Analog power supply current	A/D unit 0	During A/D conversion (programmable gain amplifier in use)	I_{AVCC}	—	1.5	2.5	mA	
		During A/D conversion (programmable gain amplifier not in use)		—	1.0	1.8		
	A/D unit 1	During A/D conversion (sample-and-hold circuits in use, programmable gain amplifier in use)		—	4.6	6.9		
		During A/D conversion (sample-and-hold circuits in use, programmable gain amplifier not in use)		—	3.1	4.8		
		During A/D conversion (sample-and-hold circuits not in use, programmable gain amplifier in use)		—	2.5	3.9		
		During A/D conversion (sample-and-hold circuits not in use, programmable gain amplifier not in use)		—	1.0	1.8		
	A/D unit 2			—	1.0	1.8		
	During D/A conversion (per 1 channel)*1			—	0.7	1.0		
	Waiting for A/D or D/A conversion (all units)			—	—	2.2	μA	
Reference power supply current	During A/D conversion (at high-speed conversion per 1 unit)		I_{REFH}	—	10.0	20.0	μA	
	Waiting for A/D conversion (all units)			—	—	180.0	nA	
Comparator C operating current*3	Comparator enabled		I_{CMP}	—	40.0	60.0	μA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.
Note 2. When VCC =AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = 5 V.
Note 3. Current consumed only by the comparator C module.

Table 5.9 DC Characteristics (7)

Conditions: VCC = 0 V to AVCC0, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = 0 V to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup	SrVCC	0.02	—	20	ms/V	
	Voltage monitoring 0 reset enabled at startup*1, *2		0.02	—	—		

Note 1. When OFS1.LVDAS = 0.
Note 2. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

5.2.4 RIIC Pin Output Characteristics

Figure 5.16 to Figure 5.19 show the output characteristics of the RIIC pin.

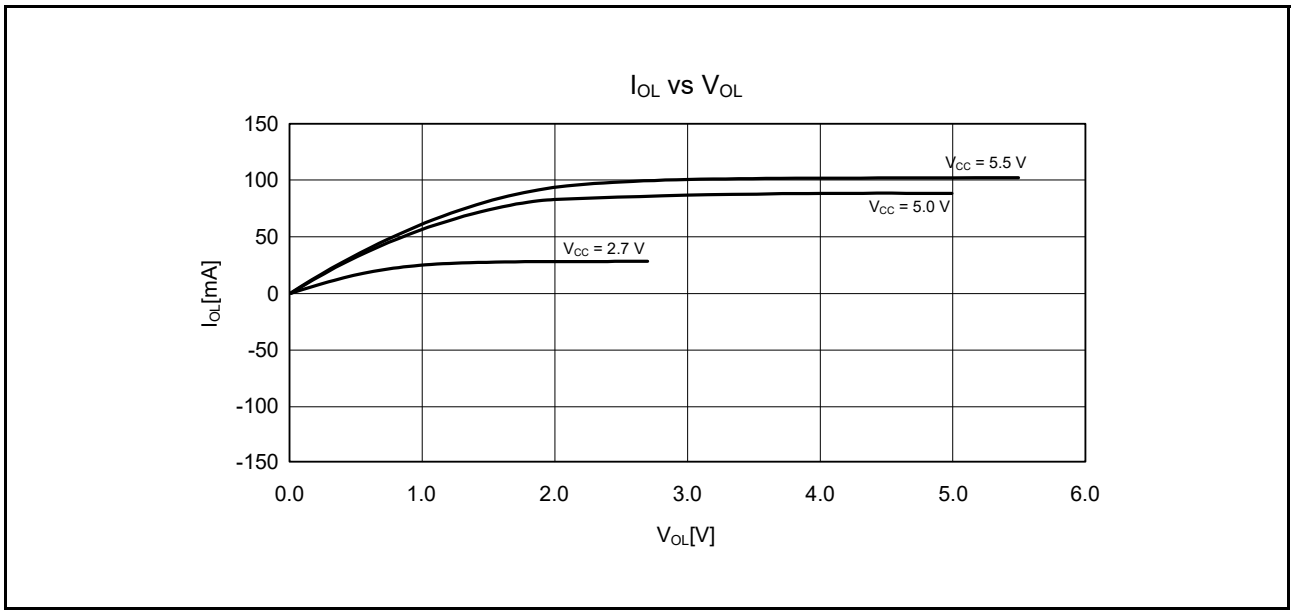


Figure 5.16 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

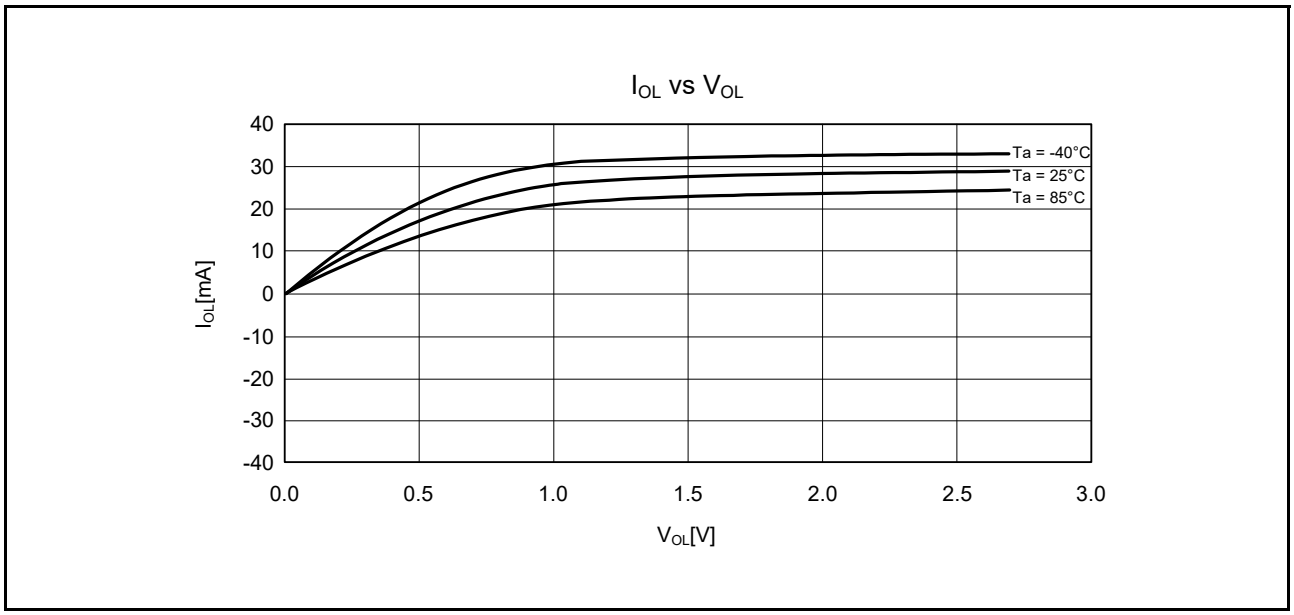


Figure 5.17 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

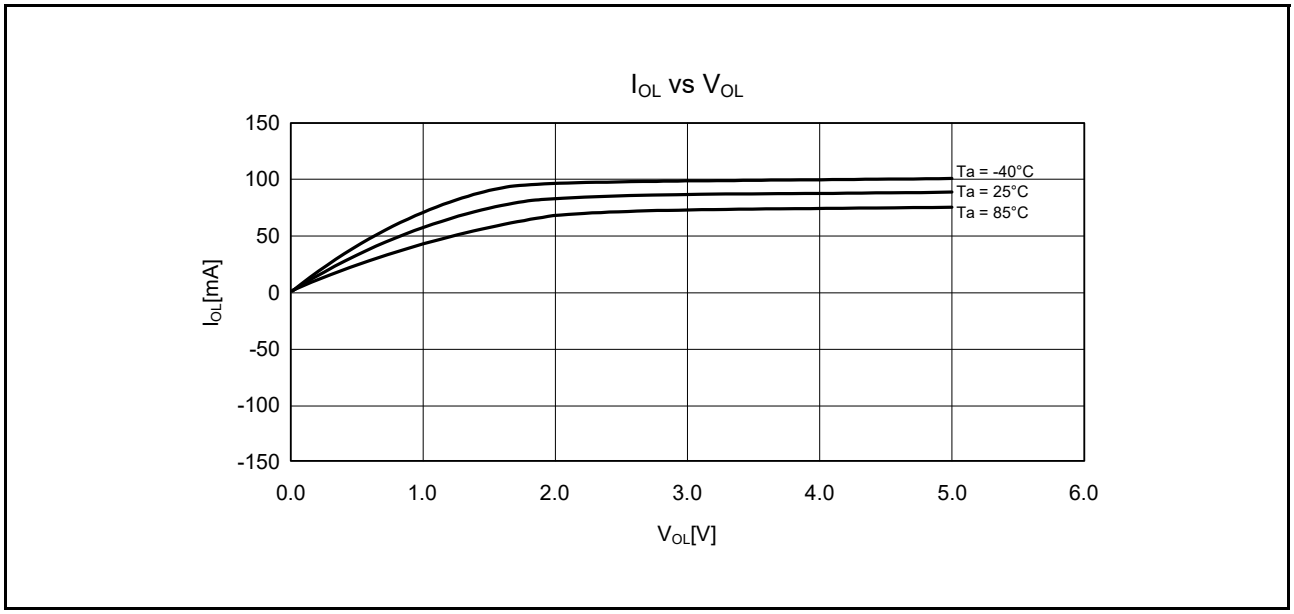


Figure 5.18 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.0 V (Reference Data)

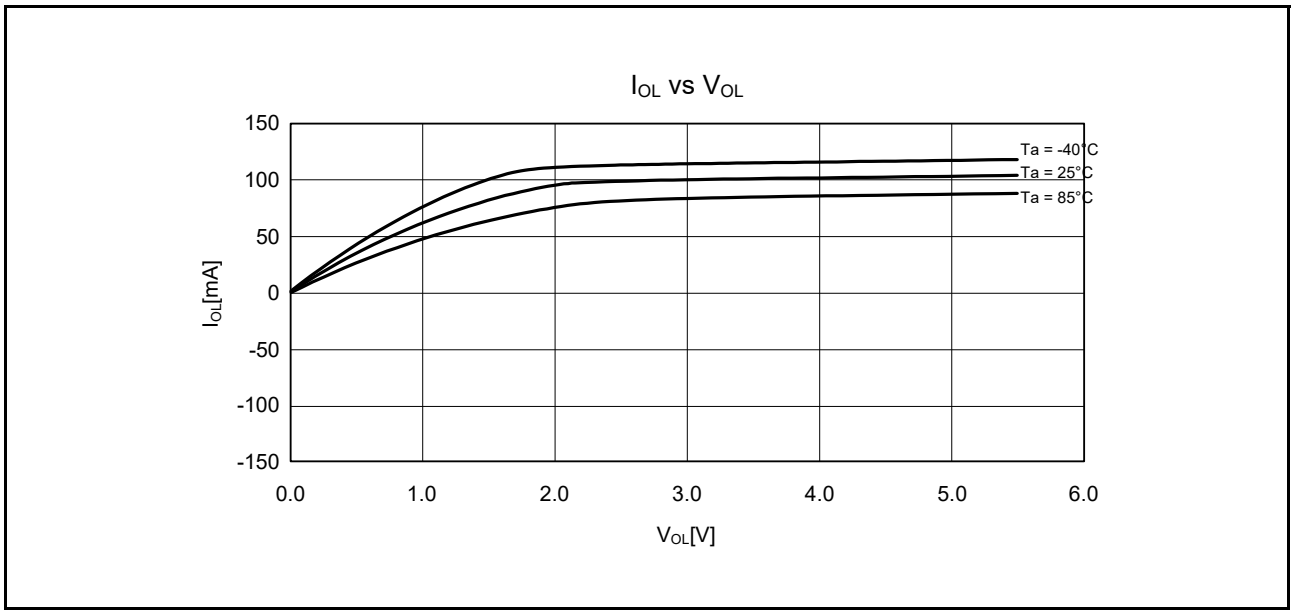


Figure 5.19 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)

5.3.2 Reset Timing

Table 5.17 Reset Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 5.27
	Other than above	t_{RESW}	30	—	—	µs	Figure 5.28
Wait time after RES# cancellation (at power-on)		t_{RESWT}	—	27.5	—	ms	Figure 5.27
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	114	—	µs	Figure 5.28
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 5.29
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*1		t_{RESW2}	—	300	—	µs	
Wait time after software reset cancellation		t_{RESW2}	—	168	—	µs	

Note 1. When IWDTCR.CKS[3:0] = 0000b.

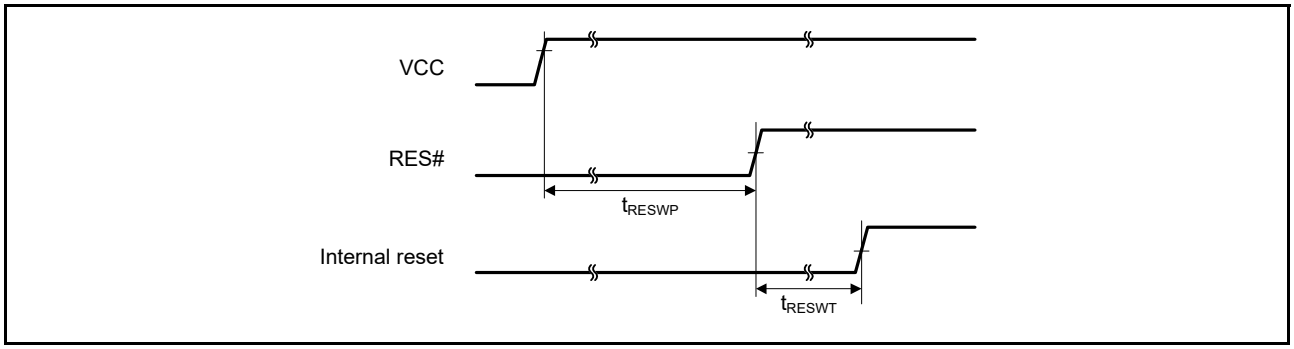


Figure 5.27 Reset Input Timing at Power-On

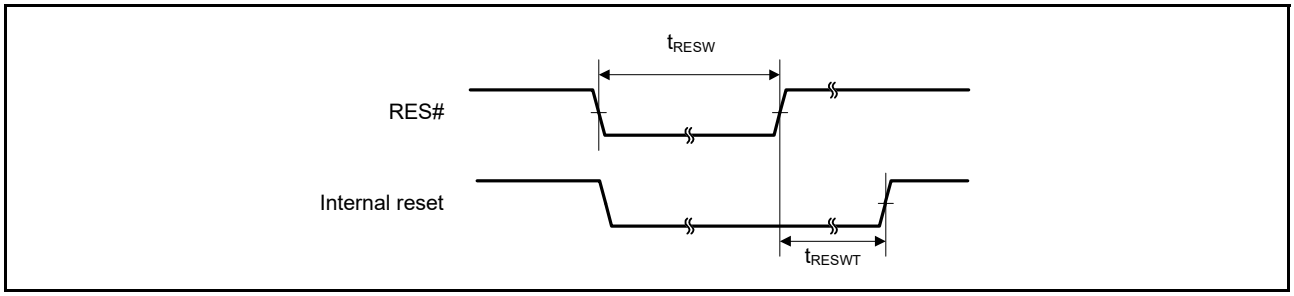


Figure 5.28 Reset Input Timing (1)

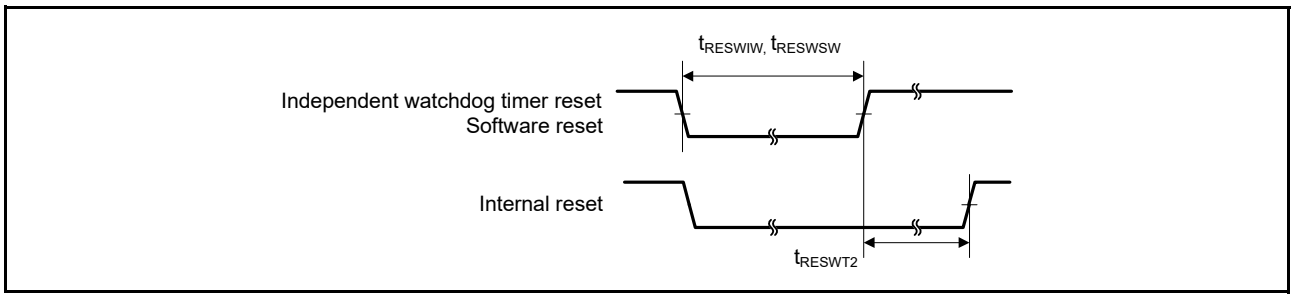


Figure 5.29 Reset Input Timing (2)

5.3.4 Control Signal Timing

Table 5.22 Control Signal Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	$t_{NMICK} \times 3 \le 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	$t_{IRQCK} \times 3 \le 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

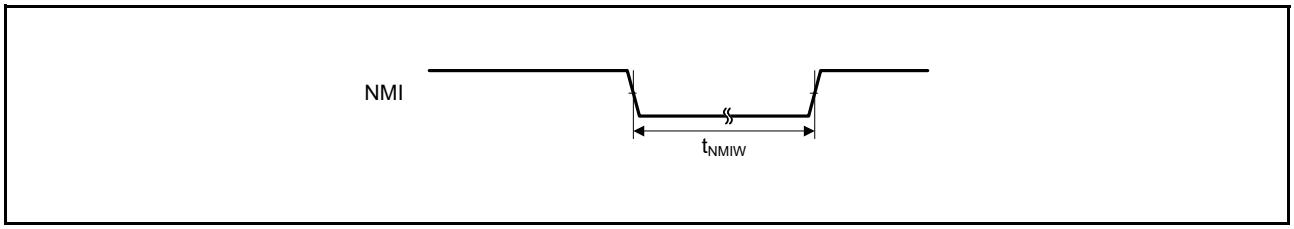


Figure 5.32 NMI Interrupt Input Timing

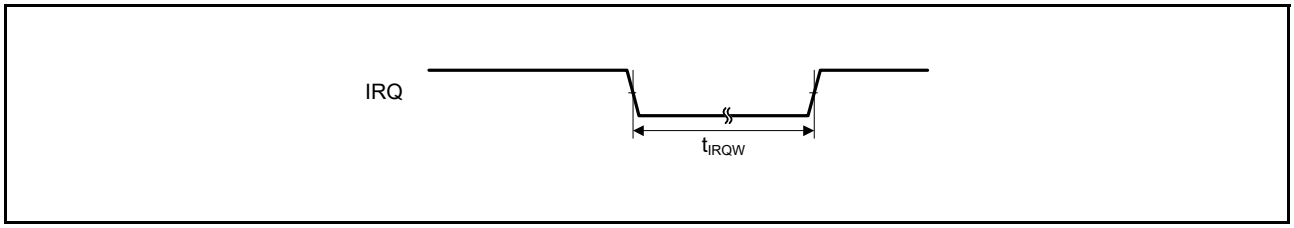


Figure 5.33 IRQ Interrupt Input Timing

Table 5.25 Timing of On-Chip Peripheral Modules (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 =AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C, C = 30 pF

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 5.45
		Slave			6	—		
	RSPCK clock high pulse width	Master	VCC = 4.0 V or above	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	VCC = 4.0 V or above	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	VCC = 4.0 V or above	t_{SPCKr}, t_{SPCKf}	—	6	ns	
			VCC = 2.7 V or above		—	10		
		Input			—	0.1	μs/V	
	Data input setup time	Master	VCC = 4.0 V or above	t_{SU}	10	—	ns	Figure 5.46 to Figure 5.49
			VCC = 2.7 V or above		26	—		
		Slave			20	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	0	—		
	SSL setup time	Master		t_{LEAD}	$–30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			6	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$–30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			6	—	t_{Pcyc}	
	Data output delay time	Master	VCC = 4.0 V or above	t_{OD}	—	10	ns	
			VCC = 2.7 V or above		—	14		
		Slave			—	65		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$6 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	10	ns	
		Input			—	1	μs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	10	ns	
		Input			—	1	μs	
	Slave access time			t_{SA}	—	6	t_{Pcyc}	Figure 5.48, Figure 5.49
	Slave output release time			t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

Table 5.27 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C, C = 30 pF

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI (SCI11)	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.45
	SCK clock cycle input (slave)			6	—	t_{Pcyc}	
	SCK clock output frequency (master)		f_{SPcyc}	—	10	MHz	
	SCK clock input frequency (slave)			—	6.67	MHz	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	VCC = 4.0 V or above	t_{SU}	40	—	ns	Figure 5.46, Figure 5.47
		VCC = 2.7 V or above		65	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	VCC = 4.0 V or above		—	40		
		VCC = 2.7 V or above		—	65		
	Data output hold time	Master	t_{OH}	–10	—	ns	
		Slave		–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	PCLKA ≤ 40MHz	t_{SA}	—	6	t_{PAcyc}	Figure 5.48, Figure 5.49
		PCLKA > 40MHz		—	12	t_{PAcyc}	
	Slave output release time	PCLKA ≤ 40MHz	t_{REL}	—	6	t_{PAcyc}	
		PCLKA > 40MHz		—	12	t_{PAcyc}	

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcyc}: PCLKA cycle

Table 5.28 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 5.50
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	1000	—	ns	
	STOP condition setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 5.50
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	300	—	ns	
	STOP condition setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note 1. t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle

Note 2. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit is 1.

Table 5.29 Timing of On-Chip Peripheral Modules (7)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = 2.7 V to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple I²C (Standard mode) (SCI1, SCI5, SCI6, SCI8, SCI9, SCI11)	SDA rise time	t_{Sr}	—	1000	ns	Figure 5.50
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}*1	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	
Simple I²C (Fast mode) (SCI, SCI5, SCI6, SCI8, SCI9, SCI11)	SDA rise time	t_{Sr}	—	300	ns	Figure 5.50
	SDA fall time	t_{Sf}	—	300	ns	
	SDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}*1	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note 1. t_{Pcyc}: PCLKB cycle
Note 2. C_b is the total capacitance of the bus lines.

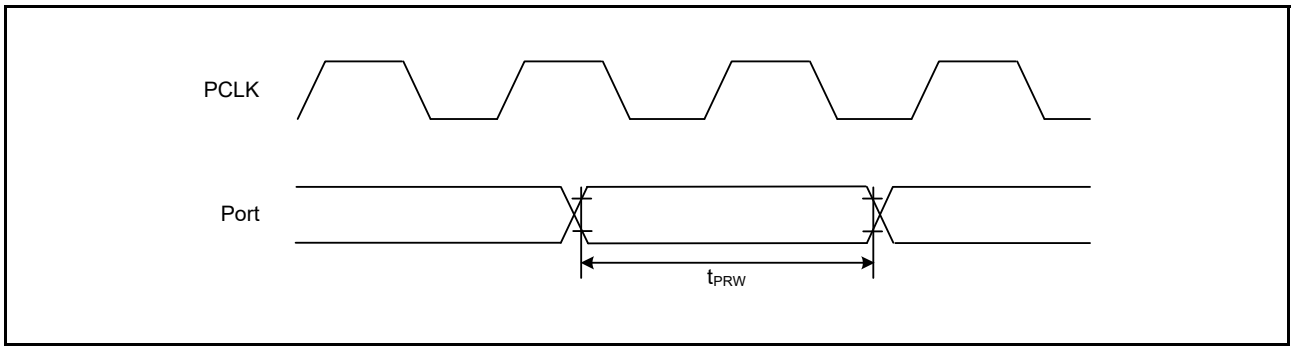


Figure 5.34 I/O Port Input Timing

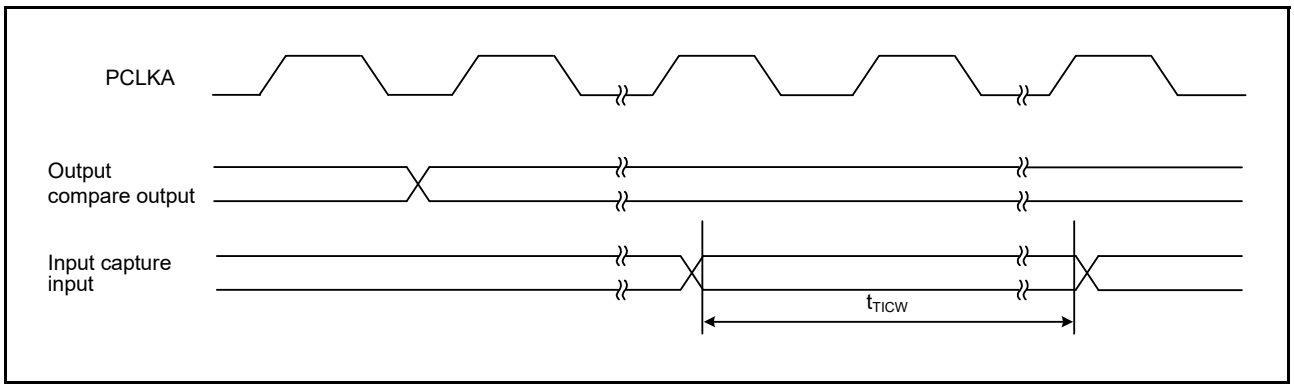


Figure 5.35 MTU3 Input/Output Timing

Table 5.45 E2 DataFlash Characteristics (3): Middle-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V,

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{Dp1}	—	135.0	1197.0	—	86.5	822.5	µs
Erasure time	1-Kbyte	t_{DE1K}	—	19.6	500.1	—	8.0	264.1	ms
	8-Kbyte	t_{DE8K}	—	119.9	2557.4	—	27.7	668.2	ms
Blank check time	1-byte	t_{DBC1}	—	—	85.0	—	—	50.9	µs
	1-Kbyte	t_{DBC1K}	—	—	7246.0	—	—	1457.5	µs
Erase operation forcible stop time		t_{DSED}	—	—	28.0	—	—	21.3	µs
Data flash-module stop release time		t_{DSTOP}	0.72	—	—	0.72	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

REVISION HISTORY	RX24U Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Mar 31, 2017	—	First edition, issued	