Renesas Electronics America Inc - R5F524UCADFB#30 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	110
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 22x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524ucadfb-30

Table 1.5 List of Pins and Pin Functions (144-Pin LFQFP) (2/4)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU3, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
50		PB0	MTIOC0D, MTIOC0D#, TMO0	TXD6, SMOSI6, SSDA6, MOSIA	ADTRG2#
51		PA7	TMO2, ADSM0		
52		PA6	TMO6, ADSM1		
53		PA5	MTIOC1A, MTIOC1A#, TMCI3	RXD6, SMISO6, SSCL6, MISOA	IRQ1, ADTRG1#
54		PA4	MTIOC1B, MTIOC1B#, TMCI7	SCK6, RSPCKA	ADTRG0#
55		PA3	MTIOC2A, MTIOC2A#, TMRI7, GTADSM0	SSLA0	
56		PA2	MTIOC2B, MTIOC2B#, TMO7, GTADSM1	CTS6#, RTS6#, SS6#, SSLA1	
57		PA1	MTIOC6A, MTIOC6A#, TMO4	SSLA2, CRXD0	ADTRG0#
58		PA0	MTIOC6C, MTIOC6C#, TMO2	SSLA3, CTXD0	
59		P35	TMO0, GTADSM0	CTS8#, RTS8#, SS8#	
60		P34	TMO4, GTADSM1	CTS9#, RTS9#, SS9#	
61		PC6	MTIOC1A, MTIOC1A#	RXD11, SMISO11, SSCL11	
62		PC5	MTIOC1B, MTIOC1B#	TXD11, SMOSI11, SSDA11	
63	VCC				
64		P96	POE4#	CTS8#, RTS8#, SS8#	IRQ4
65	VSS				
66	VSS				
67		P95	MTIOC6B, MTIOC6B#		
68		P94	MTIOC7A, MTIOC7A#		
69		P93	MTIOC7B, MTIOC7B#		
70		P92	MTIOC6D, MTIOC6D#		
71		P91	MTIOC7C, MTIOC7C#		
72		P90	MTIOC7D, MTIOC7D#		
73		P76	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#		
74		P75	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#		
75		P74	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#		
76		P73	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#		
77		P72	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#		
78		P71	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#		
79		P70	POE0#	CTS9#, RTS9#, SS9#	IRQ5
80		PG2	GTETRG	SCK9	COMP0
81		PG1		TXD9, SMOSI9, SSDA9	COMP1
82		PG0		RXD9, SMISO9, SSCL9	COMP2
83		P33	MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0	SSLA3	
84		P32	MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6	SSLA2	
85	VCC				
86	VCC				
87		P31	MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6	SSLA1	IRQ6
88	VSS				
89	VSS				
90		P30	MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6	SSLA0	IRQ7, COMP3
91		P27	MTIOC1A, MTIOC1A#		
92		P26	MTIOC9A, MTIOC9A#	CTS1#, RTS1#, SS1#	ADST0
93		P25	MTIOC9C, MTIOC9C#	SCK1	ADST1
94		P24	MTIC5U, MTIC5U#, TMCI2, TMO6	RSPCKA	COMP0, DA0
95		P23	MTIC5V, MTIC5V#, TMO2, CACREF	MOSIA	COMP1, DA1

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU3, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
51		P76	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#		
52		P75	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#		
53		P74	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#		
54		P73	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#		
55		P72	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#		
56		P71	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#		
57		P70	POE0#		IRQ5
58		P33	MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0	SSLA3	
59		P32	MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6	SSLA2	
60	VCC				
61		P31	MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6	SSLA1	IRQ6
62	VSS				
63		P30	MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6	SSLA0	IRQ7, COMP3
64		P27	MTIOC1A, MTIOC1A#		
65		P24	MTIC5U, MTIC5U#, TMCI2, TMO6	RSPCKA	COMP0, DA0
66		P23	MTIC5V, MTIC5V#, TMO2, CACREF	MOSIA	COMP1, DA1
67		P22	MTIC5W, MTIC5W#, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
68		P21	MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCI4		IRQ6, ADTRG1#, AN116
69		P20	MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4		IRQ7, ADTRG0#, AN016
70		P65			AN205
71		P64			AN204
72	AVCC2				
73	AVSS2				
74		P63			AN203, IRQ7
75		P62			AN202, IRQ6
76		P61			AN201, IRQ5
77		P60			AN200, IRQ4
78		P55			AN211, IRQ3
79		P54			AN210, IRQ2
80		P53			AN209, IRQ1
81		P52			AN208, IRQ0
82		P47			AN103
83		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
84		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
85		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
86	PGAVSS1				
87		P43			AN003
88		P42			AN002
89		P41			AN001
90		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
91	PGAVSS0				

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen 32-bit general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers.
R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt stack pointer (ISP) and user stack pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Exception table register (EXTB)

The exception table register (EXTB) specifies the address where the exception vector table starts.
Set the EXTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(3) Interrupt table register (INTB)

The interrupt table register (INTB) specifies the address where the interrupt vector table starts.
Set the INTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(4) Program counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(5) Processor status word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(6) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(7) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(8) Fast interrupt vector register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK
0008 0031h	SYSTEM	Memory Wait Cycle Setting Register	MEMWAIT	8	8	3 ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK
0008 0037h	SYSTEM	High-Speed On-Chip Oscillator Control Register 2	HOCOCR2	8	8	3 ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK
0008 00A5h	SYSTEM	High-Speed On-Chip Oscillator Wait Control Register	HOCOWTCR	8	8	3 ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK
0008 1000h	FLASH	ROM Cache Enable Register	ROMCE	16	16	3 ICLK
0008 1004h	FLASH	ROM Cache Invalidate Register	ROMCIV	16	16	3 ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK

Table 4.1 List of I/O Registers (Address Order) (3/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 7043h	ICU	Interrupt Request Register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt Request Register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt Request Register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt Request Register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt Request Register 071	IR071	8	8	2 ICLK
0008 7058h	ICU	Interrupt Request Register 088	IR088	8	8	2 ICLK
0008 7059h	ICU	Interrupt Request Register 089	IR089	8	8	2 ICLK
0008 7062h	ICU	Interrupt Request Register 098	IR098	8	8	2 ICLK
0008 7063h	ICU	Interrupt Request Register 099	IR099	8	8	2 ICLK
0008 7064h	ICU	Interrupt Request Register 100	IR100	8	8	2 ICLK
0008 7065h	ICU	Interrupt Request Register 101	IR101	8	8	2 ICLK
0008 7066h	ICU	Interrupt Request Register 102	IR102	8	8	2 ICLK
0008 7067h	ICU	Interrupt Request Register 103	IR103	8	8	2 ICLK
0008 7068h	ICU	Interrupt Request Register 104	IR104	8	8	2 ICLK
0008 7069h	ICU	Interrupt Request Register 105	IR105	8	8	2 ICLK
0008 706Ah	ICU	Interrupt Request Register 106	IR106	8	8	2 ICLK
0008 706Bh	ICU	Interrupt Request Register 107	IR107	8	8	2 ICLK
0008 706Ch	ICU	Interrupt Request Register 108	IR108	8	8	2 ICLK
0008 706Dh	ICU	Interrupt Request Register 109	IR109	8	8	2 ICLK
0008 706Eh	ICU	Interrupt Request Register 110	IR110	8	8	2 ICLK
0008 706Fh	ICU	Interrupt Request Register 111	IR111	8	8	2 ICLK
0008 7070h	ICU	Interrupt Request Register 112	IR112	8	8	2 ICLK
0008 7071h	ICU	Interrupt Request Register 113	IR113	8	8	2 ICLK
0008 7072h	ICU	Interrupt Request Register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt Request Register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK
0008 708Eh	ICU	Interrupt Request Register 142	IR142	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (14/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 9086h	S12AD	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB
0008 90D4h	S12AD	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB
0008 90D6h	S12AD	A/D Channel Select Register C1	ADANSC1	16	16	2 or 3 PCLKB
0008 90D9h	S12AD	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB
0008 90DDh	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 91A0h	S12AD	A/D Programmable Gain Amplifier Control Register	ADPGACR	16	16	2 or 3 PCLKB
0008 91A2h	S12AD	A/D Programmable Gain Amplifier Gain Setting Register 0	ADPGAGS0	16	16	2 or 3 PCLKB
0008 9200h	S12AD1	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9204h	S12AD1	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9206h	S12AD1	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB
0008 9208h	S12AD1	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 920Ah	S12AD1	A/D-Converted Value Addition/Average Function Channel Select Register 1	ADADS1	16	16	2 or 3 PCLKB
0008 920Ch	S12AD1	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 920Eh	S12AD1	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9210h	S12AD1	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9214h	S12AD1	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9216h	S12AD1	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB
0008 9218h	S12AD1	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 921Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9220h	S12AD1	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9222h	S12AD1	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9224h	S12AD1	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9226h	S12AD1	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9240h	S12AD1	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB
0008 9266h	S12AD1	A/D Sample-and-hold Circuit Control Register	ADSHCR	16	16	2 or 3 PCLKB
0008 927Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 9280h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 9284h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB
0008 9286h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB
0008 92D4h	S12AD1	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB
0008 92D6h	S12AD1	A/D Channel Select Register C1	ADANSC1	16	16	2 or 3 PCLKB
0008 92D9h	S12AD1	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB
0008 92DDh	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 92E0h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 92E1h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 92E2h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 92E3h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 93A0h	S12AD1	A/D Programmable Gain Amplifier Control Register	ADPGACR	16	16	2 or 3 PCLKB
0008 93A2h	S12AD1	A/D Programmable Gain Amplifier Gain Setting Register 0	ADPGAGS0	16	16	2 or 3 PCLKB
0008 9400h	S12AD2	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9404h	S12AD2	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9408h	S12AD2	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 940Ch	S12AD2	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 940Eh	S12AD2	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9410h	S12AD2	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (18/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C006h	PORT6	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C007h	PORT7	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C008h	PORT8	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C009h	PORT9	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Fh	PORTF	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C010h	PORTG	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C026h	PORT6	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C027h	PORT7	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C028h	PORT8	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C029h	PORT9	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Dh	PORTD	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C02Fh	PORTF	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C030h	PORTG	Port Output Data Register	PODR	8	8	2 or 3 PCLKB
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C045h	PORT5	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C046h	PORT6	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C047h	PORT7	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C048h	PORT8	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C049h	PORT9	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C04Ah	PORTA	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C04Dh	PORTD	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C04Fh	PORTF	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C050h	PORTG	Port Input Data Register	PIDR	8	8	2 or 3 PCLKB
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 or 3 PCLKB
0008 C067h	PORT7	Port Mode Register	PMR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (22/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2 or 3 PCLKB
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2 or 3 PCLKB
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2 or 3 PCLKB
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2 or 3 PCLKB
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2 or 3 PCLKB
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2 or 3 PCLKB
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2 or 3 PCLKB
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2 or 3 PCLKB
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2 or 3 PCLKB
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2 or 3 PCLKB
0008 C1B8h	MPC	PF0 Pin Function Control Register	PF0PFS	8	8	2 or 3 PCLKB
0008 C1B9h	MPC	PF1 Pin Function Control Register	PF1PFS	8	8	2 or 3 PCLKB
0008 C1BAh	MPC	PF2 Pin Function Control Register	PF2PFS	8	8	2 or 3 PCLKB
0008 C1BBh	MPC	PF3 Pin Function Control Register	PF3PFS	8	8	2 or 3 PCLKB
0008 C1C0h	MPC	PG0 Pin Function Control Register	PG0PFS	8	8	2 or 3 PCLKB
0008 C1C1h	MPC	PG1 Pin Function Control Register	PG1PFS	8	8	2 or 3 PCLKB
0008 C1C2h	MPC	PG2 Pin Function Control Register	PG2PFS	8	8	2 or 3 PCLKB
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4 or 5 PCLKB
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 or 5 PCLKB
0008 C4C0h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB
0008 C4C2h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB
0008 C4C4h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB
0008 C4C6h	POE	Output Level Control/Status Register 2	OCSR2	16	8, 16	2 or 3 PCLKB
0008 C4C8h	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB
0008 C4CAh	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB
0008 C4CBh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB
0008 C4CCh	POE	Port Output Enable Control Register 2	POECR2	16	16	2 or 3 PCLKB
0008 C4CEh	POE	Port Output Enable Control Register 3	POECR3	16	16	2 or 3 PCLKB
0008 C4D0h	POE	Port Output Enable Control Register 4	POECR4	16	16	2 or 3 PCLKB
0008 C4D2h	POE	Port Output Enable Control Register 5	POECR5	16	16	2 or 3 PCLKB
0008 C4D4h	POE	Port Output Enable Control Register 6	POECR6	16	16	2 or 3 PCLKB
0008 C4D6h	POE	Input Level Control/Status Register 4	ICSR4	16	8, 16	2 or 3 PCLKB
0008 C4D8h	POE	Input Level Control/Status Register 5	ICSR5	16	8, 16	2 or 3 PCLKB
0008 C4DAh	POE	Active Level Setting Register 1	ALR1	16	8, 16	2 or 3 PCLKB
0008 C4DCh	POE	Input Level Control/Status Register 6	ICSR6	16	16	2 or 3 PCLKB
0008 C4DEh	POE	Active Level Setting Register 2	ALR2	16	8, 16	2 or 3 PCLKB
0008 C4E0h	POE	Input Level Control/Status Register 7	ICSR7	16	8, 16	2 or 3 PCLKB
0008 C4E2h	POE	Port Output Enable Control Register 7	POECR7	16	16	2 or 3 PCLKB
0008 C4E4h	POE	Port Output Enable Control Register 8	POECR8	16	16	2 or 3 PCLKB
0008 C4E6h	POE	Port Output Enable Comparator Output Detection Flag Register	POECMPFR	16	16	2 or 3 PCLKB
0008 C4E8h	POE	Port Output Enable Comparator Request Select Register	POECMPSEL	16	16	2 or 3 PCLKB
0008 C4EAh	POE	Output Level Control/Status Register 3	OCSR3	16	8, 16	2 or 3 PCLKB
0008 C4ECh	POE	Active Level Setting Register 3	ALR3	16	8, 16	2 or 3 PCLKB
0008 C4F0h	POE	Port Mode Mask Control Register 0	PMMCR0	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (34/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000C 1A2Dh	MTU7	Timer Status Register	TSR	8	8	4 or 5 PCLKA
000C 1A30h	MTU	Timer Interrupt Skipping Set Register 1B	TITCR1B	8	8, 16	4 or 5 PCLKA
000C 1A31h	MTU	Timer Interrupt Skipping Counters 1B	TITCNT1B	8	8	4 or 5 PCLKA
000C 1A32h	MTU	Timer Buffer Transfer Set Register B	TBTERB	8	8	4 or 5 PCLKA
000C 1A34h	MTU	Timer Dead Time Enable Register B	TDERB	8	8	4 or 5 PCLKA
000C 1A36h	MTU	Timer Output Level Buffer Register B	TOLBRB	8	8	4 or 5 PCLKA
000C 1A38h	MTU6	Timer Buffer Operation Transfer Mode Register	TBTM	8	8, 16	4 or 5 PCLKA
000C 1A39h	MTU7	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4 or 5 PCLKA
000C 1A3Ah	MTU	Timer Interrupt Skipping Mode Register B	TITMRB	8	8	4 or 5 PCLKA
000C 1A3Bh	MTU	Timer Interrupt Skipping Set Register 2B	TITCR2B	8	8	4 or 5 PCLKA
000C 1A3Ch	MTU	Timer Interrupt Skipping Counters 2B	TITCNT2B	8	8	4 or 5 PCLKA
000C 1A40h	MTU7	Timer A/D Converter Start Request Control Register	TADCR	16	16	4 or 5 PCLKA
000C 1A44h	MTU7	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16, 32	4 or 5 PCLKA
000C 1A46h	MTU7	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4 or 5 PCLKA
000C 1A48h	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16, 32	4 or 5 PCLKA
000C 1A4Ah	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4 or 5 PCLKA
000C 1A4Ch	MTU6	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA
000C 1A4Dh	MTU7	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA
000C 1A50h	MTU6	Timer Synchronous Clear Register	TSYCR	8	8	4 or 5 PCLKA
000C 1A60h	MTU	Timer Waveform Control Register B	TWCRB	8	8	4 or 5 PCLKA
000C 1A70h	MTU	Timer Mode Register 2B	TMDR2B	8	8	4 or 5 PCLKA
000C 1A72h	MTU6	Timer General Register E	TGRE	16	16	4 or 5 PCLKA
000C 1A74h	MTU7	Timer General Register E	TGRE	16	16	4 or 5 PCLKA
000C 1A76h	MTU7	Timer General Register F	TGRF	16	16	4 or 5 PCLKA
000C 1A80h	MTU	Timer Start Register B	TSTRB	8	8, 16	4 or 5 PCLKA
000C 1A81h	MTU	Timer Synchronous Register B	TSYRB	8	8	4 or 5 PCLKA
000C 1A84h	MTU	Timer Read/Write Enable Register B	TRWERB	8	8	4 or 5 PCLKA
000C 1A93h	MTU6	Noise Filter Control Register 6	NFCR6	8	8	4 or 5 PCLKA
000C 1A94h	MTU7	Noise Filter Control Register 7	NFCR7	8	8	4 or 5 PCLKA
000C 1A95h	MTU5	Noise Filter Control Register 5	NFCR5	8	8	4 or 5 PCLKA
000C 1C80h	MTU5	Timer Counter U	TCNTU	16	16, 32	4 or 5 PCLKA
000C 1C82h	MTU5	Timer General Register U	TGRU	16	16	4 or 5 PCLKA
000C 1C84h	MTU5	Timer Control Register U	TCRU	8	8	4 or 5 PCLKA
000C 1C85h	MTU5	Timer Control Register 2U	TCR2U	8	8	4 or 5 PCLKA
000C 1C86h	MTU5	Timer I/O Control Register U	TIORU	8	8	4 or 5 PCLKA
000C 1C90h	MTU5	Timer Counter V	TCNTV	16	16, 32	4 or 5 PCLKA
000C 1C92h	MTU5	Timer General Register V	TGRV	16	16	4 or 5 PCLKA
000C 1C94h	MTU5	Timer Control Register V	TCRV	8	8	4 or 5 PCLKA
000C 1C95h	MTU5	Timer Control Register 2V	TCR2V	8	8	4 or 5 PCLKA
000C 1C96h	MTU5	Timer I/O Control Register V	TIORV	8	8	4 or 5 PCLKA
000C 1CA0h	MTU5	Timer Counter W	TCNTW	16	16, 32	4 or 5 PCLKA
000C 1CA2h	MTU5	Timer General Register W	TGRW	16	16	4 or 5 PCLKA
000C 1CA4h	MTU5	Timer Control Register W	TCRW	8	8	4 or 5 PCLKA
000C 1CA5h	MTU5	Timer Control Register 2W	TCR2W	8	8	4 or 5 PCLKA
000C 1CA6h	MTU5	Timer I/O Control Register W	TIORW	8	8	4 or 5 PCLKA
000C 1CB2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	4 or 5 PCLKA
000C 1CB4h	MTU5	Timer Start Register	TSTR	8	8	4 or 5 PCLKA
000C 1CB6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	4 or 5 PCLKA
000C 1D30h	MTU	A/D Conversion Start Request Select Register 0	TADSTRGR0	8	8	4 or 5 PCLKA
000C 1D32h	MTU	A/D Conversion Start Request Select Register 1	TADSTRGR1	8	8	4 or 5 PCLKA
000C 2000h	GPT	General PWM Timer Software Start Register	GTSTR	16	8, 16, 32	4 or 5 PCLKA

Table 4.1 List of I/O Registers (Address Order) (39/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000C 23C4h	GPT23	General PWM Timer Longword Dead Time Value Register D	GTDVDLW	32	32	4 or 5 PCLKA
000C 23C8h	GPT23	General PWM Timer Longword Dead Time Buffer Register U	GTDBULW	32	32	4 or 5 PCLKA
000C 23CCh	GPT23	General PWM Timer Longword Dead Time Buffer Register D	GTDBDLW	32	32	4 or 5 PCLKA
000D 0000h	SCI11	Serial Mode Register	SMR	8	8	3 or 4 PCLKA
000D 0001h	SCI11	Bit Rate Register	BRR	8	8	3 or 4 PCLKA
000D 0002h	SCI11	Serial Control Register	SCR	8	8	3 or 4 PCLKA
000D 0003h	SCI11	Transmit Data Register	TDR	8	8	3 or 4 PCLKA
000D 0004h	SCI11	Serial Status Register	SSR	8	8	3 or 4 PCLKA
000D 0005h	SCI11	Receive Data Register	RDR	8	8	3 or 4 PCLKA
000D 0006h	SMCI11	Smart Card Mode Register	SCMR	8	8	3 or 4 PCLKA
000D 0007h	SCI11	Serial Extended Mode Register	SEMR	8	8	3 or 4 PCLKA
000D 0008h	SCI11	Noise Filter Setting Register	SNFR	8	8	3 or 4 PCLKA
000D 0009h	SCI11	I^2C Mode Register 1	SIMR1	8	8	3 or 4 PCLKA
000D 000Ah	SCI11	I^2C Mode Register 2	SIMR2	8	8	3 or 4 PCLKA
000D 000Bh	SCI11	I^2C Mode Register 3	SIMR3	8	8	3 or 4 PCLKA
000D 000Ch	SCI11	I^2C Status Register	SISR	8	8	3 or 4 PCLKA
000D 000Dh	SCI11	SPI Mode Register	SPMR	8	8	3 or 4 PCLKA
000D 000Eh	SCI11	Transmit Data Register HL	TDRHL	16	16	5 or 6 PCLKA
000D 000Eh	SCI11	Transmit Data Register H	TDRH	8	8	3 or 4 PCLKA
000D 000Fh	SCI11	Transmit Data Register L	TDRL	8	8	3 or 4 PCLKA
000D 0010h	SCI11	Receive Data Register HL	RDRHL	16	16	5 or 6 PCLKA
000D 0010h	SCI11	Receive Data Register H	RDRH	8	8	3 or 4 PCLKA
000D 0011h	SCI11	Receive Data Register L	RDRL	8	8	3 or 4 PCLKA
000D 0012h	SCI11	Modulation Duty Register	MDDR	8	8	3 or 4 PCLKA
007F C090h	FLASH	E2 DataFlash Control Register	DFLCTL	8	8	2 or 3 FCLK
007F C100h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 FCLK
007F C104h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 FCLK
007F C108h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 FCLK
007F C110h	FLASH	Flash Processing Start Address Register H	FSARH	16	16	2 or 3 FCLK
007F C114h	FLASH	Flash Control Register	FCR	8	8	2 or 3 FCLK
007F C118h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 FCLK
007F C120h	FLASH	Flash Processing End Address Register H	FEARH	16	16	2 or 3 FCLK
007F C124h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 FCLK
007F C12Ch	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 FCLK
007F C130h	FLASH	Flash Write Buffer 0 Register	FWB0	16	16	2 or 3 FCLK
007F C138h	FLASH	Flash Write Buffer 1 Register	FWB1	16	16	2 or 3 FCLK
007F C140h	FLASH	Flash Write Buffer 2 Register	FWB2	16	16	2 or 3 FCLK
007F C144h	FLASH	Flash Write Buffer 3 Register	FWB3	16	16	2 or 3 FCLK
007F C180h	FLASH	Protection Unlock Register	FPR	8	8	2 or 3 FCLK
007F C184h	FLASH	Protection Unlock Status Register	FPSR	8	8	2 or 3 FCLK
007F C1C0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	2 or 3 FCLK
007F C1C8h	FLASH	Flash Access Window Start Address Monitor Register	FAWSMR	16	16	2 or 3 FCLK
007F C1D0h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 FCLK
007F C1D8h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 FCLK
007F C1DCh	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 FCLK
007F C1E0h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 FCLK
007F C1E8h	FLASH	Flash Error Address Monitor Register H	FEAMH	16	16	2 or 3 FCLK
007F C1F0h	FLASH	Flash Status Register 0	FSTATR0	8	8	2 or 3 FCLK
007F C350h	FLASHCONST	Unique ID Register 0	UIDR0	32	32	2 or 3 FCLK

Table 4.1 List of I/O Registers (Address Order) (40/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
007F C354h	FLASHCONST	Unique ID Register 1	UIDR1	32	32	2 or 3 FCLK
007F C358h	FLASHCONST	Unique ID Register 2	UIDR2	32	32	2 or 3 FCLK
007F C35Ch	FLASHCONST	Unique ID Register 3	UIDR3	32	32	2 or 3 FCLK
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 or 3 FCLK

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0, TMR2, TMR4, or TMR6 register. Table 23.5 lists register allocation for 16-bit access in the User's Manual: Hardware.

Item					Symbol	Typ. *7	Max.	Unit	Test Conditions
Supply current *1	High-speed operating mode	Deep sleep mode	No peripheral operation*2	ICLK = 80 MHz	I_{CC}	3.4	—	mA	
				ICLK = 64 MHz		2.9	—		
				ICLK = 32 MHz		2.5	—		
				ICLK = 16 MHz		2.3	—		
				ICLK = 8 MHz		2.2	—		
			All peripheral operation: Normal	ICLK = 80 MHz*3		22.2	—		
				ICLK = 64 MHz*4		17.9	—		
				ICLK = 32 MHz*5		12.9	—		
				ICLK = 16 MHz*5		7.6	—		
				ICLK = 8 MHz*5		4.8	—		
		Increase during BGO operation*6				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*8	ICLK = 12 MHz*10	I_{CC}	5.3	—	mA	
				ICLK = 8 MHz		4.5	—		
				ICLK = 1 MHz		2.5	—		
			All peripheral operation: Normal*9	ICLK = 12 MHz*10		8.7	—		
				ICLK = 8 MHz		6.9	—		
				ICLK = 1 MHz		2.7	—		
			All peripheral operation: Max.*9	ICLK = 12 MHz*10		—	18.0		
		Sleep mode	No peripheral operation*8	ICLK = 12 MHz*10		2.6	—		
				ICLK = 8 MHz		2.7	—		
				ICLK = 1 MHz		2.2	—		
			All peripheral operation: Normal*9	ICLK = 12 MHz*10		6.7	—		
				ICLK = 8 MHz		5.6	—		
				ICLK = 1 MHz		2.5	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 12 MHz*10		1.8	—		
				ICLK = 8 MHz		2.1	—		
				ICLK = 1 MHz		2.1	—		
			All peripheral operation: Normal*9	ICLK = 12 MHz*10		5.7	—		
				ICLK = 8 MHz		4.8	—		
				ICLK = 1 MHz		2.3	—		
		Increase during BGO operation*6				2.5	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Supply of the clock signal to peripheral modules is stopped in this state. The clock source is PLL. FCLK, PCLKA, PCLKB, and PCLKD are set to divided by 64.
Note 3. The clock signal to peripheral modules is supplied in this state. The clock source is PLL. FCLK is set to divided by 4. PCLKA is set to divided by 1. PCLKB and PCLKD are set to divided by 2.
Note 4. The clock signal to peripheral modules is supplied in this state. The clock source is PLL. PCLKA is set to divided by 1. FCLK, PCLKB, and PCLKD are set to divided by 2.
Note 5. The clock signal to peripheral modules is supplied in this state. The clock source is PLL. The frequencies of FCLK, PCLKA, PCLKB, and PCLKD are same as ICLK.
Note 6. This is the increase when data is programmed to or erased from the ROM or E2 DataFlash during program execution.
Note 7. Values when VCC = 5 V.
Note 8. Supply of the clock signal to peripheral modules is stopped in this state. The clock source is PLL. FCLK, PCLKA, PCLKB, and PCLKD are set to divided by 64.
Note 9. Supply of the clock signal to peripheral modules is stopped in this state. The clock source is PLL. The frequencies of FCLK, PCLKA, PCLKB, and PCLKD are same as ICLK.
Note 10. When the frequency of PLL is 48 MHz.

Table 5.10 DC Characteristics (8)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

The ripple voltage must meet the allowable ripple frequency $f_{r\,(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (2.7 V). When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 5.3 $V_{r\,(VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 5.3 $V_{r\,(VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 5.3 $V_{r\,(VCC)} \leq VCC \times 0.06$
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

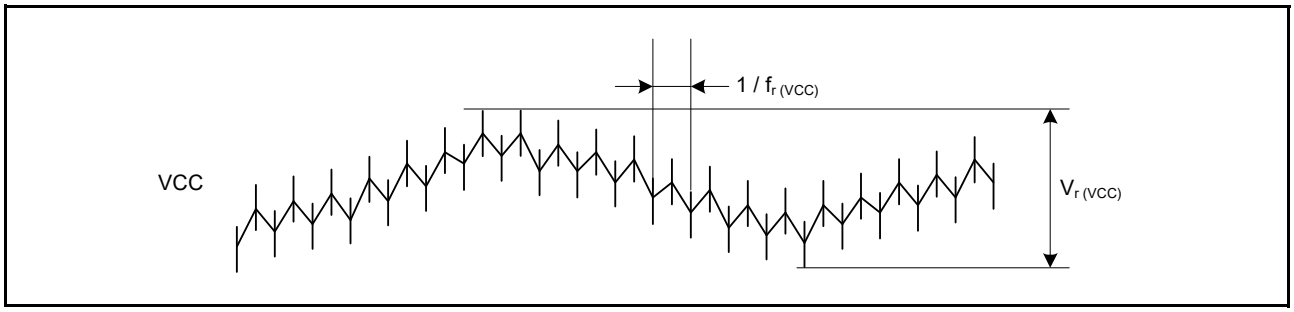

Figure 5.3 Ripple Waveform

Table 5.11 DC Characteristics (9)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C_{VCL}	3.3	4.7	6.1	µF	

Note: The recommended capacitance is 4.7 µF. Variations in connected capacitors should be within the above range.

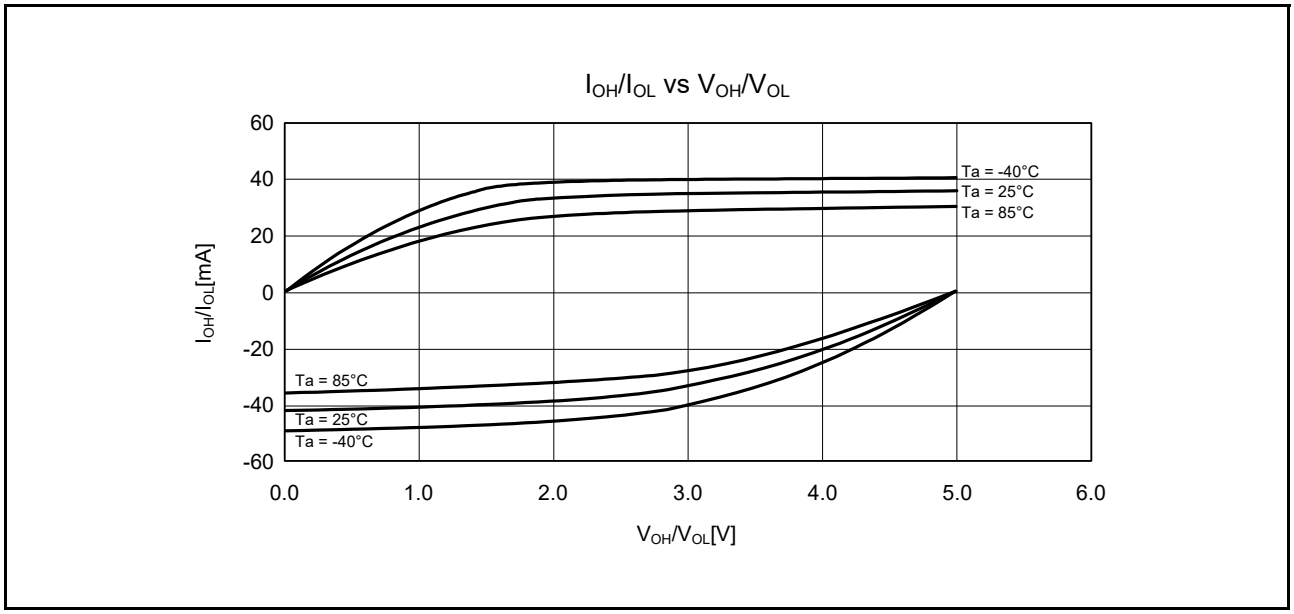

Figure 5.6 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.0 V when Normal Output is Selected (Reference Data)**

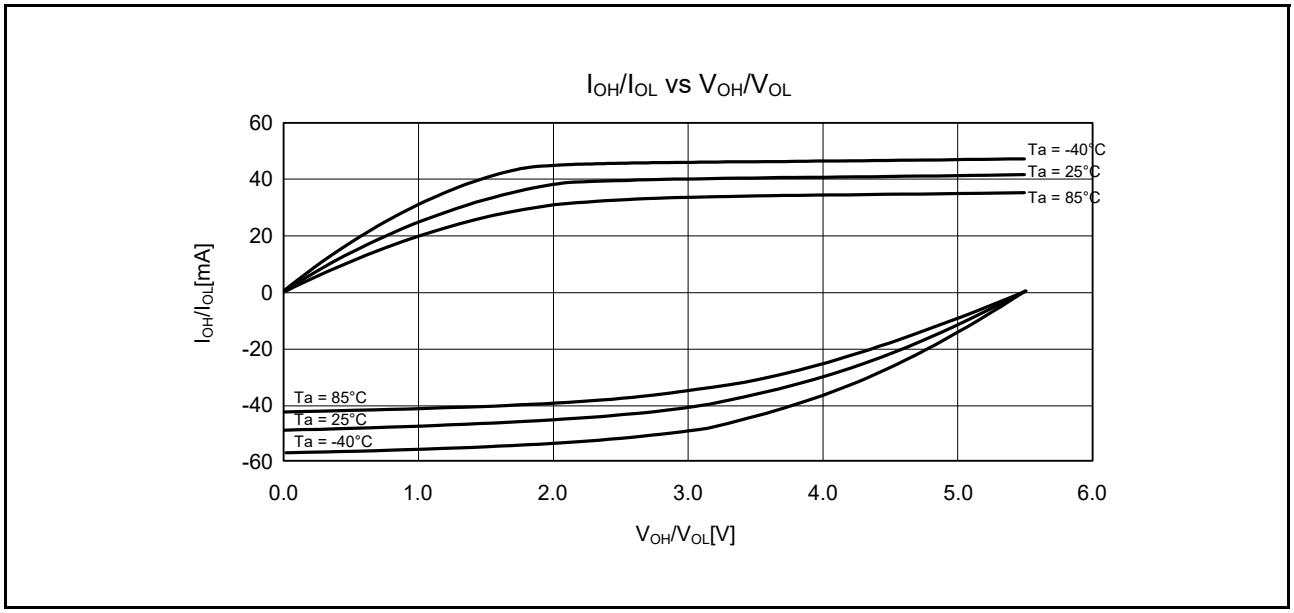

Figure 5.7 **V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 5.5 V when Normal Output is Selected (Reference Data)**

5.3.2 Reset Timing

Table 5.17 Reset Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 5.27
	Other than above	t_{RESW}	30	—	—	µs	Figure 5.28
Wait time after RES# cancellation (at power-on)		t_{RESWT}	—	27.5	—	ms	Figure 5.27
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	114	—	µs	Figure 5.28
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 5.29
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*1		t_{RESW2}	—	300	—	µs	
Wait time after software reset cancellation		t_{RESW2}	—	168	—	µs	

Note 1. When IWDTCR.CKS[3:0] = 0000b.

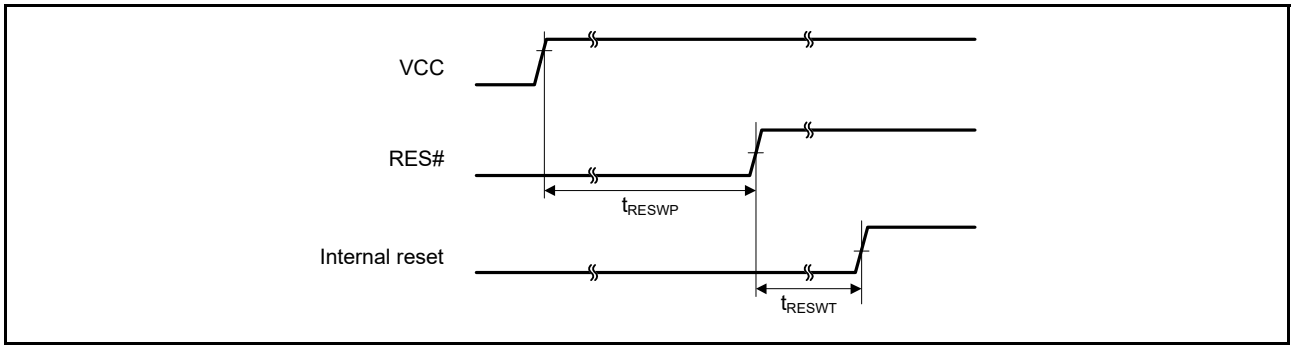

Figure 5.27 Reset Input Timing at Power-On

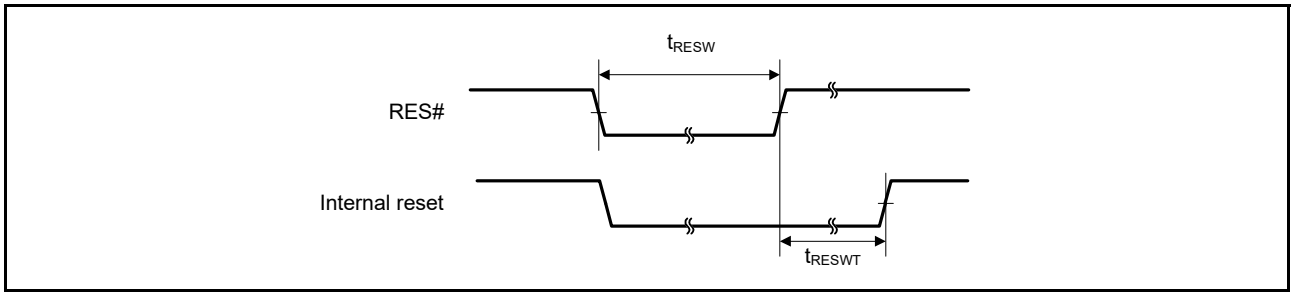

Figure 5.28 Reset Input Timing (1)

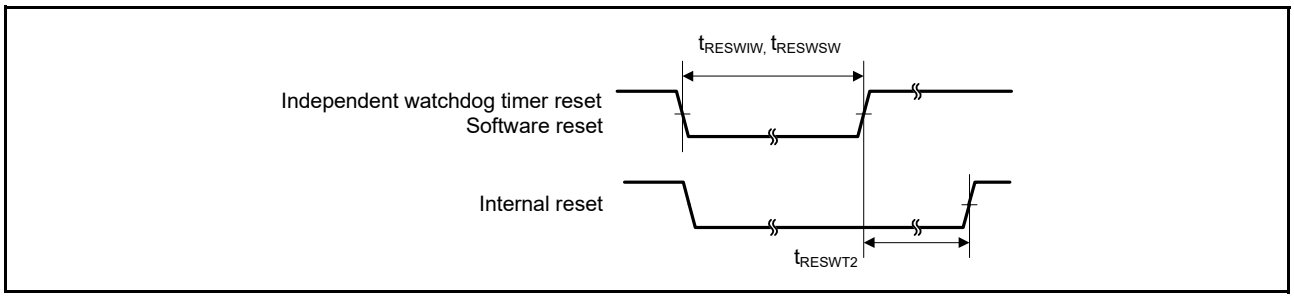

Figure 5.29 Reset Input Timing (2)

Table 5.24 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
SCI11	Input clock cycle		Asynchronous	t_{Scyc}	4	—	t_{PAcyc}	Figure 5.42
			Clock synchronous		6	—		
	Input clock frequency		Asynchronous	t_{Scyc}	—	10	MHz	
			Clock synchronous		—	6.67		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle		Asynchronous	t_{Scyc}	16	—	t_{PAcyc}	Figure 5.43
			Clock synchronous		4	—		
	Output clock frequency		Asynchronous	t_{Scyc}	—	5	MHz	
			Clock synchronous		—	10		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	VCC = 4.0 V or above		—	40	ns	
			VCC = 2.7 V or above		—	65	ns	
	Receive data setup time (master)	Clock synchronous	VCC = 4.0 V or above	t_{RXS}	40	—	ns	
			VCC = 2.7 V or above		65	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcyc}: PCLKA cycle

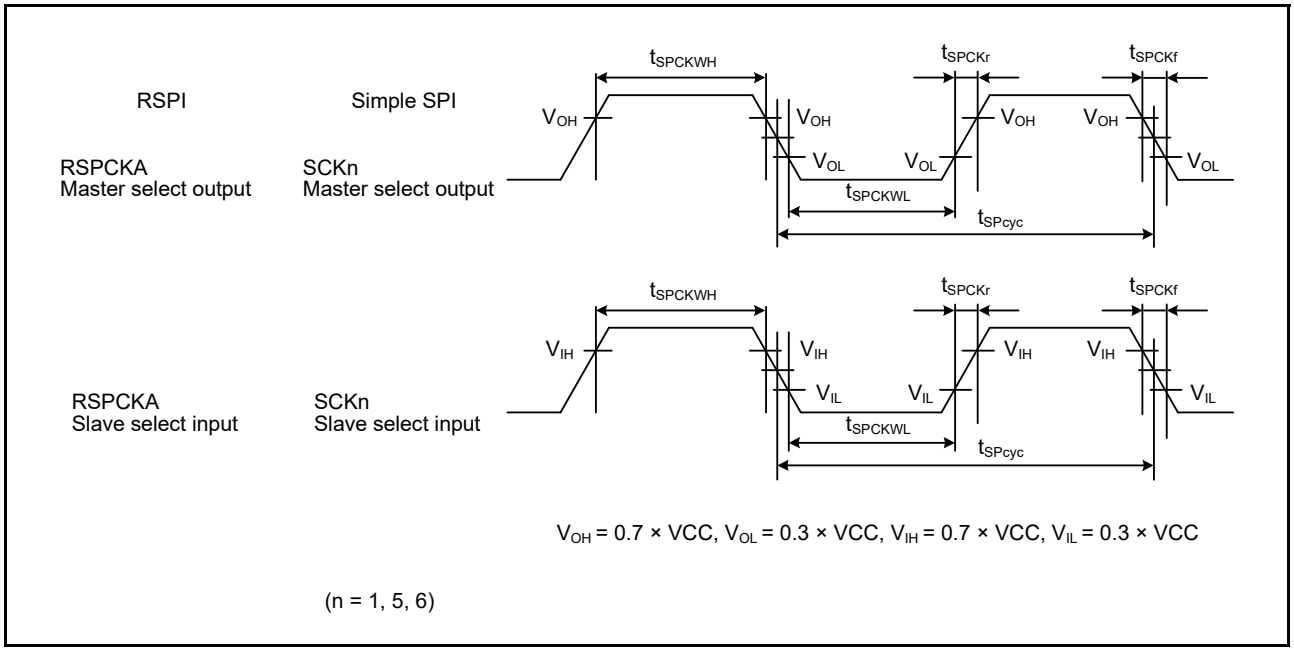

Figure 5.45 RSPI Clock Timing and Simple SPI Clock Timing

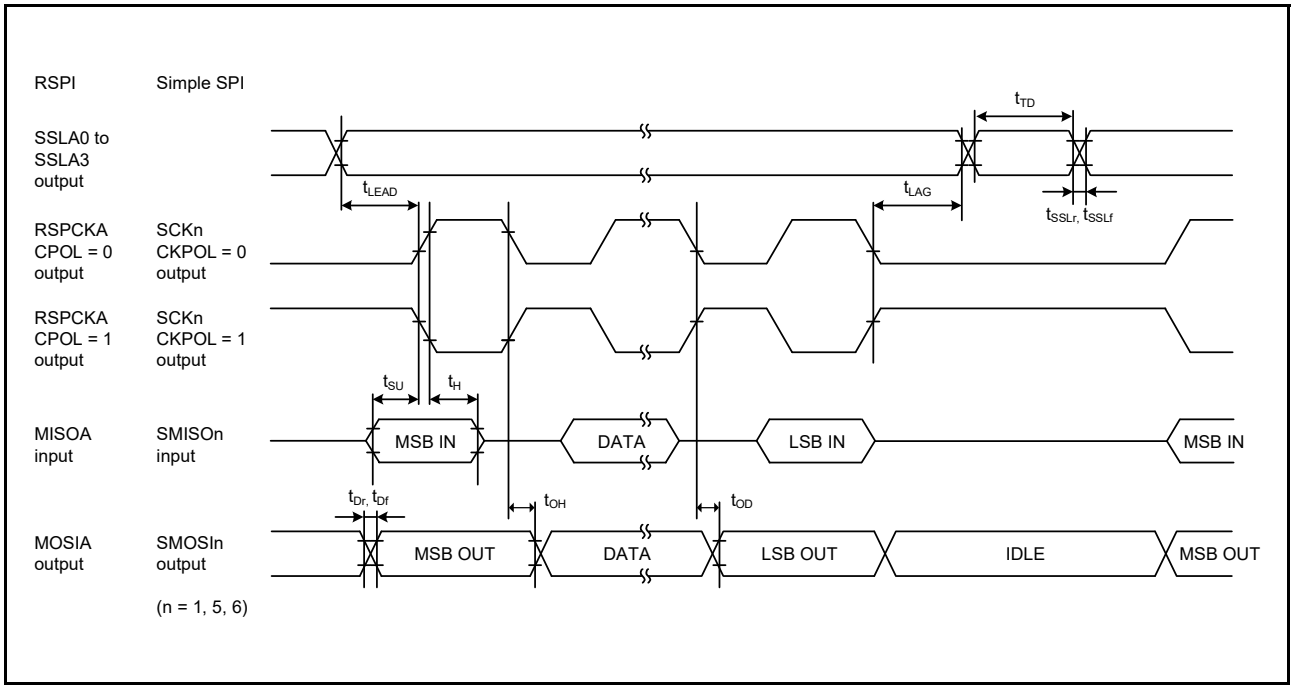

Figure 5.46 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

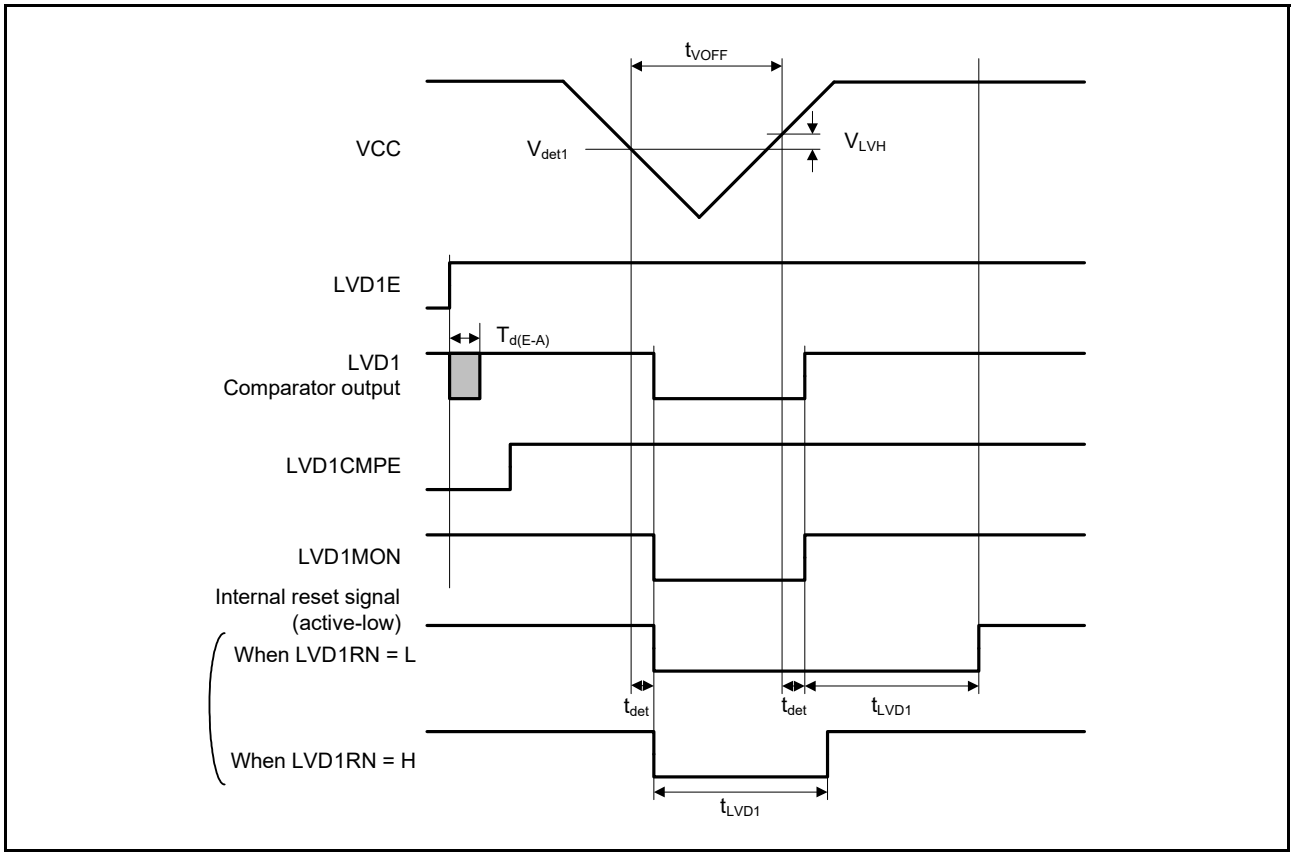

Figure 5.56 Voltage Detection Circuit Timing (V_{det1})

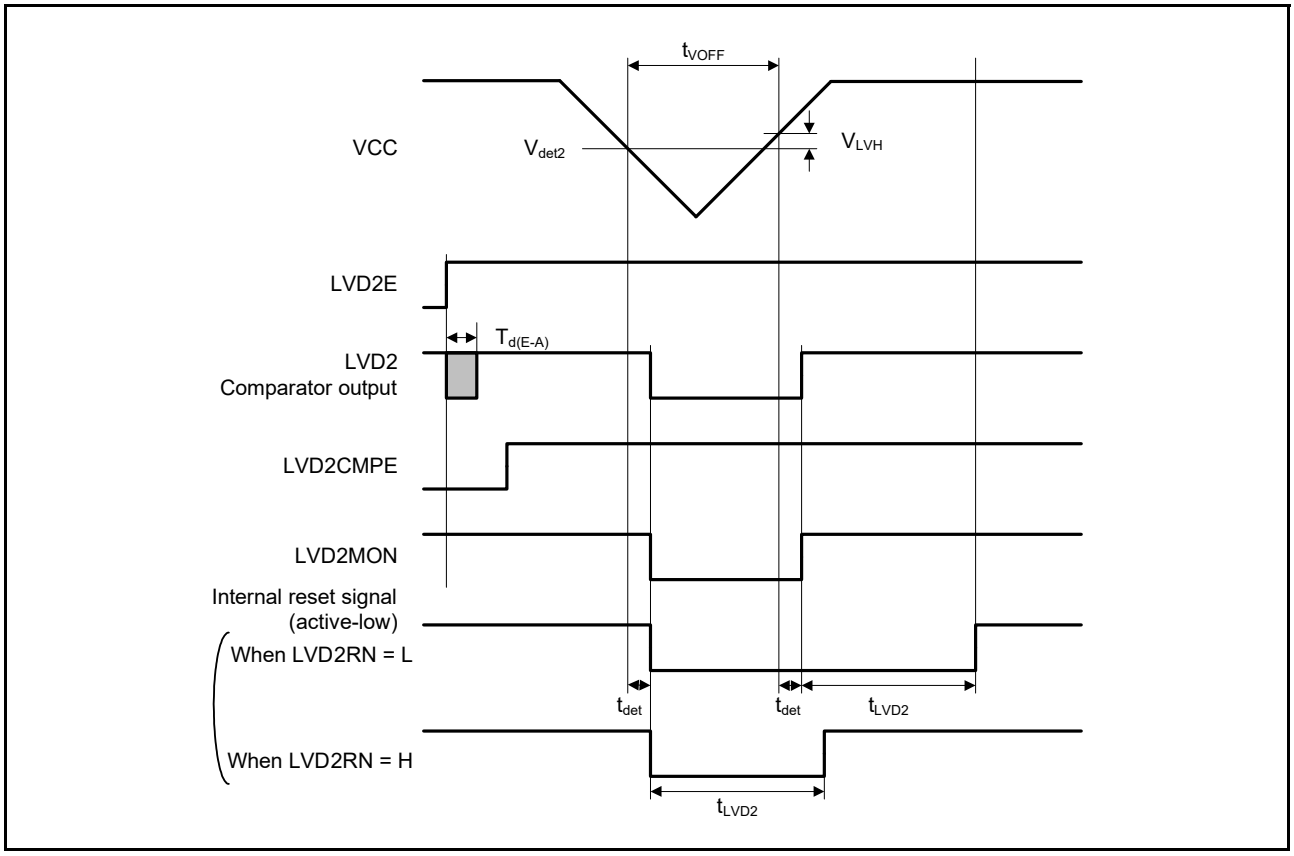

Figure 5.57 Voltage Detection Circuit Timing (V_{det2})

5.10 ROM (Flash Memory for Code Storage) Characteristics

Table 5.40 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	—	—	Year	T_a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 5.41 ROM (Flash Memory for Code Storage) Characteristics (2): High-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	112.0	967.0	—	52.3	490.5	µs
Erasure time	2-Kbyte	t_{E2K}	—	8.7	278.1	—	5.5	214.6	ms
	512-Kbyte (when block erase command used)	t_{E512K}	—	927.8	19218.0	—	72.0	1678.9	ms
	512-Kbyte (when all-block erase command used)	t_{EA512K}	—	922.7	19013.4	—	66.7	1469.2	ms
Blank check time	8-byte	t_{BC8}	—	—	55.0	—	—	16.1	µs
	2-Kbyte	t_{BC2K}	—	—	1840.0	—	—	135.7	µs
Erase operation forcible stop time		t_{SED}	—	—	18.0	—	—	10.7	µs
Start-up area switching setting time		t_{SAS}	—	12.3	566.5	—	6.2	433.5	ms
Access window time		t_{AWS}	—	12.3	566.5	—	6.2	433.5	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	µs
ROM mode transition wait time 2		t_{MS}	5.0	—	—	5.0	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

5.12 Usage Notes

5.12.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU to adjust automatically to the optimum level. A 4.7-µF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and VSS pin. Figure 5.59 and Figure 5.60 shows how to connect external capacitors. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin. Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor to the MCU power supply pins as close as possible. Use a recommended value of 0.1 µF as the capacitance of the capacitors. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 31, 12-Bit A/D Converter (S12ADF) in the User's Manual: Hardware.
For notes on designing the printed circuit board, see the descriptions of the application note "Hardware Design Guide" (R01AN1411EJ). The latest version can be downloaded from Renesas Electronics Website.

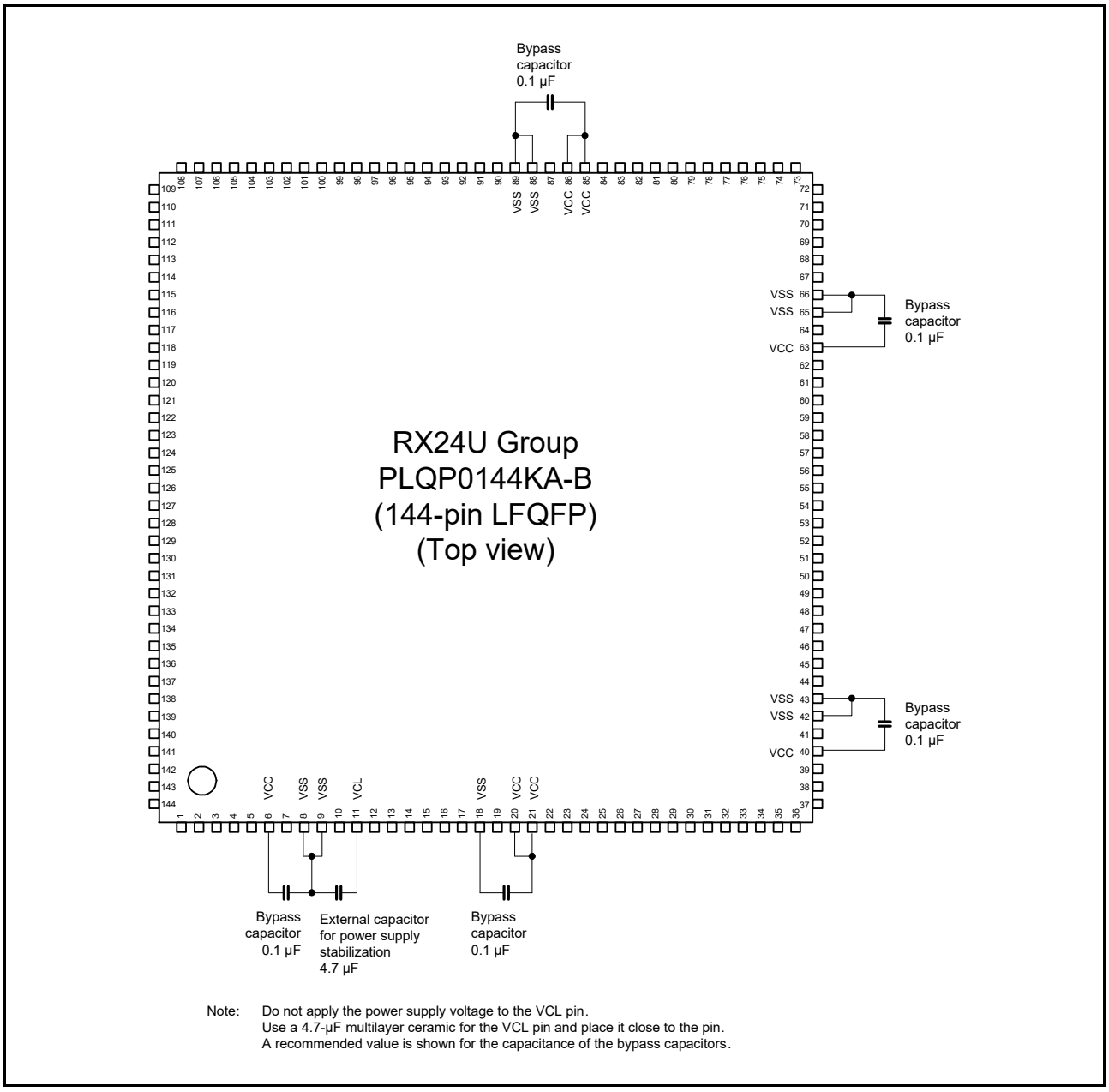

Figure 5.59 Connecting Capacitors (144 Pins)