Renesas Electronics America Inc - R5F524UCADFP#30 Datasheet

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Applications of "Embedded - Microcontrollers"

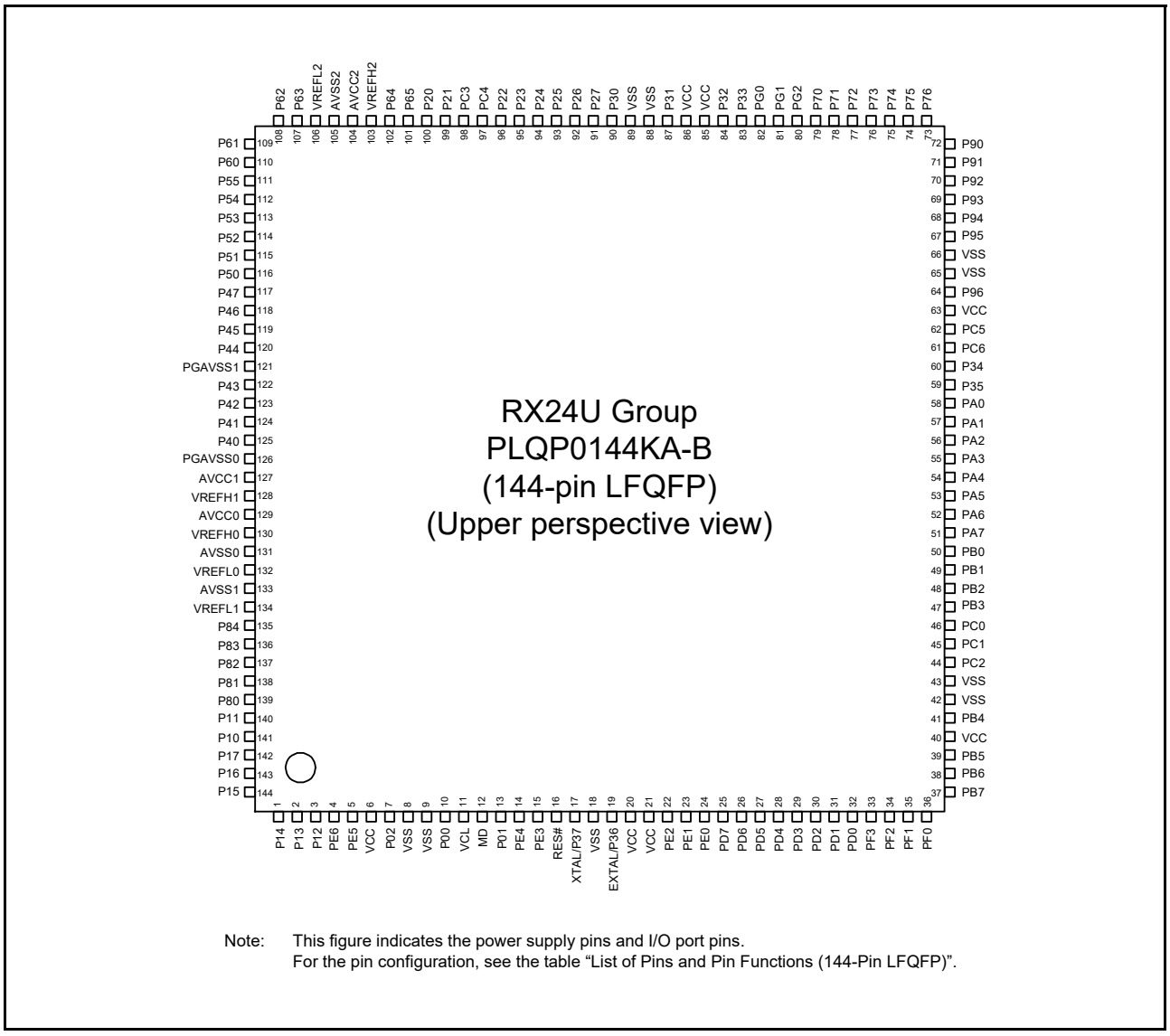
Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	79
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524ucadfp-30

Table 1.1 Outline of Specifications (4/4)

Classification	Module/Function	Description
12-bit A/D converter (S12ADF)		• 12 bits (5 channels × 2 units/12 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.0 µs per channel when the ADCLK is operating at 40 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and 3 group scan mode) Group A priority control (only for 3 group scan mode) • Sampling variable Sampling time can be set up for each channel • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Assist on analog input disconnection detection • A/D conversion start conditions A software trigger, a trigger from a timer (MTU3, GPT, TMR), or an external trigger signal • Sample-and-hold function Sample-and-hold circuit included (3 channels for unit 1) • Amplification of input signals by a programmable gain amplifier (1 channel for unit 0, 3 channels for unit 1) Amplification rate: 2.0 times, 2.5 times, 3.077 times, 3.636 times, 4.0 times, 4.444 times, 5.0 times, 6.667 times, 8.0 times, 10.0 times, 13.333 times (total of 11 steps)
Comparator C (CMPC)		• 4 channels • Function to compare the reference voltage and the analog input voltage • Reference voltage: DA0 or DA1 output is selectable • Analog input voltage is selectable from 4 inputs
8-bit D/A converter (DAa)		• 2 channels • 8-bit resolution • Output voltage: 0 V to AVCC2
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An address exception occurs when the detected access is not in the permitted area.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRC)	• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
	Main clock oscillation stop function	• Main clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, high-speed on-chip oscillator, low-speed on-chip oscillator, the PLL frequency synthesizer, IWDT-dedicated on-chip oscillator, and PCLKB.
	Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data
Power supply voltages/Operating frequencies		VCC = 2.7 to 5.5 V: 80 MHz
Packages		144-pin LFQFP 0.5 mm pitch 100-pin LFQFP 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

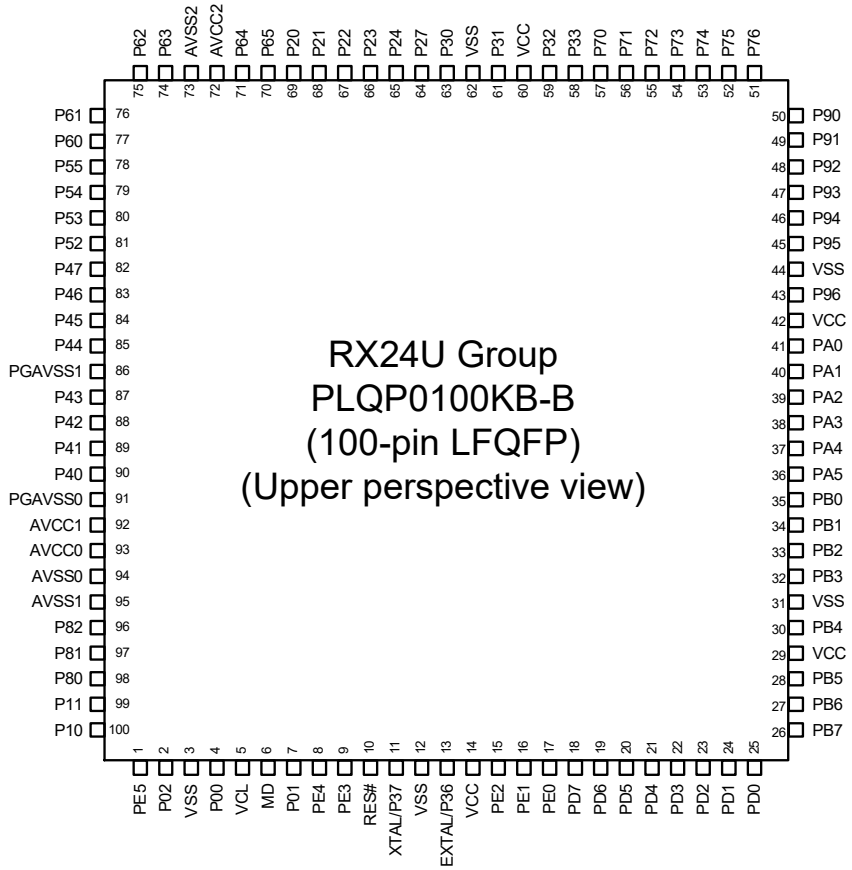
1.5 Pin Assignments

Figure 1.3 and Figure 1.4 show the pin assignments. Table 1.5 and Table 1.6 show the lists of pins and pin functions.



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (144-Pin LFQFP)”.

Figure 1.3 Pin Assignments of the 144-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin LFQFP)”.

Figure 1.4 Pin Assignments of the 100-Pin LFQFP

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU3, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
51		P76	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#		
52		P75	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#		
53		P74	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#		
54		P73	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#		
55		P72	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#		
56		P71	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#		
57		P70	POE0#		IRQ5
58		P33	MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0	SSLA3	
59		P32	MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6	SSLA2	
60	VCC				
61		P31	MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6	SSLA1	IRQ6
62	VSS				
63		P30	MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6	SSLA0	IRQ7, COMP3
64		P27	MTIOC1A, MTIOC1A#		
65		P24	MTIC5U, MTIC5U#, TMCI2, TMO6	RSPCKA	COMP0, DA0
66		P23	MTIC5V, MTIC5V#, TMO2, CACREF	MOSIA	COMP1, DA1
67		P22	MTIC5W, MTIC5W#, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
68		P21	MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCI4		IRQ6, ADTRG1#, AN116
69		P20	MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4		IRQ7, ADTRG0#, AN016
70		P65			AN205
71		P64			AN204
72	AVCC2				
73	AVSS2				
74		P63			AN203, IRQ7
75		P62			AN202, IRQ6
76		P61			AN201, IRQ5
77		P60			AN200, IRQ4
78		P55			AN211, IRQ3
79		P54			AN210, IRQ2
80		P53			AN209, IRQ1
81		P52			AN208, IRQ0
82		P47			AN103
83		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
84		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
85		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
86	PGAVSS1				
87		P43			AN003
88		P42			AN002
89		P41			AN001
90		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
91	PGAVSS0				

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU3, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
92	AVCC1				
93	AVCC0				
94	AVSS0				
95	AVSS1				
96		P82	MTIC5U, MTIC5U#, TMO4	SCK6	
97		P81	MTIC5V, MTIC5V#, TMCI4	TXD6, SMOSI6, SSDA6	
98		P80	MTIC5W, MTIC5W#, TMRI4	RXD6, SMISO6, SSCL6	
99		P11	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3		IRQ1
100		P10	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0

Table 4.1 List of I/O Registers (Address Order) (4/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK
0008 709Fh	ICU	Interrupt Request Register 159	IR159	8	8	2 ICLK
0008 70A0h	ICU	Interrupt Request Register 160	IR160	8	8	2 ICLK
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK
0008 70A9h	ICU	Interrupt Request Register 169	IR169	8	8	2 ICLK
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK
0008 70ACh	ICU	Interrupt Request Register 172	IR172	8	8	2 ICLK
0008 70ADh	ICU	Interrupt Request Register 173	IR173	8	8	2 ICLK
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK
0008 70C0h	ICU	Interrupt Request Register 192	IR192	8	8	2 ICLK
0008 70C1h	ICU	Interrupt Request Register 193	IR193	8	8	2 ICLK
0008 70C2h	ICU	Interrupt Request Register 194	IR194	8	8	2 ICLK
0008 70C3h	ICU	Interrupt Request Register 195	IR195	8	8	2 ICLK
0008 70C4h	ICU	Interrupt Request Register 196	IR196	8	8	2 ICLK
0008 70C5h	ICU	Interrupt Request Register 197	IR197	8	8	2 ICLK
0008 70CAh	ICU	Interrupt Request Register 202	IR202	8	8	2 ICLK
0008 70CBh	ICU	Interrupt Request Register 203	IR203	8	8	2 ICLK
0008 70CCh	ICU	Interrupt Request Register 204	IR204	8	8	2 ICLK
0008 70CDh	ICU	Interrupt Request Register 205	IR205	8	8	2 ICLK
0008 70CEh	ICU	Interrupt Request Register 206	IR206	8	8	2 ICLK
0008 70CFh	ICU	Interrupt Request Register 207	IR207	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 7322h	ICU	Interrupt Source Priority Register 034	IPR034	8	8	2 ICLK
0008 7328h	ICU	Interrupt Source Priority Register 040	IPR040	8	8	2 ICLK
0008 7329h	ICU	Interrupt Source Priority Register 041	IPR041	8	8	2 ICLK
0008 732Ch	ICU	Interrupt Source Priority Register 044	IPR044	8	8	2 ICLK
0008 7330h	ICU	Interrupt Source Priority Register 048	IPR048	8	8	2 ICLK
0008 7331h	ICU	Interrupt Source Priority Register 049	IPR049	8	8	2 ICLK
0008 7332h	ICU	Interrupt Source Priority Register 050	IPR050	8	8	2 ICLK
0008 7333h	ICU	Interrupt Source Priority Register 051	IPR051	8	8	2 ICLK
0008 7334h	ICU	Interrupt Source Priority Register 052	IPR052	8	8	2 ICLK
0008 7335h	ICU	Interrupt Source Priority Register 053	IPR053	8	8	2 ICLK
0008 7336h	ICU	Interrupt Source Priority Register 054	IPR054	8	8	2 ICLK
0008 7337h	ICU	Interrupt Source Priority Register 055	IPR055	8	8	2 ICLK
0008 7338h	ICU	Interrupt Source Priority Register 056	IPR056	8	8	2 ICLK
0008 7339h	ICU	Interrupt Source Priority Register 057	IPR057	8	8	2 ICLK
0008 733Bh	ICU	Interrupt Source Priority Register 059	IPR059	8	8	2 ICLK
0008 733Ch	ICU	Interrupt Source Priority Register 060	IPR060	8	8	2 ICLK
0008 733Dh	ICU	Interrupt Source Priority Register 061	IPR061	8	8	2 ICLK
0008 733Eh	ICU	Interrupt Source Priority Register 062	IPR062	8	8	2 ICLK
0008 733Fh	ICU	Interrupt Source Priority Register 063	IPR063	8	8	2 ICLK
0008 7340h	ICU	Interrupt Source Priority Register 064	IPR064	8	8	2 ICLK
0008 7341h	ICU	Interrupt Source Priority Register 065	IPR065	8	8	2 ICLK
0008 7342h	ICU	Interrupt Source Priority Register 066	IPR066	8	8	2 ICLK
0008 7343h	ICU	Interrupt Source Priority Register 067	IPR067	8	8	2 ICLK
0008 7344h	ICU	Interrupt Source Priority Register 068	IPR068	8	8	2 ICLK
0008 7345h	ICU	Interrupt Source Priority Register 069	IPR069	8	8	2 ICLK
0008 7346h	ICU	Interrupt Source Priority Register 070	IPR070	8	8	2 ICLK
0008 7347h	ICU	Interrupt Source Priority Register 071	IPR071	8	8	2 ICLK
0008 7358h	ICU	Interrupt Source Priority Register 088	IPR088	8	8	2 ICLK
0008 7359h	ICU	Interrupt Source Priority Register 089	IPR089	8	8	2 ICLK
0008 7362h	ICU	Interrupt Source Priority Register 098	IPR098	8	8	2 ICLK
0008 7363h	ICU	Interrupt Source Priority Register 099	IPR099	8	8	2 ICLK
0008 7364h	ICU	Interrupt Source Priority Register 100	IPR100	8	8	2 ICLK
0008 7365h	ICU	Interrupt Source Priority Register 101	IPR101	8	8	2 ICLK
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK
0008 7368h	ICU	Interrupt Source Priority Register 104	IPR104	8	8	2 ICLK
0008 7369h	ICU	Interrupt Source Priority Register 105	IPR105	8	8	2 ICLK
0008 736Ah	ICU	Interrupt Source Priority Register 106	IPR106	8	8	2 ICLK
0008 736Bh	ICU	Interrupt Source Priority Register 107	IPR107	8	8	2 ICLK
0008 736Ch	ICU	Interrupt Source Priority Register 108	IPR108	8	8	2 ICLK
0008 736Dh	ICU	Interrupt Source Priority Register 109	IPR109	8	8	2 ICLK
0008 736Eh	ICU	Interrupt Source Priority Register 110	IPR110	8	8	2 ICLK
0008 736Fh	ICU	Interrupt Source Priority Register 111	IPR111	8	8	2 ICLK
0008 7370h	ICU	Interrupt Source Priority Register 112	IPR112	8	8	2 ICLK
0008 7371h	ICU	Interrupt Source Priority Register 113	IPR113	8	8	2 ICLK
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK
0008 7376h	ICU	Interrupt Source Priority Register 118	IPR118	8	8	2 ICLK
0008 7379h	ICU	Interrupt Source Priority Register 121	IPR121	8	8	2 ICLK
0008 737Bh	ICU	Interrupt Source Priority Register 123	IPR123	8	8	2 ICLK
0008 737Dh	ICU	Interrupt Source Priority Register 125	IPR125	8	8	2 ICLK
0008 737Fh	ICU	Interrupt Source Priority Register 127	IPR127	8	8	2 ICLK
0008 7381h	ICU	Interrupt Source Priority Register 129	IPR129	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (12/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8219h	TMR3	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8220h	TMR4	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8221h	TMR5	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8222h	TMR4	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8223h	TMR5	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8224h	TMR4	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8225h	TMR5	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8226h	TMR4	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8227h	TMR5	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8228h	TMR4	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8229h	TMR5	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 822Ah	TMR4	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 822Bh	TMR5	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8230h	TMR6	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8231h	TMR7	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8232h	TMR6	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8233h	TMR7	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8234h	TMR6	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8235h	TMR7	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8236h	TMR6	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8237h	TMR7	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8238h	TMR6	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8239h	TMR7	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 823Ah	TMR6	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 823Bh	TMR7	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB
0008 8300h	RIIC0	I^2C-bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB
0008 8301h	RIIC0	I^2C-bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB
0008 8302h	RIIC0	I^2C-bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB
0008 8303h	RIIC0	I^2C-bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB
0008 8304h	RIIC0	I^2C-bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB
0008 8305h	RIIC0	I^2C-bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB
0008 8306h	RIIC0	I^2C-bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB
0008 8307h	RIIC0	I^2C-bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB
0008 8308h	RIIC0	I^2C-bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB
0008 8309h	RIIC0	I^2C-bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (14/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 9086h	S12AD	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB
0008 90D4h	S12AD	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB
0008 90D6h	S12AD	A/D Channel Select Register C1	ADANSC1	16	16	2 or 3 PCLKB
0008 90D9h	S12AD	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB
0008 90DDh	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 91A0h	S12AD	A/D Programmable Gain Amplifier Control Register	ADPGACR	16	16	2 or 3 PCLKB
0008 91A2h	S12AD	A/D Programmable Gain Amplifier Gain Setting Register 0	ADPGAGS0	16	16	2 or 3 PCLKB
0008 9200h	S12AD1	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9204h	S12AD1	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9206h	S12AD1	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB
0008 9208h	S12AD1	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 920Ah	S12AD1	A/D-Converted Value Addition/Average Function Channel Select Register 1	ADADS1	16	16	2 or 3 PCLKB
0008 920Ch	S12AD1	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 920Eh	S12AD1	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9210h	S12AD1	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9214h	S12AD1	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9216h	S12AD1	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB
0008 9218h	S12AD1	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 921Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9220h	S12AD1	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9222h	S12AD1	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9224h	S12AD1	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9226h	S12AD1	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9240h	S12AD1	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB
0008 9266h	S12AD1	A/D Sample-and-hold Circuit Control Register	ADSHCR	16	16	2 or 3 PCLKB
0008 927Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 9280h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 9284h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB
0008 9286h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB
0008 92D4h	S12AD1	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB
0008 92D6h	S12AD1	A/D Channel Select Register C1	ADANSC1	16	16	2 or 3 PCLKB
0008 92D9h	S12AD1	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB
0008 92DDh	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 92E0h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 92E1h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 92E2h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 92E3h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 93A0h	S12AD1	A/D Programmable Gain Amplifier Control Register	ADPGACR	16	16	2 or 3 PCLKB
0008 93A2h	S12AD1	A/D Programmable Gain Amplifier Gain Setting Register 0	ADPGAGS0	16	16	2 or 3 PCLKB
0008 9400h	S12AD2	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9404h	S12AD2	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9408h	S12AD2	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 940Ch	S12AD2	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 940Eh	S12AD2	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9410h	S12AD2	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (23/40)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 C4F2h	POE	Port Mode Mask Control Register 1	PMMCR1	16	16	2 or 3 PCLKB
0008 C4F4h	POE	Port Mode Mask Control Register 2	PMMCR2	16	16	2 or 3 PCLKB
0008 C4F6h	POE	Port Mode Mask Control Register 3	PMMCR3	16	16	2 or 3 PCLKB
0008 C4F8h	POE	Port Output Enable Comparator Request Extended Selection Register 0	POECMPEX0	8	8	2 or 3 PCLKB
0008 C4F9h	POE	Port Output Enable Comparator Request Extended Selection Register 1	POECMPEX1	8	8	2 or 3 PCLKB
0008 C4FAh	POE	Port Output Enable Comparator Request Extended Selection Register 2	POECMPEX2	8	8	2 or 3 PCLKB
0008 C4FBh	POE	Port Output Enable Comparator Request Extended Selection Register 3	POECMPEX3	8	8	2 or 3 PCLKB
0008 C4FCh	POE	Port Output Enable Comparator Request Extended Selection Register 4	POECMPEX4	8	8	2 or 3 PCLKB
0008 C4FDh	POE	Port Output Enable Comparator Request Extended Selection Register 5	POECMPEX5	8	8	2 or 3 PCLKB
000A 0C80h	CMPC0	Comparator Control Register 0	CMPCTL	8	8	1 or 2 PCLKB
000A 0C84h	CMPC0	Comparator Input Select Register 0	CMPSEL0	8	8	1 or 2 PCLKB
000A 0C88h	CMPC0	Comparator Reference Voltage Select Register 0	CMPSEL1	8	8	1 or 2 PCLKB
000A 0C8Ch	CMPC0	Comparator Output Monitor Register 0	CMPMON	8	8	1 or 2 PCLKB
000A 0C90h	CMPC0	Comparator External Output Enable Register 0	CMPIOC	8	8	1 or 2 PCLKB
000A 0CA0h	CMPC1	Comparator Control Register 1	CMPCTL	8	8	1 or 2 PCLKB
000A 0CA4h	CMPC1	Comparator Input Select Register 1	CMPSEL0	8	8	1 or 2 PCLKB
000A 0CA8h	CMPC1	Comparator Reference Voltage Select Register 1	CMPSEL1	8	8	1 or 2 PCLKB
000A 0CACh	CMPC1	Comparator Output Monitor Register 1	CMPMON	8	8	1 or 2 PCLKB
000A 0CB0h	CMPC1	Comparator External Output Enable Register 1	CMPIOC	8	8	1 or 2 PCLKB
000A 0CC0h	CMPC2	Comparator Control Register 2	CMPCTL	8	8	1 or 2 PCLKB
000A 0CC4h	CMPC2	Comparator Input Select Register 2	CMPSEL0	8	8	1 or 2 PCLKB
000A 0CC8h	CMPC2	Comparator Reference Voltage Select Register 2	CMPSEL1	8	8	1 or 2 PCLKB
000A 0CCCh	CMPC2	Comparator Output Monitor Register 2	CMPMON	8	8	1 or 2 PCLKB
000A 0CD0h	CMPC2	Comparator External Output Enable Register 2	CMPIOC	8	8	1 or 2 PCLKB
000A 0CE0h	CMPC3	Comparator Control Register 3	CMPCTL	8	8	1 or 2 PCLKB
000A 0CE4h	CMPC3	Comparator Input Select Register 3	CMPSEL0	8	8	1 or 2 PCLKB
000A 0CE8h	CMPC3	Comparator Reference Voltage Select Register 3	CMPSEL1	8	8	1 or 2 PCLKB
000A 0CECh	CMPC3	Comparator Output Monitor Register 3	CMPMON	8	8	1 or 2 PCLKB
000A 0CF0h	CMPC3	Comparator External Output Enable Register 3	CMPIOC	8	8	1 or 2 PCLKB
000A 8300h	RSCAN0	Bit Configuration Register L	CFGL	16	16	2 or 3 PCLKB
000A 8302h	RSCAN0	Bit Configuration Register H	CFGH	16	16	2 or 3 PCLKB
000A 8304h	RSCAN0	Control Register L	CTRL	16	16	2 or 3 PCLKB
000A 8306h	RSCAN0	Control Register H	CTRH	16	16	2 or 3 PCLKB
000A 8308h	RSCAN0	Status Register L	STSL	16	16	2 or 3 PCLKB
000A 830Ah	RSCAN0	Status Register H	STSH	16	16	2 or 3 PCLKB
000A 830Ch	RSCAN0	Error Flag Register L	ERFLL	16	16	2 or 3 PCLKB
000A 830Eh	RSCAN0	Error Flag Register H	ERFLH	16	16	2 or 3 PCLKB
000A 8322h	RSCAN	Global Configuration Register L	GCFGL	16	16	2 or 3 PCLKB
000A 8324h	RSCAN	Global Configuration Register H	GCFGH	16	16	2 or 3 PCLKB
000A 8326h	RSCAN	Global Control Register L	GCTRL	16	16	2 or 3 PCLKB
000A 8328h	RSCAN	Global Control Register H	GCTRH	16	16	2 or 3 PCLKB
000A 832Ah	RSCAN	Global Status Register	GSTS	16	16	2 or 3 PCLKB
000A 832Ch	RSCAN	Global Error Flag Register	GERFLL	8	8	1 or 2 PCLKB
000A 832Eh	RSCAN	Timestamp Register	GTSC	16	16	2 or 3 PCLKB
000A 8330h	RSCAN	Receive Rule Number Configuration Register	GAFLCFG	16	16	2 or 3 PCLKB
000A 8332h	RSCAN	Receive Buffer Number Configuration Register	RMNB	16	16	2 or 3 PCLKB
000A 8334h	RSCAN	Receive Buffer Receive Complete Flag Register	RMND0	16	16	2 or 3 PCLKB
000A 8338h	RSCAN	Receive FIFO Control Register 0	RFCC0	16	16	2 or 3 PCLKB

Table 5.6 DC Characteristics (4)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	1.5	15.0	µA	
		T_a = 55°C		3.0	38.0		
		T_a = 85°C		13.0	135.0		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 5 V.

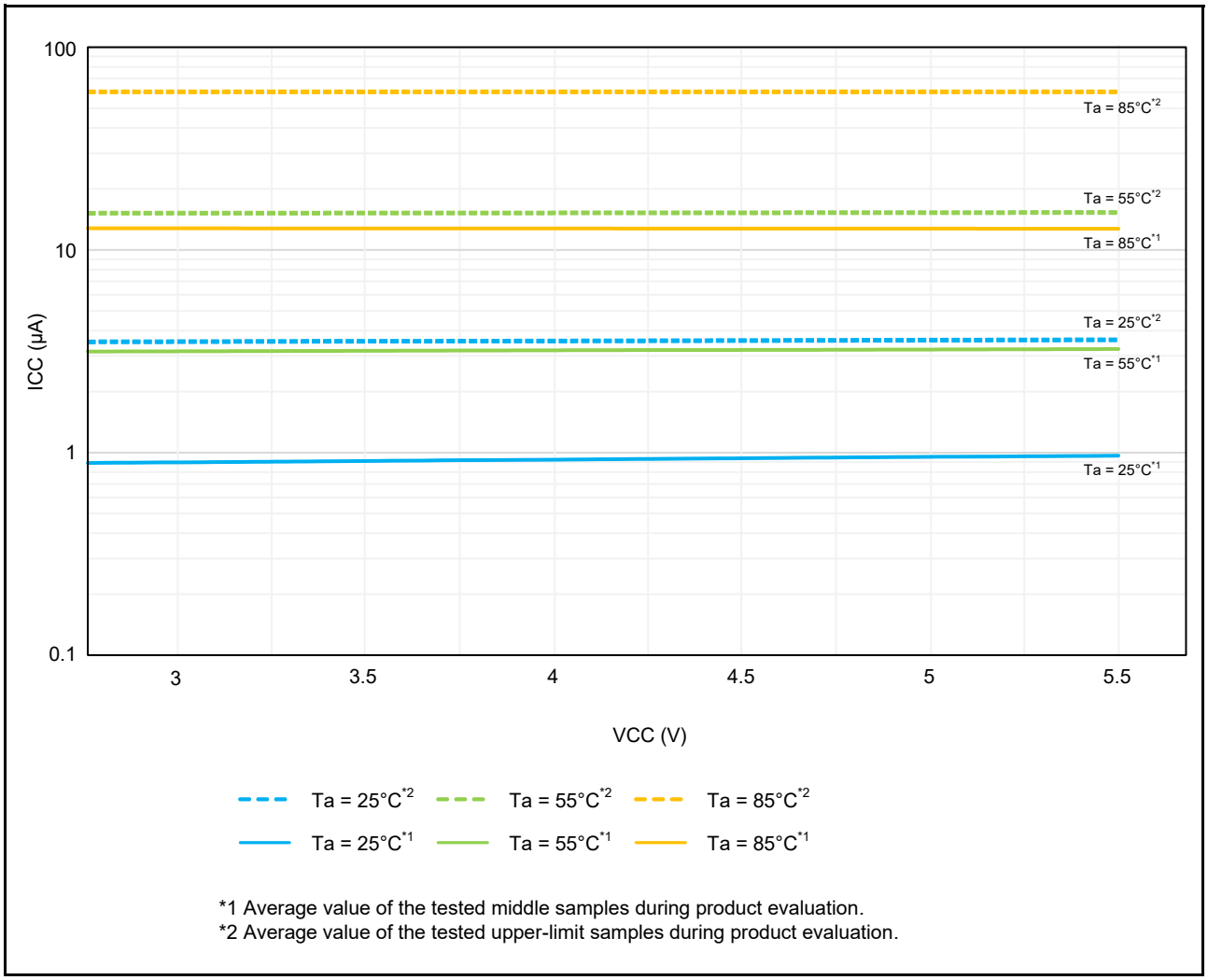


Figure 5.1 Voltage Dependency in Software Standby Mode (Reference Data)

Table 5.8 DC Characteristics (6)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0V, T_a = –40 to +85°C

Item			Symbol	Min.	Typ.*2	Max.	Unit	Test Conditions
Analog power supply current	A/D unit 0	During A/D conversion (programmable gain amplifier in use)	I_{AVCC}	—	1.5	2.5	mA	
		During A/D conversion (programmable gain amplifier not in use)		—	1.0	1.8		
	A/D unit 1	During A/D conversion (sample-and-hold circuits in use, programmable gain amplifier in use)		—	4.6	6.9		
		During A/D conversion (sample-and-hold circuits in use, programmable gain amplifier not in use)		—	3.1	4.8		
		During A/D conversion (sample-and-hold circuits not in use, programmable gain amplifier in use)		—	2.5	3.9		
		During A/D conversion (sample-and-hold circuits not in use, programmable gain amplifier not in use)		—	1.0	1.8		
	A/D unit 2			—	1.0	1.8		
	During D/A conversion (per 1 channel)*1			—	0.7	1.0		
	Waiting for A/D or D/A conversion (all units)			—	—	2.2	μA	
Reference power supply current	During A/D conversion (at high-speed conversion per 1 unit)		I_{REFH}	—	10.0	20.0	μA	
	Waiting for A/D conversion (all units)			—	—	180.0	nA	
Comparator C operating current*3	Comparator enabled		I_{CMP}	—	40.0	60.0	μA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.
Note 2. When VCC =AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = 5 V.
Note 3. Current consumed only by the comparator C module.

Table 5.9 DC Characteristics (7)

Conditions: VCC = 0 V to AVCC0, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = 0 V to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup	SrVCC	0.02	—	20	ms/V	
	Voltage monitoring 0 reset enabled at startup*1, *2		0.02	—	—		

Note 1. When OFS1.LVDAS = 0.
Note 2. Turn on the power supply voltage according to the normal startup rising gradient because the register settings set by OFS1 are not read in boot mode.

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.18 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.30
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	35	50	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	70	95	µs	
		HOCO clock operation	HOCO clock oscillator operation 1 *6	t_{SBYHO}	—	40	55	µs	
			HOCO clock oscillator operation 2 *7		—	75	90	µs	
			HOCO clock oscillator, PLL circuit operation*8	t_{SBYPH}	—	110	130	µs	
		LOCO clock oscillator operating*9		t_{SBYLO}	—	40	55	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of crystal is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 3. When the frequency of PLL is 80 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK and PCLKA are set to 80 MHz, PCLKB and PCLKD are set to 40 MHz, and FCLK is set to 20 MHz.

Note 4. When the frequency of the external clock is 20 MHz.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 5. When the frequency of PLL is 80 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
When the frequencies of ICLK and PCLKA are set to 80 MHz, PCLKB and PCLKD are set to 40 MHz, and FCLK is set to 20 MHz.

Note 6. When the frequency of the high-speed on-chip oscillator is 32 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 7. When the frequency of the high-speed on-chip oscillator is 64 MHz. Set the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 06h. When the frequencies of ICLK and PCLKA are set to 64 MHz, and the frequencies of PCLKB, PCLKD, and FCLK are set to 32 MHz.

Note 8. When the frequency of the high-speed on-chip oscillator is 32 MHz, and the frequency of PLL is 80 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK and PCLKA are set to 80 MHz, the frequencies of PCLKB and PCLKD are set to 40 MHz, and the frequency of FCLK is set to 20MHz.

Note 9. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Table 5.27 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C, C = 30 pF

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI (SCI11)	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.45
	SCK clock cycle input (slave)			6	—	t_{Pcyc}	
	SCK clock output frequency (master)		f_{SPcyc}	—	10	MHz	
	SCK clock input frequency (slave)			—	6.67	MHz	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	VCC = 4.0 V or above	t_{SU}	40	—	ns	Figure 5.46, Figure 5.47
		VCC = 2.7 V or above		65	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SS input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	VCC = 4.0 V or above		—	40		
		VCC = 2.7 V or above		—	65		
	Data output hold time	Master	t_{OH}	–10	—	ns	
		Slave		–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	PCLKA ≤ 40MHz	t_{SA}	—	6	t_{PAcyc}	Figure 5.48, Figure 5.49
		PCLKA > 40MHz		—	12	t_{PAcyc}	
	Slave output release time	PCLKA ≤ 40MHz	t_{REL}	—	6	t_{PAcyc}	
		PCLKA > 40MHz		—	12	t_{PAcyc}	

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcyc}: PCLKA cycle

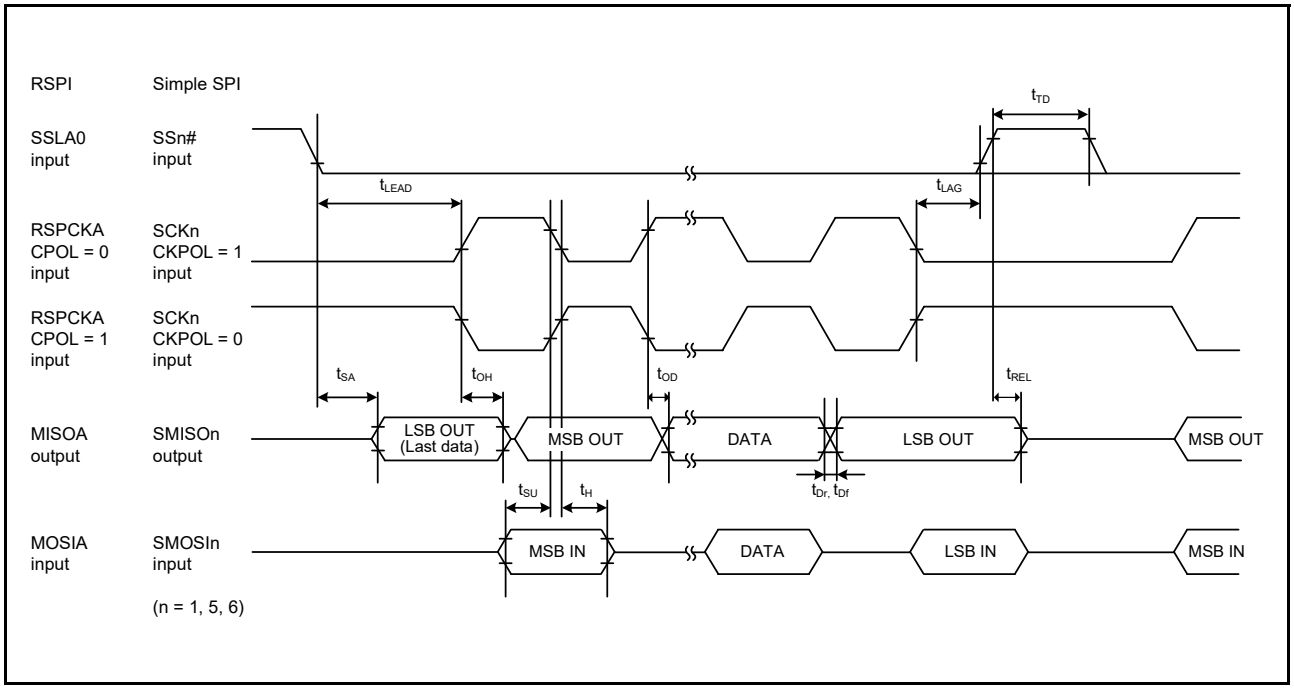
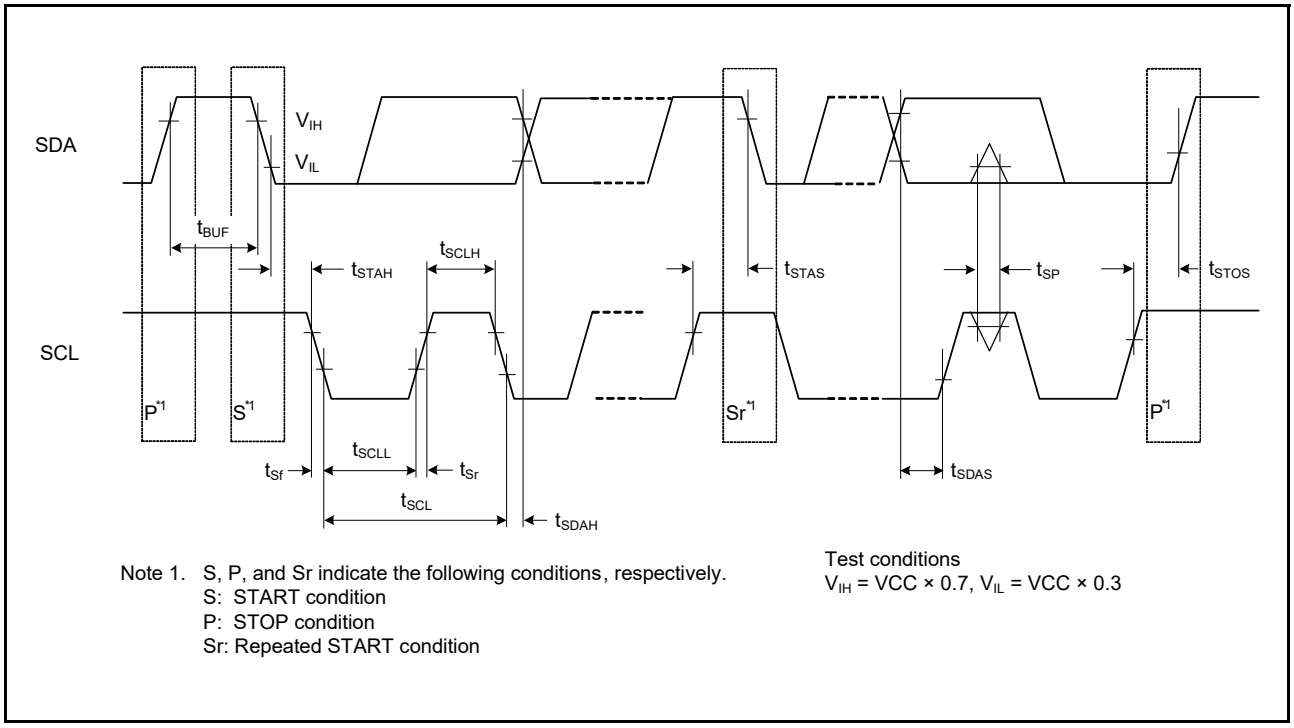


Figure 5.49 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3

Figure 5.50 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

Table 5.31 A/D Conversion Characteristics (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	40	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 40 MHz)	Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit not in use	1.15	—	—	µs	High-precision channel ADSSTRn.SST[7:0] bits = 0Eh
		1.30	—	—	µs	Normal-precision channel ADSSTRn.SST[7:0] bits = 14h
	Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit in use	1.90	—	—	µs	High-precision channel ADSSTRn.SST[7:0] bits = 0Eh ADSHCR.SSTSH[7:0] bits = 11h AN100 to 102 = 0.25 V to AVCC1 – 0.25 V
Analog input capacitance		—	—	12	pF	
Offset error		—	±2.0	±6.5	LSB	
Full-scale error		—	±2.0	±6.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±0.5	±1.5	LSB	
INL integral nonlinearity error		—	±1.5	±4.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.32 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN003, AN100 to AN103, AN200 to AN211	AVCC0 = AVCC1 = AVCC2 = 2.7 to 5.5 V	
Normal-precision channel	AN016, AN116	VCC = AVCC0 = AVCC1 =AVCC2 = 2.7 to 5.5 V	
Internal reference voltage input channel	Internal reference voltage	AVCC0 = AVCC1 = AVCC2 = 2.7 to 5.5 V	

Table 5.33 A/D Internal Reference Voltage Characteristics

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Internal reference voltage input channel*1	1.35	1.43	1.50	V	

Note 1. The A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the A/D converter.

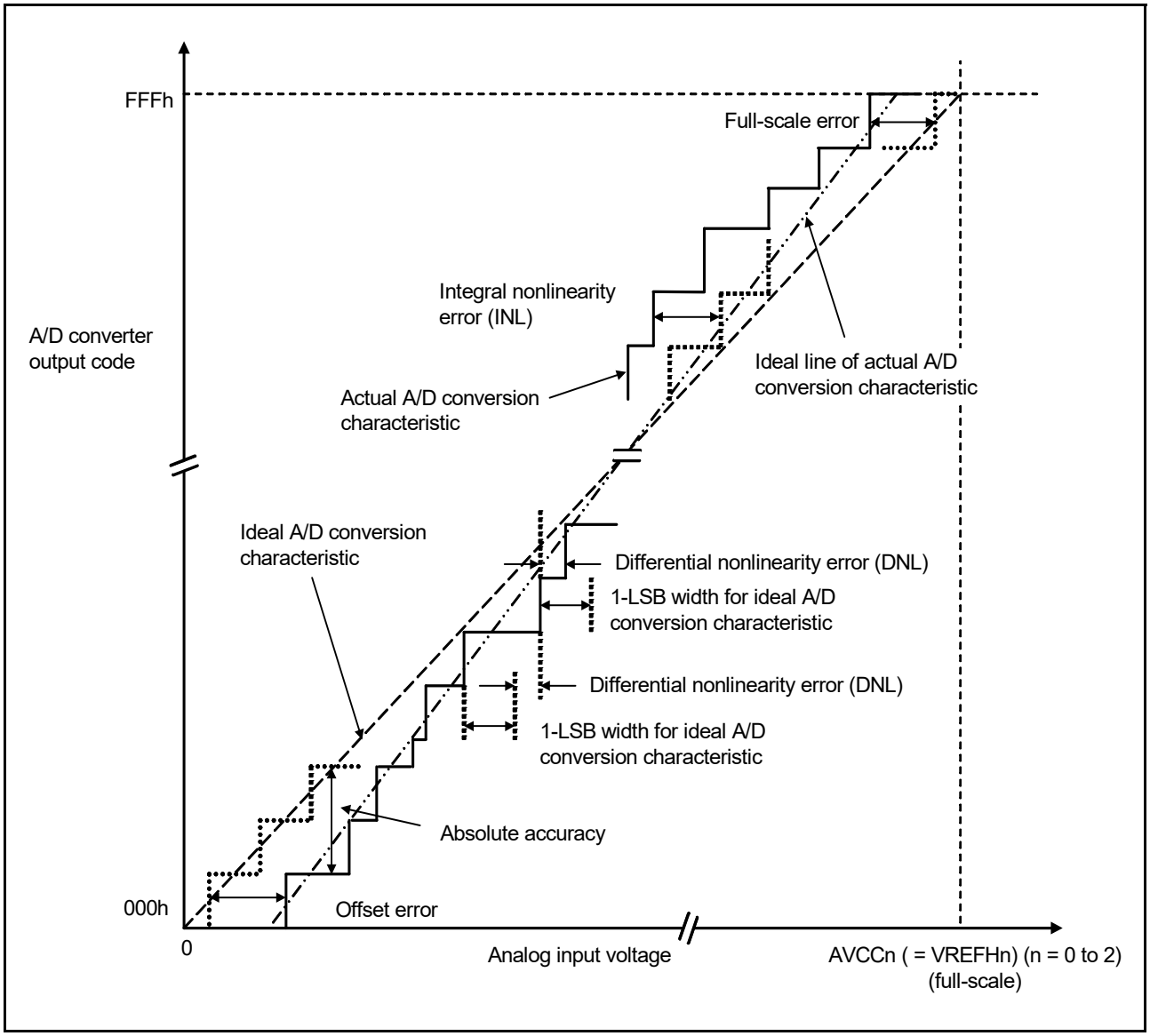


Figure 5.51 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (AVCCn (= VREFHn) (n = 0 to 2)) is 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

5.6 Comparator Characteristics

Table 5.35 Comparator Characteristics

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Offset voltage	V_{cioff}	—	—	40	mV	
Response time	t_{cr}	—	—	200	ns	VOD = 100 mV CMPCTL.CDFS = 0
	t_{cf}	—	—	200	ns	
Stabilization wait time for input selection	t_{cwait}	300	—	—	ns	
Operation stabilization wait time	t_{cmp}		—	1	µs	

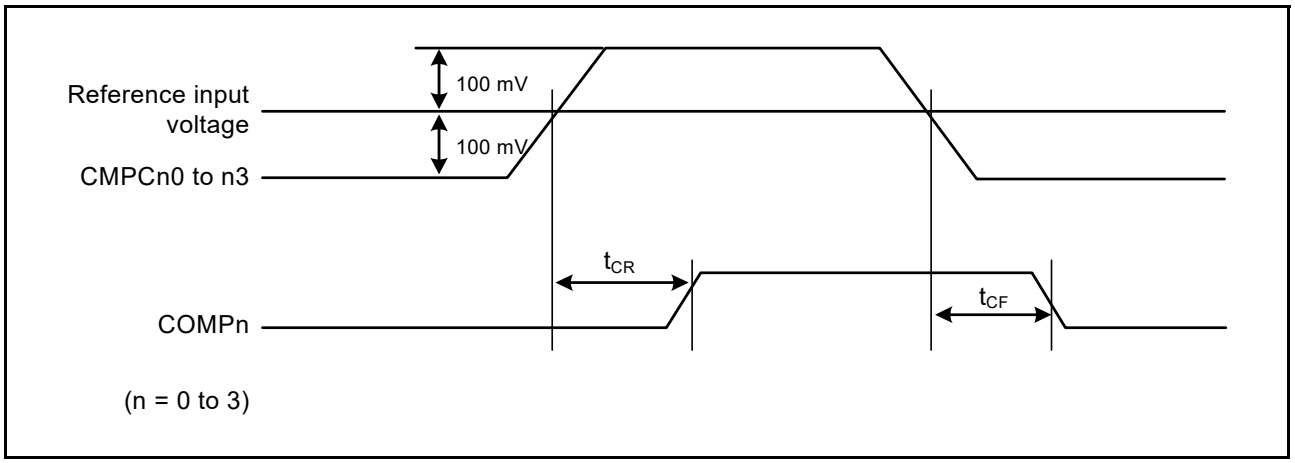


Figure 5.52 Comparator Response Time

5.10 ROM (Flash Memory for Code Storage) Characteristics

Table 5.40 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	—	—	Year	T_a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 5.41 ROM (Flash Memory for Code Storage) Characteristics (2): High-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V

Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	112.0	967.0	—	52.3	490.5	µs
Erasure time	2-Kbyte	t_{E2K}	—	8.7	278.1	—	5.5	214.6	ms
	512-Kbyte (when block erase command used)	t_{E512K}	—	927.8	19218.0	—	72.0	1678.9	ms
	512-Kbyte (when all-block erase command used)	t_{EA512K}	—	922.7	19013.4	—	66.7	1469.2	ms
Blank check time	8-byte	t_{BC8}	—	—	55.0	—	—	16.1	µs
	2-Kbyte	t_{BC2K}	—	—	1840.0	—	—	135.7	µs
Erase operation forcible stop time		t_{SED}	—	—	18.0	—	—	10.7	µs
Start-up area switching setting time		t_{SAS}	—	12.3	566.5	—	6.2	433.5	ms
Access window time		t_{AWS}	—	12.3	566.5	—	6.2	433.5	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	µs
ROM mode transition wait time 2		t_{MS}	5.0	—	—	5.0	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.