# Renesas Electronics America Inc - R5F524UEADFP#30 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RXv2 |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, I²C, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 110 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 22x12b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LFQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524ueadfp-30 |

**Table 1.2 Comparison of Functions for Different Packages**

| Module/Functions | | RX24U Group | |
|---|---|---|---|
| | | 144 Pins | 100 Pins |
| Memory | ROM | 512 Kbytes | |
| | RAM | 32 Kbytes | |
| | E2 Data Flash | 8 Kbytes | |
| Interrupts | External interrupts | NMI, IRQ0 to IRQ7 | |
| DTC | Data transfer controller (DTCa) | Available | |
| Timers | Multi-function timer pulse unit 3 (MTU3d) | 9 channels | |
| | General PWM timer (GPTB) | 4 channels | |
| | Port output enable 3 (POE3A) | POE0#, POE4#, POE8#, POE10#, POE11#, POE12# | |
| | 8-bit timer (TMR) | 2 channels × 4 units | |
| | Compare match timer (CMT) | 2 channels × 2 units | |
| | Independent watchdog timer (IWDTa) | Available | |
| Communication functions | Serial communications interfaces (SCIg) [including simple $I^2C$ and simple SPI] | 6 channels (SCI1, 5, 6, 8, 9, 11) | 4 channels (SCI1, 5, 6, 11) |
| | $I^2C$ bus interface (RIICa) | 1 channel | |
| | Serial peripheral interface (RSPIb) | 1 channel | |
| | CAN module (RSCAN) | 1 channel | |
| 12-bit A/D converter (including high-precision channels) (S12ADF) | | 5 channels × 2 units, 12 channels × 1 unit (4 channels × 2 units, 12 channels × 1 unit) | 5 channels × 2 units, 10 channels × 1 unit (4 channels × 2 units, 10 channels × 1 unit) |
| | 3 channels simultaneous sampling function | 3 channels/unit 1 | |
| | Programmable gain amplifier | 1 channel/unit 0, 3 channels/unit 1 | |
| Comparator C (CMPC) | | 4 channels | |
| D/A converter (DAa) | | 2 channels | |
| CRC calculator (CRC) | | Available | |
| Packages | | 144-pin LFQFP | 100-pin LFQFP |

**Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP) (2/3)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | Timers (TMR, MTU3, POE, CAC, GPT) | Communications (SCI, RSPI, RIIC, RSCAN) | Others |
|---|---|---|---|---|---|
| 51 | | P76 | MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B# | | |
| 52 | | P75 | MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B# | | |
| 53 | | P74 | MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B# | | |
| 54 | | P73 | MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A# | | |
| 55 | | P72 | MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A# | | |
| 56 | | P71 | MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A# | | |
| 57 | | P70 | POE0# | | IRQ5 |
| 58 | | P33 | MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0 | SSLA3 | |
| 59 | | P32 | MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6 | SSLA2 | |
| 60 | VCC | | | | |
| 61 | | P31 | MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6 | SSLA1 | IRQ6 |
| 62 | VSS | | | | |
| 63 | | P30 | MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6 | SSLA0 | IRQ7, COMP3 |
| 64 | | P27 | MTIOC1A, MTIOC1A# | | |
| 65 | | P24 | MTIC5U, MTIC5U#, TMCI2, TMO6 | RSPCKA | COMP0, DA0 |
| 66 | | P23 | MTIC5V, MTIC5V#, TMO2, CACREF | MOSIA | COMP1, DA1 |
| 67 | | P22 | MTIC5W, MTIC5W#, TMRI2, TMO4 | MISOA | ADTRG2#, COMP2 |
| 68 | | P21 | MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCI4 | | IRQ6, ADTRG1#, AN116 |
| 69 | | P20 | MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4 | | IRQ7, ADTRG0#, AN016 |
| 70 | | P65 | | | AN205 |
| 71 | | P64 | | | AN204 |
| 72 | AVCC2 | | | | |
| 73 | AVSS2 | | | | |
| 74 | | P63 | | | AN203, IRQ7 |
| 75 | | P62 | | | AN202, IRQ6 |
| 76 | | P61 | | | AN201, IRQ5 |
| 77 | | P60 | | | AN200, IRQ4 |
| 78 | | P55 | | | AN211, IRQ3 |
| 79 | | P54 | | | AN210, IRQ2 |
| 80 | | P53 | | | AN209, IRQ1 |
| 81 | | P52 | | | AN208, IRQ0 |
| 82 | | P47 | | | AN103 |
| 83 | | P46 | | | AN102, CMPC12, CMPC13, CMPC30, CMPC31 |
| 84 | | P45 | | | AN101, CMPC02, CMPC03, CMPC20, CMPC21 |
| 85 | | P44 | | | AN100, CMPC10, CMPC11, CMPC32, CMPC33 |
| 86 | PGAVSS1 | | | | |
| 87 | | P43 | | | AN003 |
| 88 | | P42 | | | AN002 |
| 89 | | P41 | | | AN001 |
| 90 | | P40 | | | AN000, CMPC00, CMPC01, CMPC22, CMPC23 |
| 91 | PGAVSS0 | | | | |

**Table 4.1 List of I/O Registers (Address Order) (7/40)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles ICLK ≥ PCLK |
|---|---|---|---|---|---|---|
| 0008 718Dh | ICU | DTC Transfer Request Enable Register 141 | DTCER141 | 8 | 8 | 2 ICLK |
| 0008 718Eh | ICU | DTC Transfer Request Enable Register 142 | DTCER142 | 8 | 8 | 2 ICLK |
| 0008 718Fh | ICU | DTC Transfer Request Enable Register 143 | DTCER143 | 8 | 8 | 2 ICLK |
| 0008 7190h | ICU | DTC Transfer Request Enable Register 144 | DTCER144 | 8 | 8 | 2 ICLK |
| 0008 7191h | ICU | DTC Transfer Request Enable Register 145 | DTCER145 | 8 | 8 | 2 ICLK |
| 0008 7195h | ICU | DTC Transfer Request Enable Register 149 | DTCER149 | 8 | 8 | 2 ICLK |
| 0008 7196h | ICU | DTC Transfer Request Enable Register 150 | DTCER150 | 8 | 8 | 2 ICLK |
| 0008 7197h | ICU | DTC Transfer Request Enable Register 151 | DTCER151 | 8 | 8 | 2 ICLK |
| 0008 7198h | ICU | DTC Transfer Request Enable Register 152 | DTCER152 | 8 | 8 | 2 ICLK |
| 0008 7199h | ICU | DTC Transfer Request Enable Register 153 | DTCER153 | 8 | 8 | 2 ICLK |
| 0008 719Fh | ICU | DTC Transfer Request Enable Register 159 | DTCER159 | 8 | 8 | 2 ICLK |
| 0008 71A0h | ICU | DTC Transfer Request Enable Register 160 | DTCER160 | 8 | 8 | 2 ICLK |
| 0008 71A1h | ICU | DTC Transfer Request Enable Register 161 | DTCER161 | 8 | 8 | 2 ICLK |
| 0008 71A2h | ICU | DTC Transfer Request Enable Register 162 | DTCER162 | 8 | 8 | 2 ICLK |
| 0008 71ADh | ICU | DTC Transfer Request Enable Register 173 | DTCER173 | 8 | 8 | 2 ICLK |
| 0008 71AEh | ICU | DTC Transfer Request Enable Register 174 | DTCER174 | 8 | 8 | 2 ICLK |
| 0008 71AFh | ICU | DTC Transfer Request Enable Register 175 | DTCER175 | 8 | 8 | 2 ICLK |
| 0008 71B1h | ICU | DTC Transfer Request Enable Register 177 | DTCER177 | 8 | 8 | 2 ICLK |
| 0008 71B2h | ICU | DTC Transfer Request Enable Register 178 | DTCER178 | 8 | 8 | 2 ICLK |
| 0008 71B4h | ICU | DTC Transfer Request Enable Register 180 | DTCER180 | 8 | 8 | 2 ICLK |
| 0008 71B5h | ICU | DTC Transfer Request Enable Register 181 | DTCER181 | 8 | 8 | 2 ICLK |
| 0008 71B7h | ICU | DTC Transfer Request Enable Register 183 | DTCER183 | 8 | 8 | 2 ICLK |
| 0008 71B8h | ICU | DTC Transfer Request Enable Register 184 | DTCER184 | 8 | 8 | 2 ICLK |
| 0008 71BAh | ICU | DTC Transfer Request Enable Register 186 | DTCER186 | 8 | 8 | 2 ICLK |
| 0008 71BBh | ICU | DTC Transfer Request Enable Register 187 | DTCER187 | 8 | 8 | 2 ICLK |
| 0008 71BDh | ICU | DTC Transfer Request Enable Register 189 | DTCER189 | 8 | 8 | 2 ICLK |
| 0008 71BEh | ICU | DTC Transfer Request Enable Register 190 | DTCER190 | 8 | 8 | 2 ICLK |
| 0008 71C0h | ICU | DTC Transfer Request Enable Register 192 | DTCER192 | 8 | 8 | 2 ICLK |
| 0008 71C1h | ICU | DTC Transfer Request Enable Register 193 | DTCER193 | 8 | 8 | 2 ICLK |
| 0008 71C3h | ICU | DTC Transfer Request Enable Register 195 | DTCER195 | 8 | 8 | 2 ICLK |
| 0008 71C4h | ICU | DTC Transfer Request Enable Register 196 | DTCER196 | 8 | 8 | 2 ICLK |
| 0008 71CBh | ICU | DTC Transfer Request Enable Register 203 | DTCER203 | 8 | 8 | 2 ICLK |
| 0008 71CCh | ICU | DTC Transfer Request Enable Register 204 | DTCER204 | 8 | 8 | 2 ICLK |
| 0008 71CDh | ICU | DTC Transfer Request Enable Register 205 | DTCER205 | 8 | 8 | 2 ICLK |
| 0008 71CEh | ICU | DTC Transfer Request Enable Register 206 | DTCER206 | 8 | 8 | 2 ICLK |
| 0008 71CFh | ICU | DTC Transfer Request Enable Register 207 | DTCER207 | 8 | 8 | 2 ICLK |
| 0008 71D0h | ICU | DTC Transfer Request Enable Register 208 | DTCER208 | 8 | 8 | 2 ICLK |
| 0008 71D1h | ICU | DTC Transfer Request Enable Register 209 | DTCER209 | 8 | 8 | 2 ICLK |
| 0008 71D2h | ICU | DTC Transfer Request Enable Register 210 | DTCER210 | 8 | 8 | 2 ICLK |
| 0008 71D4h | ICU | DTC Transfer Request Enable Register 212 | DTCER212 | 8 | 8 | 2 ICLK |
| 0008 71D5h | ICU | DTC Transfer Request Enable Register 213 | DTCER213 | 8 | 8 | 2 ICLK |
| 0008 71D6h | ICU | DTC Transfer Request Enable Register 214 | DTCER214 | 8 | 8 | 2 ICLK |
| 0008 71D7h | ICU | DTC Transfer Request Enable Register 215 | DTCER215 | 8 | 8 | 2 ICLK |
| 0008 71D8h | ICU | DTC Transfer Request Enable Register 216 | DTCER216 | 8 | 8 | 2 ICLK |
| 0008 71D9h | ICU | DTC Transfer Request Enable Register 217 | DTCER217 | 8 | 8 | 2 ICLK |
| 0008 71DBh | ICU | DTC Transfer Request Enable Register 219 | DTCER219 | 8 | 8 | 2 ICLK |
| 0008 71DCh | ICU | DTC Transfer Request Enable Register 220 | DTCER220 | 8 | 8 | 2 ICLK |
| 0008 71DFh | ICU | DTC Transfer Request Enable Register 223 | DTCER223 | 8 | 8 | 2 ICLK |
| 0008 71E0h | ICU | DTC Transfer Request Enable Register 224 | DTCER224 | 8 | 8 | 2 ICLK |
| 0008 71E3h | ICU | DTC Transfer Request Enable Register 227 | DTCER227 | 8 | 8 | 2 ICLK |
| 0008 71E4h | ICU | DTC Transfer Request Enable Register 228 | DTCER228 | 8 | 8 | 2 ICLK |
| 0008 71E7h | ICU | DTC Transfer Request Enable Register 231 | DTCER231 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (9/40)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles ICLK ≥ PCLK |
|---|---|---|---|---|---|---|
| 0008 7322h | ICU | Interrupt Source Priority Register 034 | IPR034 | 8 | 8 | 2 ICLK |
| 0008 7328h | ICU | Interrupt Source Priority Register 040 | IPR040 | 8 | 8 | 2 ICLK |
| 0008 7329h | ICU | Interrupt Source Priority Register 041 | IPR041 | 8 | 8 | 2 ICLK |
| 0008 732Ch | ICU | Interrupt Source Priority Register 044 | IPR044 | 8 | 8 | 2 ICLK |
| 0008 7330h | ICU | Interrupt Source Priority Register 048 | IPR048 | 8 | 8 | 2 ICLK |
| 0008 7331h | ICU | Interrupt Source Priority Register 049 | IPR049 | 8 | 8 | 2 ICLK |
| 0008 7332h | ICU | Interrupt Source Priority Register 050 | IPR050 | 8 | 8 | 2 ICLK |
| 0008 7333h | ICU | Interrupt Source Priority Register 051 | IPR051 | 8 | 8 | 2 ICLK |
| 0008 7334h | ICU | Interrupt Source Priority Register 052 | IPR052 | 8 | 8 | 2 ICLK |
| 0008 7335h | ICU | Interrupt Source Priority Register 053 | IPR053 | 8 | 8 | 2 ICLK |
| 0008 7336h | ICU | Interrupt Source Priority Register 054 | IPR054 | 8 | 8 | 2 ICLK |
| 0008 7337h | ICU | Interrupt Source Priority Register 055 | IPR055 | 8 | 8 | 2 ICLK |
| 0008 7338h | ICU | Interrupt Source Priority Register 056 | IPR056 | 8 | 8 | 2 ICLK |
| 0008 7339h | ICU | Interrupt Source Priority Register 057 | IPR057 | 8 | 8 | 2 ICLK |
| 0008 733Bh | ICU | Interrupt Source Priority Register 059 | IPR059 | 8 | 8 | 2 ICLK |
| 0008 733Ch | ICU | Interrupt Source Priority Register 060 | IPR060 | 8 | 8 | 2 ICLK |
| 0008 733Dh | ICU | Interrupt Source Priority Register 061 | IPR061 | 8 | 8 | 2 ICLK |
| 0008 733Eh | ICU | Interrupt Source Priority Register 062 | IPR062 | 8 | 8 | 2 ICLK |
| 0008 733Fh | ICU | Interrupt Source Priority Register 063 | IPR063 | 8 | 8 | 2 ICLK |
| 0008 7340h | ICU | Interrupt Source Priority Register 064 | IPR064 | 8 | 8 | 2 ICLK |
| 0008 7341h | ICU | Interrupt Source Priority Register 065 | IPR065 | 8 | 8 | 2 ICLK |
| 0008 7342h | ICU | Interrupt Source Priority Register 066 | IPR066 | 8 | 8 | 2 ICLK |
| 0008 7343h | ICU | Interrupt Source Priority Register 067 | IPR067 | 8 | 8 | 2 ICLK |
| 0008 7344h | ICU | Interrupt Source Priority Register 068 | IPR068 | 8 | 8 | 2 ICLK |
| 0008 7345h | ICU | Interrupt Source Priority Register 069 | IPR069 | 8 | 8 | 2 ICLK |
| 0008 7346h | ICU | Interrupt Source Priority Register 070 | IPR070 | 8 | 8 | 2 ICLK |
| 0008 7347h | ICU | Interrupt Source Priority Register 071 | IPR071 | 8 | 8 | 2 ICLK |
| 0008 7358h | ICU | Interrupt Source Priority Register 088 | IPR088 | 8 | 8 | 2 ICLK |
| 0008 7359h | ICU | Interrupt Source Priority Register 089 | IPR089 | 8 | 8 | 2 ICLK |
| 0008 7362h | ICU | Interrupt Source Priority Register 098 | IPR098 | 8 | 8 | 2 ICLK |
| 0008 7363h | ICU | Interrupt Source Priority Register 099 | IPR099 | 8 | 8 | 2 ICLK |
| 0008 7364h | ICU | Interrupt Source Priority Register 100 | IPR100 | 8 | 8 | 2 ICLK |
| 0008 7365h | ICU | Interrupt Source Priority Register 101 | IPR101 | 8 | 8 | 2 ICLK |
| 0008 7366h | ICU | Interrupt Source Priority Register 102 | IPR102 | 8 | 8 | 2 ICLK |
| 0008 7367h | ICU | Interrupt Source Priority Register 103 | IPR103 | 8 | 8 | 2 ICLK |
| 0008 7368h | ICU | Interrupt Source Priority Register 104 | IPR104 | 8 | 8 | 2 ICLK |
| 0008 7369h | ICU | Interrupt Source Priority Register 105 | IPR105 | 8 | 8 | 2 ICLK |
| 0008 736Ah | ICU | Interrupt Source Priority Register 106 | IPR106 | 8 | 8 | 2 ICLK |
| 0008 736Bh | ICU | Interrupt Source Priority Register 107 | IPR107 | 8 | 8 | 2 ICLK |
| 0008 736Ch | ICU | Interrupt Source Priority Register 108 | IPR108 | 8 | 8 | 2 ICLK |
| 0008 736Dh | ICU | Interrupt Source Priority Register 109 | IPR109 | 8 | 8 | 2 ICLK |
| 0008 736Eh | ICU | Interrupt Source Priority Register 110 | IPR110 | 8 | 8 | 2 ICLK |
| 0008 736Fh | ICU | Interrupt Source Priority Register 111 | IPR111 | 8 | 8 | 2 ICLK |
| 0008 7370h | ICU | Interrupt Source Priority Register 112 | IPR112 | 8 | 8 | 2 ICLK |
| 0008 7371h | ICU | Interrupt Source Priority Register 113 | IPR113 | 8 | 8 | 2 ICLK |
| 0008 7372h | ICU | Interrupt Source Priority Register 114 | IPR114 | 8 | 8 | 2 ICLK |
| 0008 7376h | ICU | Interrupt Source Priority Register 118 | IPR118 | 8 | 8 | 2 ICLK |
| 0008 7379h | ICU | Interrupt Source Priority Register 121 | IPR121 | 8 | 8 | 2 ICLK |
| 0008 737Bh | ICU | Interrupt Source Priority Register 123 | IPR123 | 8 | 8 | 2 ICLK |
| 0008 737Dh | ICU | Interrupt Source Priority Register 125 | IPR125 | 8 | 8 | 2 ICLK |
| 0008 737Fh | ICU | Interrupt Source Priority Register 127 | IPR127 | 8 | 8 | 2 ICLK |
| 0008 7381h | ICU | Interrupt Source Priority Register 129 | IPR129 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (25/40)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles ICLK ≥ PCLK |
|---|---|---|---|---|---|---|
| 000A 83B2h | RSCAN | Receive Buffer Register 1AH | RMIDH1 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83B4h | RSCAN | Receive Rule Entry Register 1CL | GAFLPL1 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83B4h | RSCAN | Receive Buffer Register 1BL | RMTS1 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83B6h | RSCAN | Receive Rule Entry Register 1CH | GAFLPH1 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83B6h | RSCAN | Receive Buffer Register 1BH | RMPTR1 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83B8h | RSCAN | Receive Rule Entry Register 2AL | GAFLIDL2 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83B8h | RSCAN | Receive Buffer Register 1CL | RMDF01 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83BAh | RSCAN | Receive Rule Entry Register 2AH | GAFLIDH2 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83BAh | RSCAN | Receive Buffer Register 1CH | RMDF11 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83BCh | RSCAN | Receive Rule Entry Register 2BL | GAFLML2 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83BCh | RSCAN | Receive Buffer Register 1DL | RMDF21 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83BEh | RSCAN | Receive Rule Entry Register 2BH | GAFLMH2 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83BEh | RSCAN | Receive Buffer Register 1DH | RMDF31 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83C0h | RSCAN | Receive Rule Entry Register 2CL | GAFLPL2 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83C0h | RSCAN | Receive Buffer Register 2AL | RMIDL2 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83C2h | RSCAN | Receive Rule Entry Register 2CH | GAFLPH2 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83C2h | RSCAN | Receive Buffer Register 2AH | RMIDH2 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83C4h | RSCAN | Receive Rule Entry Register 3AL | GAFLIDL3 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83C4h | RSCAN | Receive Buffer Register 2BL | RMTS2 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83C6h | RSCAN | Receive Rule Entry Register 3AH | GAFLIDH3 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83C6h | RSCAN | Receive Buffer Register 2BH | RMPTR2 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83C8h | RSCAN | Receive Rule Entry Register 3BL | GAFLML3 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83C8h | RSCAN | Receive Buffer Register 2CL | RMDF02 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83CAh | RSCAN | Receive Rule Entry Register 3BH | GAFLMH3 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83CAh | RSCAN | Receive Buffer Register 2CH | RMDF12 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83CCh | RSCAN | Receive Rule Entry Register 3CL | GAFLPL3 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83CCh | RSCAN | Receive Buffer Register 2DL | RMDF22 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83CEh | RSCAN | Receive Rule Entry Register 3CH | GAFLPH3 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83CEh | RSCAN | Receive Buffer Register 2DH | RMDF32 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83D0h | RSCAN | Receive Rule Entry Register 4AL | GAFLIDL4 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83D0h | RSCAN | Receive Buffer Register 3AL | RMIDL3 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83D2h | RSCAN | Receive Rule Entry Register 4AH | GAFLIDH4 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83D2h | RSCAN | Receive Buffer Register 3AH | RMIDH3 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83D4h | RSCAN | Receive Rule Entry Register 4BL | GAFLML4 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83D4h | RSCAN | Receive Buffer Register 3BL | RMTS3 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83D6h | RSCAN | Receive Rule Entry Register 4BH | GAFLMH4 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83D6h | RSCAN | Receive Buffer Register 3BH | RMPTR3 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83D8h | RSCAN | Receive Rule Entry Register 4CL | GAFLPL4 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83D8h | RSCAN | Receive Buffer Register 3CL | RMDF03 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83DAh | RSCAN | Receive Rule Entry Register 4CH | GAFLPH4 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83DAh | RSCAN | Receive Buffer Register 3CH | RMDF13 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83DCh | RSCAN | Receive Rule Entry Register 5AL | GAFLIDL5 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83DCh | RSCAN | Receive Buffer Register 3DL | RMDF23 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83DEh | RSCAN | Receive Rule Entry Register 5AH | GAFLIDH5 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83DEh | RSCAN | Receive Buffer Register 3DH | RMDF33 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83E0h | RSCAN | Receive Rule Entry Register 5BL | GAFLML5 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83E0h | RSCAN | Receive Buffer Register 4AL | RMIDL4 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83E2h | RSCAN | Receive Rule Entry Register 5BH | GAFLMH5 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83E2h | RSCAN | Receive Buffer Register 4AH | RMIDH4 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83E4h | RSCAN | Receive Rule Entry Register 5CL | GAFLPL5 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83E4h | RSCAN | Receive Buffer Register 4BL | RMTS4 | 16 | 16 | 2 or 3 PCLKB |
| 000A 83E6h | RSCAN | Receive Rule Entry Register 5CH | GAFLPH5 | 16 | 16 | 2 or 3 PCLKB |

**Table 4.1 List of I/O Registers (Address Order) (34/40)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK |
| 000C 1A2Dh | MTU7 | Timer Status Register | TSR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A30h | MTU | Timer Interrupt Skipping Set Register 1B | TITCR1B | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1A31h | MTU | Timer Interrupt Skipping Counters 1B | TITCNT1B | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A32h | MTU | Timer Buffer Transfer Set Register B | TBTERB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A34h | MTU | Timer Dead Time Enable Register B | TDERB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A36h | MTU | Timer Output Level Buffer Register B | TOLBRB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A38h | MTU6 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1A39h | MTU7 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A3Ah | MTU | Timer Interrupt Skipping Mode Register B | TITMRB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A3Bh | MTU | Timer Interrupt Skipping Set Register 2B | TITCR2B | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A3Ch | MTU | Timer Interrupt Skipping Counters 2B | TITCNT2B | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A40h | MTU7 | Timer A/D Converter Start Request Control Register | TADCR | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A44h | MTU7 | Timer A/D Converter Start Request Cycle Set Register A | TADCORA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1A46h | MTU7 | Timer A/D Converter Start Request Cycle Set Register B | TADCORB | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A48h | MTU7 | Timer A/D Converter Start Request Cycle Set Buffer Register A | TADCOBRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1A4Ah | MTU7 | Timer A/D Converter Start Request Cycle Set Buffer Register B | TADCOBRB | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A4Ch | MTU6 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A4Dh | MTU7 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A50h | MTU6 | Timer Synchronous Clear Register | TSYCR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A60h | MTU | Timer Waveform Control Register B | TWCRB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A70h | MTU | Timer Mode Register 2B | TMDR2B | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A72h | MTU6 | Timer General Register E | TGRE | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A74h | MTU7 | Timer General Register E | TGRE | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A76h | MTU7 | Timer General Register F | TGRF | 16 | 16 | 4 or 5 PCLKA |
| 000C 1A80h | MTU | Timer Start Register B | TSTRB | 8 | 8, 16 | 4 or 5 PCLKA |
| 000C 1A81h | MTU | Timer Synchronous Register B | TSYRB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A84h | MTU | Timer Read/Write Enable Register B | TRWERB | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A93h | MTU6 | Noise Filter Control Register 6 | NFCR6 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A94h | MTU7 | Noise Filter Control Register 7 | NFCR7 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1A95h | MTU5 | Noise Filter Control Register 5 | NFCR5 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1C80h | MTU5 | Timer Counter U | TCNTU | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1C82h | MTU5 | Timer General Register U | TGRU | 16 | 16 | 4 or 5 PCLKA |
| 000C 1C84h | MTU5 | Timer Control Register U | TCRU | 8 | 8 | 4 or 5 PCLKA |
| 000C 1C85h | MTU5 | Timer Control Register 2U | TCR2U | 8 | 8 | 4 or 5 PCLKA |
| 000C 1C86h | MTU5 | Timer I/O Control Register U | TIORU | 8 | 8 | 4 or 5 PCLKA |
| 000C 1C90h | MTU5 | Timer Counter V | TCNTV | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1C92h | MTU5 | Timer General Register V | TGRV | 16 | 16 | 4 or 5 PCLKA |
| 000C 1C94h | MTU5 | Timer Control Register V | TCRV | 8 | 8 | 4 or 5 PCLKA |
| 000C 1C95h | MTU5 | Timer Control Register 2V | TCR2V | 8 | 8 | 4 or 5 PCLKA |
| 000C 1C96h | MTU5 | Timer I/O Control Register V | TIORV | 8 | 8 | 4 or 5 PCLKA |
| 000C 1CA0h | MTU5 | Timer Counter W | TCNTW | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 1CA2h | MTU5 | Timer General Register W | TGRW | 16 | 16 | 4 or 5 PCLKA |
| 000C 1CA4h | MTU5 | Timer Control Register W | TCRW | 8 | 8 | 4 or 5 PCLKA |
| 000C 1CA5h | MTU5 | Timer Control Register 2W | TCR2W | 8 | 8 | 4 or 5 PCLKA |
| 000C 1CA6h | MTU5 | Timer I/O Control Register W | TIORW | 8 | 8 | 4 or 5 PCLKA |
| 000C 1CB2h | MTU5 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4 or 5 PCLKA |
| 000C 1CB4h | MTU5 | Timer Start Register | TSTR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1CB6h | MTU5 | Timer Compare Match Clear Register | TCNTCMPCLR | 8 | 8 | 4 or 5 PCLKA |
| 000C 1D30h | MTU | A/D Conversion Start Request Select Register 0 | TADSTRGR0 | 8 | 8 | 4 or 5 PCLKA |
| 000C 1D32h | MTU | A/D Conversion Start Request Select Register 1 | TADSTRGR1 | 8 | 8 | 4 or 5 PCLKA |
| 000C 2000h | GPT | General PWM Timer Software Start Register | GTSTR | 16 | 8, 16, 32 | 4 or 5 PCLKA |

**Table 4.1 List of I/O Registers (Address Order) (35/40)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK |
| 000C 2002h | GPT | Noise Filter Control Register | NFCR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2004h | GPT | General PWM Timer Hardware Source Start/Stop Control Register 0 | GTHSCR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2006h | GPT | General PWM Timer Hardware Source Clear Control Register | GTHCCR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2008h | GPT | General PWM Timer Hardware Start Source Select Register | GTHSSR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 200Ah | GPT | General PWM Timer Hardware Stop/Clear Source Select Register | GTHPSR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 200Ch | GPT | General PWM Timer Write-Protection Register | GTWP | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 200Eh | GPT | General PWM Timer Sync Register | GTSYNC | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2010h | GPT | General PWM Timer External Trigger Input Interrupt Register | GTETINT | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2014h | GPT | General PWM Timer Buffer Operation Disable Register | GTBDR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2018h | GPT | General PWM Timer Start Write-Protection Register | GTSWP | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 201Ch | GPT | General PWM Timer Clearing Write-Protection Register | GTCWP | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2020h | GPT | General PWM Timer Common Register Write-Protection Register | GTCMNWP | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2024h | GPT | General PWM Timer Mode Register | GTMDR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2028h | GPT | General PWM Timer External Clock Noise Filter Control Register | GTECNFCR | 32 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 202Ch | GPT | General PWM Timer A/D Conversion Start Request Signal Monitor Register | GTADSMR | 32 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2100h | GPT0 | General PWM Timer I/O Control Register | GTIOR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2102h | GPT0 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2104h | GPT0 | General PWM Timer Control Register | GTCR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2106h | GPT0 | General PWM Timer Buffer Enable Register | GTBER | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2108h | GPT0 | General PWM Timer Count Direction Register | GTUDC | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 210Ah | GPT0 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 210Ch | GPT0 | General PWM Timer Status Register | GTST | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 210Eh | GPT0 | General PWM Timer Counter | GTCNT | 16 | 16 | 4 or 5 PCLKA |
| 000C 2110h | GPT0 | General PWM Timer Compare Capture Register A | GTCCRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2112h | GPT0 | General PWM Timer Compare Capture Register B | GTCCRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2114h | GPT0 | General PWM Timer Compare Capture Register C | GTCCRC | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2116h | GPT0 | General PWM Timer Compare Capture Register D | GTCCRD | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2118h | GPT0 | General PWM Timer Compare Capture Register E | GTCCRE | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 211Ah | GPT0 | General PWM Timer Compare Capture Register F | GTCCRF | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 211Ch | GPT0 | General PWM Timer Period Setting Register | GTPR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 211Eh | GPT0 | General PWM Timer Period Setting Buffer Register | GTPBR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2120h | GPT0 | General PWM Timer Period Setting Double Buffer Register | GTPDBR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2124h | GPT0 | A/D Converter Start Request Timing Register A | GTADTRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2126h | GPT0 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2128h | GPT0 | A/D Converter Start Request Timing Double Buffer Register A | GTADTDBRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 212Ch | GPT0 | A/D Converter Start Request Timing Register B | GTADTRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 212Eh | GPT0 | A/D Converter Start Request Timing Buffer Register B | GTADTBRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2130h | GPT0 | A/D Converter Start Request Timing Double Buffer Register B | GTADTDBRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2134h | GPT0 | General PWM Timer Output Negate Control Register | GTONCR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2136h | GPT0 | General PWM Timer Dead Time Control Register | GTDTCR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2138h | GPT0 | General PWM Timer Dead Time Value Register U | GTDVU | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 213Ah | GPT0 | General PWM Timer Dead Time Value Register D | GTDVD | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 213Ch | GPT0 | General PWM Timer Dead Time Buffer Register U | GTDBU | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 213Eh | GPT0 | General PWM Timer Dead Time Buffer Register D | GTDBD | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2140h | GPT0 | General PWM Timer Output Protection Function Status Register | GTSOS | 16 | 16, 32 | 4 or 5 PCLKA |

**Table 4.1 List of I/O Registers (Address Order) (37/40)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK |
| 000C 2220h | GPT2 | General PWM Timer Period Setting Double Buffer Register | GTPDBR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2224h | GPT2 | A/D Converter Start Request Timing Register A | GTADTRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2226h | GPT2 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2228h | GPT2 | A/D Converter Start Request Timing Double Buffer Register A | GTADTDBRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 222Ch | GPT2 | A/D Converter Start Request Timing Register B | GTADTRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 222Eh | GPT2 | A/D Converter Start Request Timing Buffer Register B | GTADTBRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2230h | GPT2 | A/D Converter Start Request Timing Double Buffer Register B | GTADTDBRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2234h | GPT2 | General PWM Timer Output Negate Control Register | GTONCR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2236h | GPT2 | General PWM Timer Dead Time Control Register | GTDTCR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2238h | GPT2 | General PWM Timer Dead Time Value Register U | GTDVU | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 223Ah | GPT2 | General PWM Timer Dead Time Value Register D | GTDVD | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 223Ch | GPT2 | General PWM Timer Dead Time Buffer Register U | GTDBU | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 223Eh | GPT2 | General PWM Timer Dead Time Buffer Register D | GTDBD | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2240h | GPT2 | General PWM Timer Output Protection Function Status Register | GTSOS | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2242h | GPT2 | General PWM Timer Output Protection Function Temporary Release Register | GTSOTR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2280h | GPT3 | General PWM Timer I/O Control Register | GTIOR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2282h | GPT3 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2284h | GPT3 | General PWM Timer Control Register | GTCR | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2286h | GPT3 | General PWM Timer Buffer Enable Register | GTBER | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 2288h | GPT3 | General PWM Timer Count Direction Register | GTUDC | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 228Ah | GPT3 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 228Ch | GPT3 | General PWM Timer Status Register | GTST | 16 | 8, 16, 32 | 4 or 5 PCLKA |
| 000C 228Eh | GPT3 | General PWM Timer Counter | GTCNT | 16 | 16 | 4 or 5 PCLKA |
| 000C 2290h | GPT3 | General PWM Timer Compare Capture Register A | GTCCRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2292h | GPT3 | General PWM Timer Compare Capture Register B | GTCCRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2294h | GPT3 | General PWM Timer Compare Capture Register C | GTCCRC | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2296h | GPT3 | General PWM Timer Compare Capture Register D | GTCCRD | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2298h | GPT3 | General PWM Timer Compare Capture Register E | GTCCRE | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 229Ah | GPT3 | General PWM Timer Compare Capture Register F | GTCCRF | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 229Ch | GPT3 | General PWM Timer Period Setting Register | GTPR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 229Eh | GPT3 | General PWM Timer Period Setting Buffer Register | GTPBR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22A0h | GPT3 | General PWM Timer Period Setting Double Buffer Register | GTPDBR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22A4h | GPT3 | A/D Converter Start Request Timing Register A | GTADTRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22A6h | GPT3 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22A8h | GPT3 | A/D Converter Start Request Timing Double Buffer Register A | GTADTDBRA | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22ACh | GPT3 | A/D Converter Start Request Timing Register B | GTADTRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22AEh | GPT3 | A/D Converter Start Request Timing Buffer Register B | GTADTBRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22B0h | GPT3 | A/D Converter Start Request Timing Double Buffer Register B | GTADTDBRB | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22B4h | GPT3 | General PWM Timer Output Negate Control Register | GTONCR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22B6h | GPT3 | General PWM Timer Dead Time Control Register | GTDTCR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22B8h | GPT3 | General PWM Timer Dead Time Value Register U | GTDVU | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22BAh | GPT3 | General PWM Timer Dead Time Value Register D | GTDVD | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22BCh | GPT3 | General PWM Timer Dead Time Buffer Register U | GTDBU | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22BEh | GPT3 | General PWM Timer Dead Time Buffer Register D | GTDBD | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22C0h | GPT3 | General PWM Timer Output Protection Function Status Register | GTSOS | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 22C2h | GPT3 | General PWM Timer Output Protection Function Temporary Release Register | GTSOTR | 16 | 16, 32 | 4 or 5 PCLKA |
| 000C 2300h | GPT01 | General PWM Timer Longword Counter | GTCNTLW | 32 | 32 | 4 or 5 PCLKA |

**Table 4.1 List of I/O Registers (Address Order) (40/40)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK |
| 007F C354h | FLASHCONST | Unique ID Register 1 | UIDR1 | 32 | 32 | 2 or 3 FCLK |
| 007F C358h | FLASHCONST | Unique ID Register 2 | UIDR2 | 32 | 32 | 2 or 3 FCLK |
| 007F C35Ch | FLASHCONST | Unique ID Register 3 | UIDR3 | 32 | 32 | 2 or 3 FCLK |
| 007F FFB2h | FLASH | Flash P/E Mode Entry Register | FENTRYR | 16 | 16 | 2 or 3 FCLK |

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0, TMR2, TMR4, or TMR6 register. Table 23.5 lists register allocation for 16-bit access in the User's Manual: Hardware.

**Table 5.6 DC Characteristics (4)**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, $T_a$ = –40 to +85°C

| Item | | | Symbol | Typ.*3 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Supply current*1 | Software standby mode*2 | $T_a$ = 25°C | $I_{CC}$ | 1.5 | 15.0 | µA | |
| | | $T_a$ = 55°C | | 3.0 | 38.0 | | |
| | | $T_a$ = 85°C | | 13.0 | 135.0 | | |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT and LVD are stopped.
Note 3. VCC = 5 V.

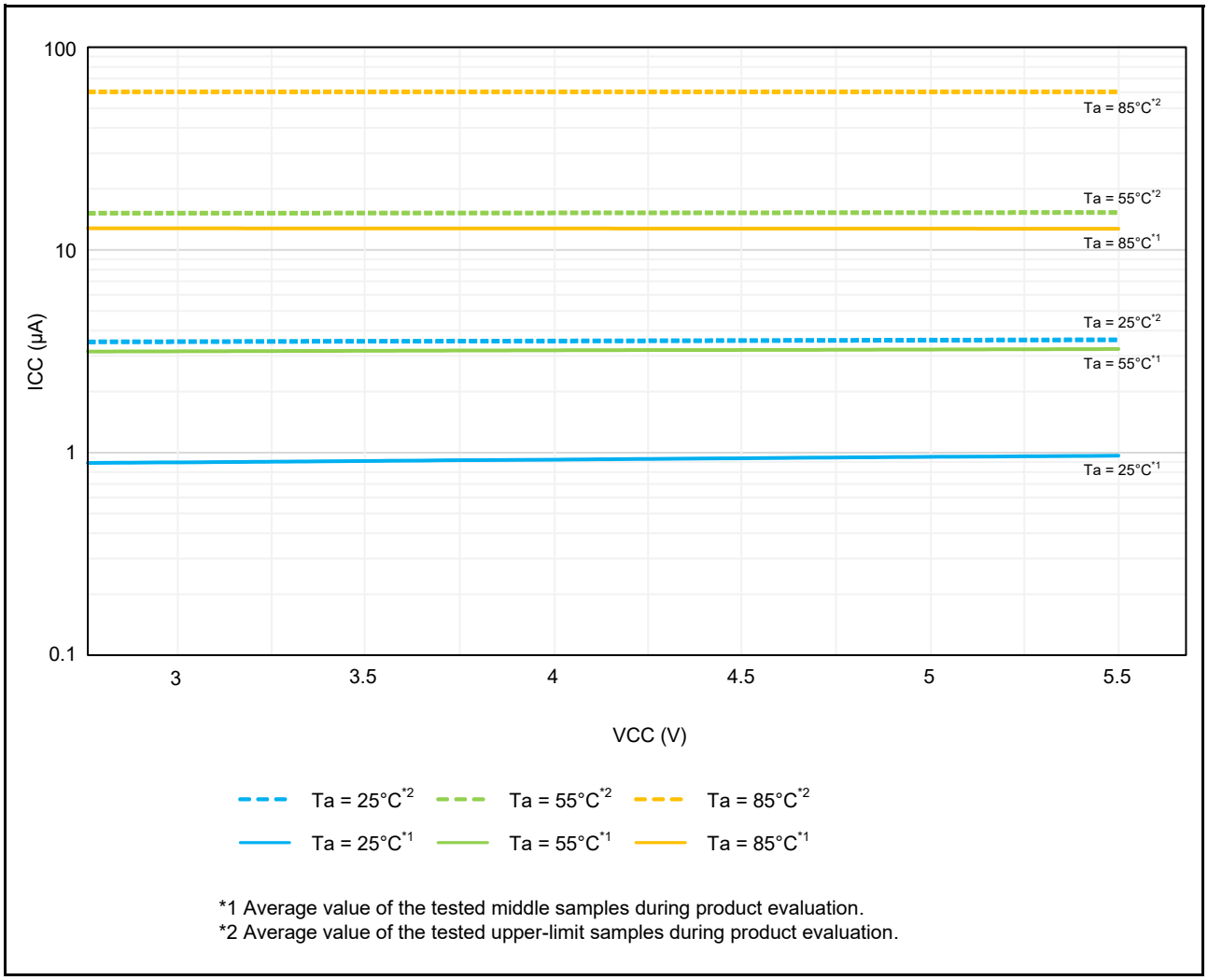



**Figure 5.1 Voltage Dependency in Software Standby Mode (Reference Data)**

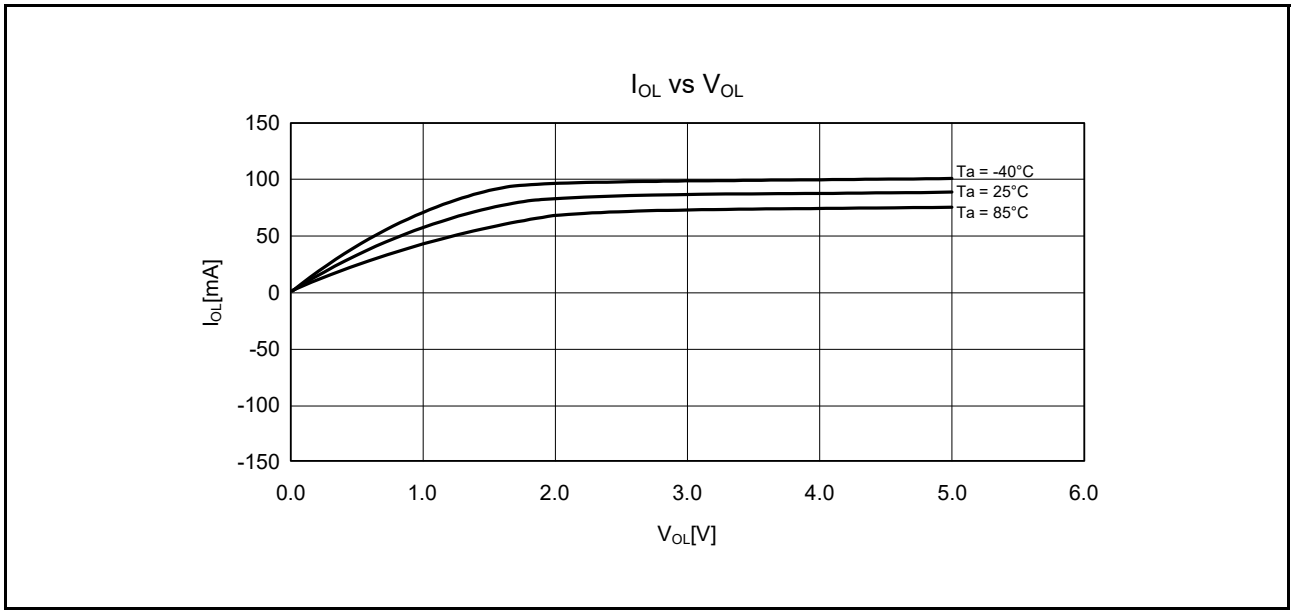



**Figure 5.18 $V_{OL}$ and $I_{OL}$ Temperature Characteristics of RIIC Output Pin at VCC = 5.0 V (Reference Data)**

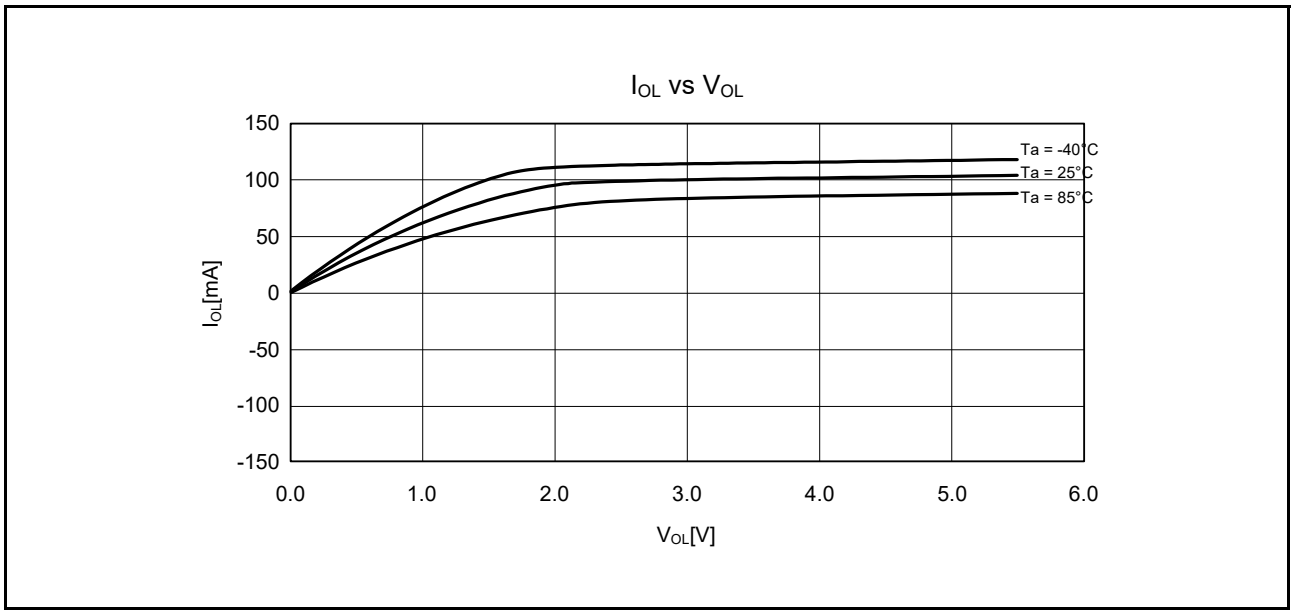



**Figure 5.19 $V_{OL}$ and $I_{OL}$ Temperature Characteristics of RIIC Output Pin at VCC = 5.5 V (Reference Data)**

## 5.3.2 Reset Timing

**Table 5.17 Reset Timing**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, $T_a$ = –40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| RES# pulse width | At power-on | $t_{RESWP}$ | 3 | — | — | ms | Figure 5.27 |
| | Other than above | $t_{RESW}$ | 30 | — | — | µs | Figure 5.28 |
| Wait time after RES# cancellation (at power-on) | | $t_{RESWT}$ | — | 27.5 | — | ms | Figure 5.27 |
| Wait time after RES# cancellation (during powered-on state) | | $t_{RESWT}$ | — | 114 | — | µs | Figure 5.28 |
| Independent watchdog timer reset period | | $t_{RESWIW}$ | — | 1 | — | IWDT clock cycle | Figure 5.29 |
| Software reset period | | $t_{RESWSW}$ | — | 1 | — | ICLK cycle | |
| Wait time after independent watchdog timer reset cancellation*1 | | $t_{RESW2}$ | — | 300 | — | µs | |
| Wait time after software reset cancellation | | $t_{RESW2}$ | — | 168 | — | µs | |

Note 1. When IWDTCR.CKS[3:0] = 0000b.

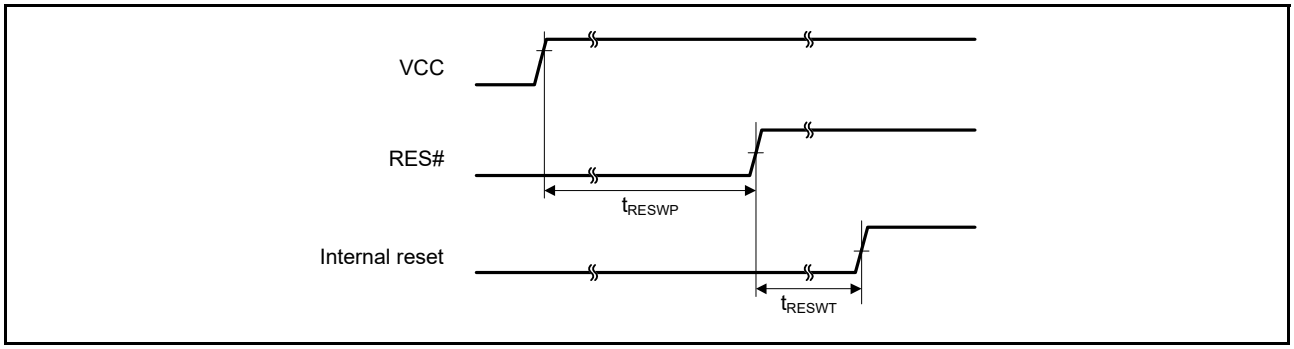



**Figure 5.27 Reset Input Timing at Power-On**

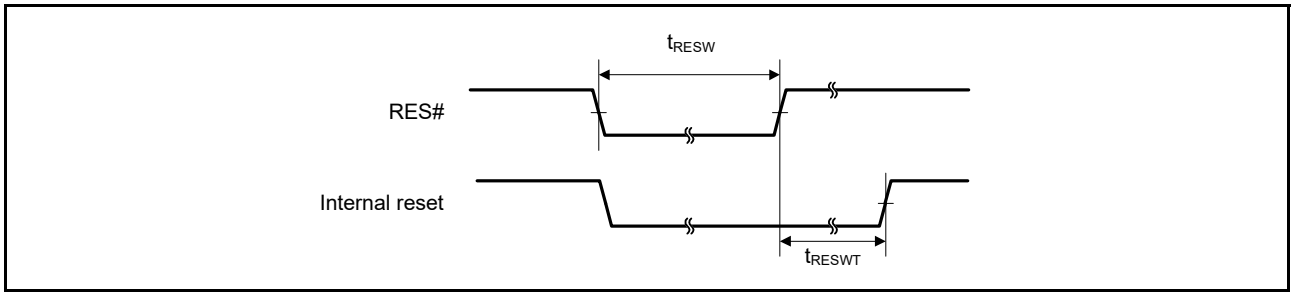



**Figure 5.28 Reset Input Timing (1)**

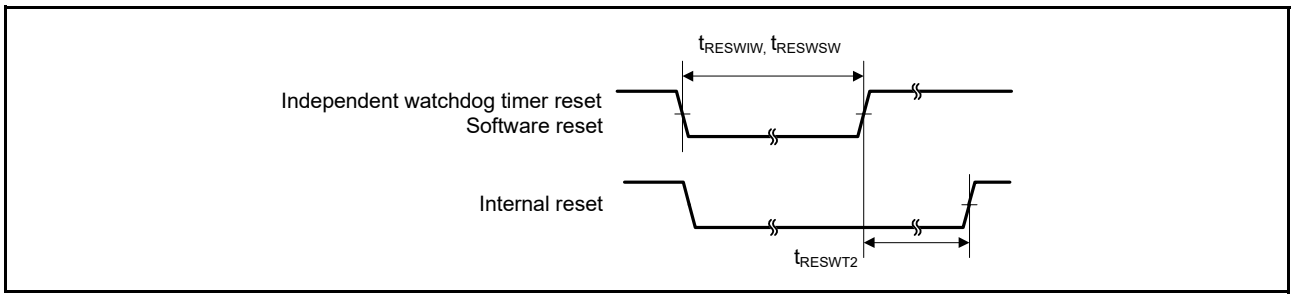



**Figure 5.29 Reset Input Timing (2)**

## 5.3.4 Control Signal Timing

**Table 5.22 Control Signal Timing**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, $T_a$ = –40 to +85°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | — | — | ns | NMI digital filter disabled (NMIFLTE.NFLTEN = 0) | $t_{Pcyc} \times 2 \le 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | — | — | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | — | — | | NMI digital filter enabled (NMIFLTE.NFLTEN = 1) | $t_{NMICK} \times 3 \le 200$ ns |
| | | $t_{NMICK} \times 3.5$*2 | — | — | | | $t_{NMICK} \times 3 > 200$ ns |
| IRQ pulse width | $t_{IRQW}$ | 200 | — | — | ns | IRQ digital filter disabled (IRQFLTE0.FLTENi = 0) | $t_{Pcyc} \times 2 \le 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | — | — | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | — | — | | IRQ digital filter enabled (IRQFLTE0.FLTENi = 1) | $t_{IRQCK} \times 3 \le 200$ ns |
| | | $t_{IRQCK} \times 3.5$*3 | — | — | | | $t_{IRQCK} \times 3 > 200$ ns |

Note: 200 ns minimum in software standby mode.
Note 1. $t_{Pcyc}$ indicates the cycle of PCLKB.
Note 2. $t_{NMICK}$ indicates the cycle of the NMI digital filter sampling clock.
Note 3. $t_{IRQCK}$ indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

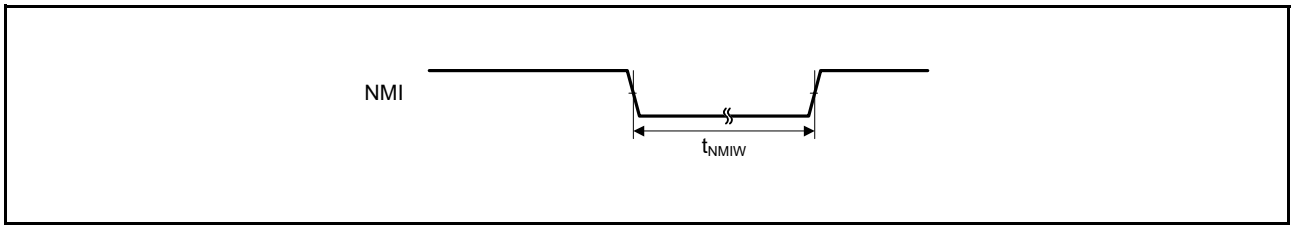



**Figure 5.32 NMI Interrupt Input Timing**

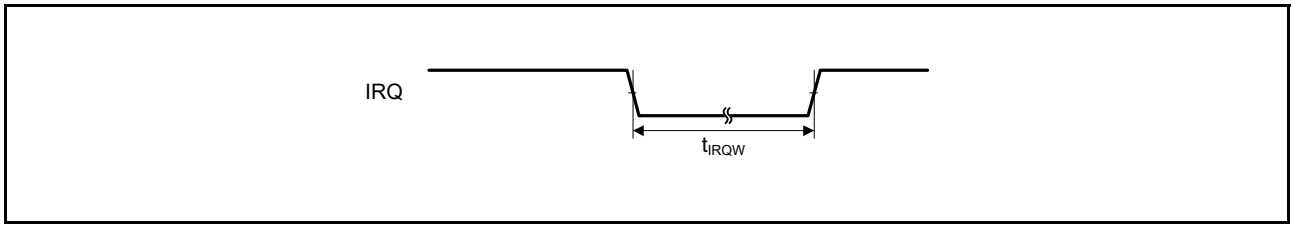



**Figure 5.33 IRQ Interrupt Input Timing**

**Table 5.26 Timing of On-Chip Peripheral Modules (4)**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, $T_a$ = –40 to +85°C, C = 30 pF

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| Simple SPI (SCI1, SCI5, SCI6, SCI8, SCI9) | SCK clock cycle output (master) | | $t_{SPcyc}$ | 4 | 65536 | $t_{Pcyc}$ | Figure 5.45 |
| | SCK clock cycle input (slave) | | | 6 | — | $t_{Pcyc}$ | |
| | SCK clock high pulse width | | $t_{SPCKWH}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock low pulse width | | $t_{SPCKWL}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock rise/fall time | | $t_{SPCKr}$, $t_{SPCKf}$ | — | 20 | ns | |
| | Data input setup time (master) | VCC = 4.0 V or above | $t_{SU}$ | 40 | — | ns | Figure 5.46, Figure 5.47 |
| | | VCC = 2.7 V or above | | 65 | — | | |
| | Data input setup time (slave) | | | 40 | — | | |
| | Data input hold time | | $t_H$ | 40 | — | ns | |
| | SS input setup time | | $t_{LEAD}$ | 3 | — | $t_{SPcyc}$ | |
| | SS input hold time | | $t_{LAG}$ | 3 | — | $t_{SPcyc}$ | |
| | Data output delay time (master) | | $t_{OD}$ | — | 40 | ns | |
| | Data output delay time (slave) | VCC = 4.0 V or above | | — | 40 | | |
| | | VCC = 2.7 V or above | | — | 65 | | |
| | Data output hold time | Master | $t_{OH}$ | –10 | — | ns | |
| | | Slave | | –10 | — | | |
| | Data rise/fall time | | $t_{Dr}$, $t_{Df}$ | — | 20 | ns | |
| | SS input rise/fall time | | $t_{SSLr}$, $t_{SSLf}$ | — | 20 | ns | |
| | Slave access time | | $t_{SA}$ | — | 6 | $t_{Pcyc}$ | Figure 5.48, Figure 5.49 |
| | Slave output release time | | $t_{REL}$ | — | 6 | $t_{Pcyc}$ | |

Note 1. $t_{Pcyc}$: PCLK cycle

## 5.7 D/A Conversion Characteristics

**Table 5.36 D/A Conversion Characteristics**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, $T_a$ = –40 to +85°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Resolution | — | — | — | 8 | Bit | |
| Conversion time | $t_{DCONV}$ | — | — | 3.0 | µs | |
| Absolute accuracy | — | — | — | ±3.0 | LSB | |
| Output load resistance | — | 4 | — | — | MΩ | |
| Output load capacity | — | — | — | 35 | pF | |
| Output resistance | — | — | 9.0 | — | kΩ | |

Note: When using ports 23 and 24 as DA0 and DA1 outputs, make sure that VCC ≥ DA output voltage.

**Table 5.38 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)**

Conditions: VCC = 0 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, $T_a$ = –40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Wait time after power-on reset cancellation | At normal startup | $t_{POR}$ | — | 28.4 | — | ms | Figure 5.54 |
| Wait time after voltage monitoring 0 reset cancellation | | $t_{LVD0}$ | — | 568 | — | µs | Figure 5.55 |
| Wait time after voltage monitoring 1 reset cancellation | | $t_{LVD1}$ | — | 100 | — | µs | Figure 5.56 |
| Wait time after voltage monitoring 2 reset cancellation | | $t_{LVD2}$ | — | 100 | — | µs | Figure 5.57 |
| Response delay time | | $t_{det}$ | — | — | 350 | µs | Figure 5.53 |
| Minimum VCC down time*1 | | $t_{VOFF}$ | 350 | — | — | µs | Figure 5.53, VCC = 1.0 V or above |
| Power-on reset enable time | | $t_{W(POR)}$ | 1 | — | — | ms | Figure 5.54, VCC = below 1.0 V |
| LVD operation stabilization time (after LVD is enabled) | | $Td_{(E-A)}$ | — | — | 300 | µs | Figure 5.56, Figure 5.57 |
| Hysteresis width (LVD0, LVD1 and LVD2) | | $V_{LVH}$ | — | 70 | — | mV | Vdet1_0 to 4 selected |
| | | | — | 60 | — | | Vdet0_0 to 2 selected<br>Vdet1_5 to 8 selected<br>LVD2 selected |

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels $V_{POR}$, $V_{det0}$, $V_{det1}$, and $V_{det2}$ for the POR/LVD.

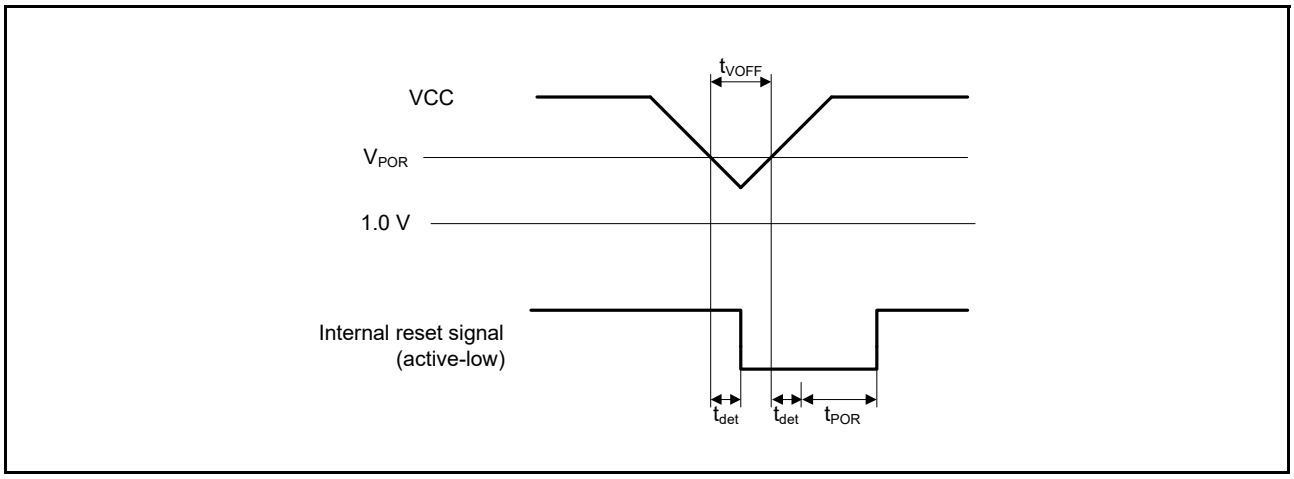



**Figure 5.53 Voltage Detection Reset Timing**

## 5.9 Oscillation Stop Detection Timing

**Table 5.39 Oscillation Stop Detection Timing**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 =AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V, $T_a$ = –40 to +85°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Detection time | $t_{dr}$ | — | — | 1 | ms | Figure 5.58 |

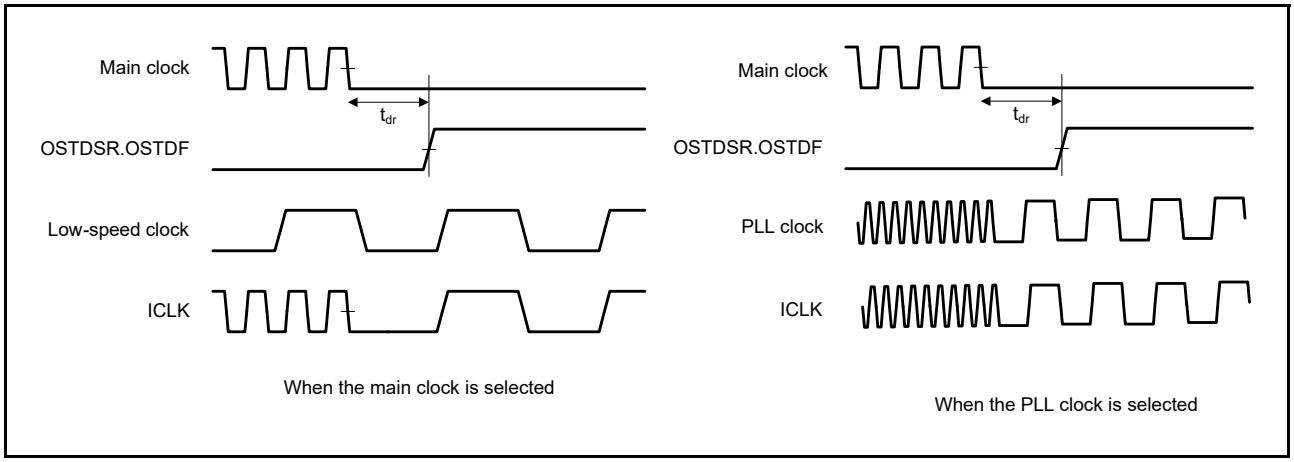



**Figure 5.58 Oscillation Stop Detection Timing**

**Table 5.42 ROM (Flash Memory for Code Storage) Characteristics (3): Middle-Speed Operating Mode**

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREFH0 = VREFH1 = VREFH2 = VCC to 5.5 V,
VSS = AVSS0 = AVSS1 = AVSS2 = VREFL0 = VREFL1 = VREFL2 = 0 V

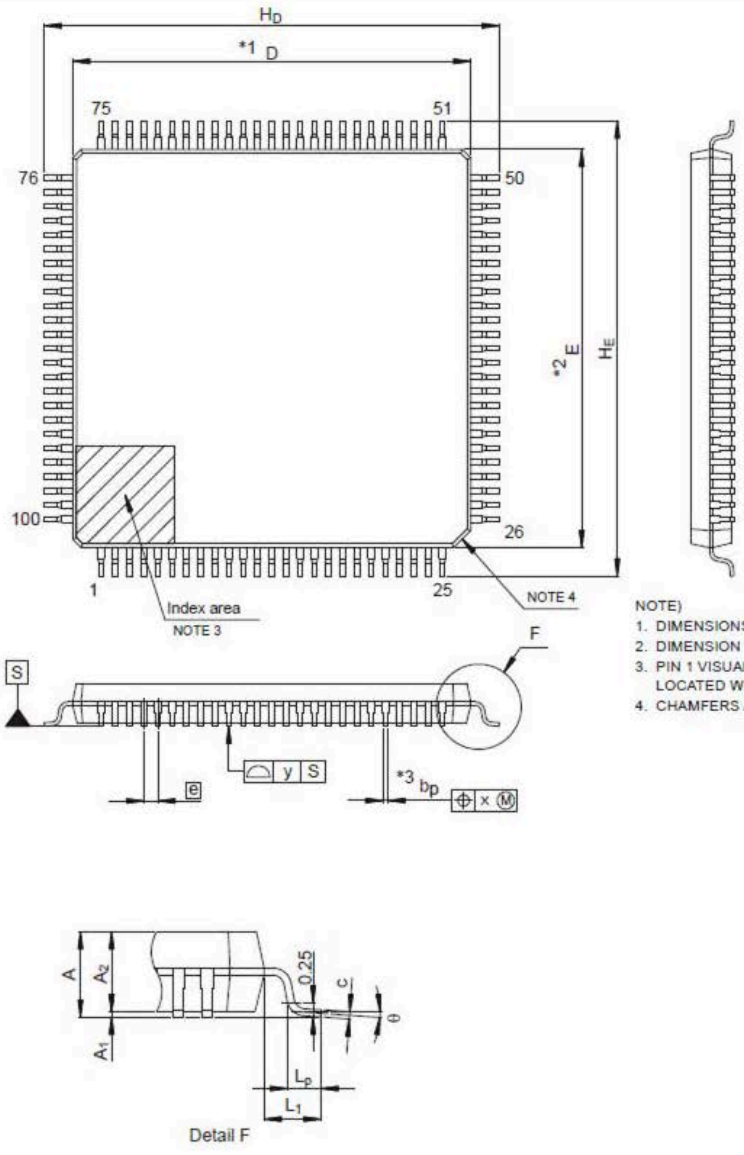
Temperature range for the programming/erasure operation: $T_a$ = –40 to +85°C

| Item | | Symbol | FCLK = 1 MHz | | | FCLK = 8 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time | 8-byte | $t_{P8}$ | — | 152.0 | 1367.0 | — | 97.9 | 936.0 | µs |
| Erasure time | 2-Kbyte | $t_{E2K}$ | — | 8.8 | 279.7 | — | 5.9 | 220.8 | ms |
| | 512-Kbyte (when block erase command used) | $t_{E512K}$ | — | 928.0 | 19221.2 | — | 190.6 | 4107.3 | ms |
| | 512-Kbyte (when all-block erase command used) | $t_{EA512K}$ | — | 922.7 | 19015.0 | — | 185.4 | 3901.0 | ms |
| Blank check time | 8-byte | $t_{BC8}$ | — | — | 85.0 | — | — | 50.9 | µs |
| | 2-Kbyte | $t_{BC2K}$ | — | — | 1870.0 | — | — | 401.5 | µs |
| Erase operation forcible stop time | | $t_{SED}$ | — | — | 28.0 | — | — | 21.3 | µs |
| Start-up area switching setting time | | $t_{SAS}$ | — | 13.0 | 573.3 | — | 7.7 | 450.1 | ms |
| Access window time | | $t_{AWS}$ | — | 13.0 | 573.3 | — | 7.7 | 450.1 | ms |
| ROM mode transition wait time 1 | | $t_{DIS}$ | 2.0 | — | — | 2.0 | — | — | µs |
| ROM mode transition wait time 2 | | $t_{MS}$ | 3.0 | — | — | 3.0 | — | — | µs |

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KB-B | — | 0.6 |

Unit: mm




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

Figure B 100-Pin LFQFP (PLQP0100KB-B)

| REVISION HISTORY | RX24U Group Datasheet |
|---|---|

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

| Rev. | Date | Description | | Classification |
|---|---|---|---|---|
| | | Page | Summary | |
| 1.00 | Mar 31, 2017 | — | First edition, issued | |