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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1516-e-ml

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.0 DEVICE OVERVIEW

The PIC16(L)F1516/7/8/9 are described within this data sheet. Figure 1-1 shows a block diagram of the PIC16(L)F1516/7/8/9 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1:DEVICE PERIPHERAL
SUMMARY

Peripheral	PIC16(L)F1516	PIC16(L)F1517	PIC16(L)F1518	PIC16(L)F1519			
Analog-to-Digital Convert	er (ADC)	٠	٠	٠	٠		
Fixed Voltage Reference	(FVR)	٠	٠	٠	٠		
Temperature Indicator		٠	٠	٠	٠		
Capture/Compare/PWM Modules							
	CCP1			٠	٠		
	CCP2	٠	٠	٠	٠		
EUSARTs							
	EUSART						
Master Synchronous Ser	ial Ports						
	MSSP	٠	٠	٠	٠		
Timers							
	Timer0	٠	٠	٠	٠		
	Timer1	٠	٠	٠	٠		
	Timer2	•	٠	•	•		



3.6.2 OVERFLOW/UNDERFLOW RESET

If the STVREN bit in Configuration Words is programmed to '1', the device will be reset if the stack is PUSHed beyond the 16th level or POPed beyond the first level, setting the appropriate bits (STKOVF or STKUNF, respectively) in the PCON register.

3.7 Indirect Addressing

The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the File Select Registers (FSR). If the FSRn address specifies one of the two INDFn registers, the read will return '0' and the write will not occur (though Status bits may be affected). The FSRn register value is created by the pair FSRnH and FSRnL.

The FSR registers form a 16-bit address that allows an addressing space with 65536 locations. These locations are divided into three memory regions:

- · Traditional Data Memory
- · Linear Data Memory
- Program Flash Memory

FIGURE 5-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



- Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
 - 2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.
 - **3:** For oscillator design assistance, reference the following Microchip Applications Notes:
 - AN826, Crystal Oscillator Basics and Crystal Selection for rfPIC[®] and PIC[®] Devices (DS00826)
 - AN849, Basic PIC[®] Oscillator Design (DS00849)
 - AN943, Practical PIC[®] Oscillator Analysis and Design (DS00943)
 - AN949, Making Your Oscillator Work (DS00949)

FIGURE 5-4:

CERAMIC RESONATOR OPERATION (XT OR HS MODE)



5.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended, unless either FSCM or Two-Speed Start-up are enabled. In this case, code will continue to execute at the selected INTOSC frequency while the OST is counting. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-Up mode can be selected (see **Section 5.4 "Two-Speed Clock Start-up Mode"**).

7.3 Interrupts During Sleep

Some interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the SLEEP instruction. The instruction directly after the SLEEP instruction will always be executed before branching to the ISR. Refer to the Section 8.0 "Power-Down Mode (Sleep)" for more details.

7.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. This interrupt is enabled by setting the INTE bit of the INTCON register. The INTEDG bit of the OPTION_REG register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF bit of the INTCON register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector.

7.5 Automatic Context Saving

Upon entering an interrupt, the return PC address is saved on the stack. Additionally, the following registers are automatically saved in the Shadow registers:

- W register
- STATUS register (except for TO and PD)
- BSR register
- FSR registers
- PCLATH register

Upon exiting the Interrupt Service Routine, these registers are automatically restored. Any modifications to these registers during the ISR will be lost. If modifications to any of these registers are desired, the corresponding Shadow register should be modified and the value will be restored when exiting the ISR. The Shadow registers are available in Bank 31 and are readable and writable. Depending on the user's application, other registers may also need to be saved.

	•••••••••••••••••••••••••••••••••••••••						
R/W-0/0	U-0	U-0	U-0	R/W-0/0	U-0	U-0	R/W-0/0
OSFIE	—	_	_	BCLIE		_	CCP2IE
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplei	mented bit, read	as '0'	
u = Bit is uncl	hanged	x = Bit is unkr	nown	-n/n = Value	at POR and BO	R/Value at all o	ther Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7	OSFIE: Oscill	lator Fail Interru	upt Enable bit				
	1 = Enables	the Oscillator F	ail interrupt				
		the Oscillator i					
bit 6-4	Unimplemen	ted: Read as '	D'				
bit 3	BCLIE: MSSI	P Bus Collision	Interrupt Ena	ble bit			
	1 = Enables	the MSSP Bus	Collision Inter	rrupt			
	0 = Disables	the MSSP Bus	Collision Inte	errupt			
bit 2-1	Unimplemen	ted: Read as '	0'				
bit 0	CCP2IE: CCF	P2 Interrupt En	able bit				
1 = Enables the CCP2 interrupt							
	0 = Disables	the CCP2 inter	rrupt				
Note: Bit	t PEIE of the IN	TCON register	must be				

PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2 REGISTER 7-3:

set to enable any peripheral interrupt.

10.1 Independent Clock Source

The WDT derives its time base from the 31 kHz LFINTOSC internal oscillator. Time intervals in this chapter are based on a nominal interval of 1 ms. See **Section 25.0 "Electrical Specifications"** for the LFINTOSC tolerances.

10.2 WDT Operating Modes

The Watchdog Timer module has four operating modes controlled by the WDTE<1:0> bits in Configuration Words. See Table .

10.2.1 WDT IS ALWAYS ON

When the WDTE bits of Configuration Words are set to '11', the WDT is always ON.

WDT protection is active during Sleep.

10.2.2 WDT IS OFF IN SLEEP

When the WDTE bits of Configuration Words are set to '10', the WDT is ON, except in Sleep.

WDT protection is not active during Sleep.

10.2.3 WDT CONTROLLED BY SOFTWARE

When the WDTE bits of Configuration Words are set to '01', the WDT is controlled by the SWDTEN bit of the WDTCON register.

WDT protection is unchanged by Sleep. See Table for more details.

TABLE 10-1:	WDT OPERATING MODES
-------------	---------------------

WDTE<1:0>	SWDTE N	Device Mode	WDT Mode
11	Х	Х	Active
1.0	v	Awake	Active
ΤŪ	X	Sleep	Disabled
01	1	v	Active
UI	0	^	Disabled
00	Х	Х	Disabled

10.3 Time-Out Period

The WDTPS bits of the WDTCON register set the time-out period from 1 ms to 256 seconds (nominal). After a Reset, the default time-out period is two seconds.

10.4 Clearing the WDT

The WDT is cleared when any of the following conditions occur:

- Any Reset
- CLRWDT instruction is executed
- · Device enters Sleep
- · Device wakes up from Sleep
- Oscillator fail
- WDT is disabled
- Oscillator Start-up Timer (OST) is running

See Table 10-2 for more information.

10.5 Operation During Sleep

When the device enters Sleep, the WDT is cleared. If the WDT is enabled during Sleep, the WDT resumes counting.

When the device exits Sleep, the WDT is cleared again. The WDT remains clear until the OST, if enabled, completes. See **Section 5.0** "Oscillator **Module (with Fail-Safe Clock Monitor)**" for more information on the OST.

When a WDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the device wakes up and resumes operation. The TO and PD bits in the STATUS register are changed to indicate the event. The RWDT bit in the PCON register can also be used. See **Section 3.0** "**Memory Organization**" and The STATUS register (Register 3-1) for more information.

TABLE 10-2: WDT CLEARING CONDITIONS

Conditions	WDT		
WDTE<1:0> = 00			
WDTE<1:0> = 01 and SWDTEN = 0			
WDTE<1:0> = 10 and enter Sleep	Cleared		
CLRWDT Command	Cleared		
Oscillator Fail Detected			
Exit Sleep + System Clock = SOSC, EXTRC, INTOSC, EXTCLK			
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST		
Change INTOSC divider (IRCF bits)	Unaffected		

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11.3 Modifying Flash Program Memory

When modifying existing data in a program memory row, and data within that row must be preserved, it must first be read and saved in a RAM image. Program memory is modified using the following steps:

- 1. Load the starting address of the row to be modified.
- 2. Read the existing data from the row into a RAM image.
- 3. Modify the RAM image to contain the new data to be written into program memory.
- 4. Load the starting address of the row to be rewritten.
- 5. Erase the program memory row.
- 6. Load the write latches with data from the RAM image.
- 7. Initiate a programming operation.

FIGURE 11-7: FLASH PROGRAM MEMORY MODIFY FLOWCHART



U-1	R/W-0/0	R/W-0/0	R/W/HC-0/0	R/W/HC-x/q ⁽²⁾	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0
(1	CFGS	LWLO	FREE	WRERR	WREN	WR	RD
bit 7						·	bit C
Legend:							
R = Read	able bit	W = Writable b	it	U = Unimpleme	ented bit, read as	s '0'	
S = Bit ca	n only be set	x = Bit is unkno	own	-n/n = Value at	POR and BOR/	/alue at all other I	Resets
'1' = Bit is	set	'0' = Bit is clear	red	HC = Bit is clea	ared by hardware	9	
hit 7	Unimplemen	tad. Pead as '1'					
bit 6	CECS. Confi	nuration Soloot bit					
DILO	1 = Access	Configuration Use	er ID and Device	ID Registers			
	0 = Access	Flash program me	mory	12 Registere			
bit 5	LWLO: Load	Write Latches Onl	y bit ⁽³⁾				
	1 = Only the	addressed progra	am memory write	e latch is loaded/	updated on the r	next WR comman	d
	0 = The add	ressed program m	emory write latcl	h is loaded/updat	ed and a write of	all program mem	ory write latche
	will be in	nitiated on the next	t WR command				
bit 4	FREE: Progra	am Flash Erase Ei	nable bit				
	1 = Perform 0 = Perform	s an erase operati s an write operatic	on on the next v on on the next W	VR command (ha /R command	ardware cleared	upon completion)	
bit 3	WRERR: Pro	gram/Frase Error	Flag bit				
2.1.0	1 = Conditio	n indicates an imp	proper program	or erase sequen	ce attempt or te	rmination (bit is s	et automatically
	on any s	et attempt (write	1') of the WR bit	:).	·	,	-
	0 = The prog	gram or erase ope	ration complete	d normally.			
bit 2	WREN: Prog	ram/Erase Enable	bit				
	1 = Allows p	orogram/erase cycl	es				
L:1 4		orogramming/eras	ing of program r	-18511			
DIC		a program Elash r	rogram/oraso o	poration			
	The ope	ration is self-timed	and the bit is c	leared by hardwa	are once operatio	on is complete.	
	The WR	bit can only be se	et (not cleared) in	n software.		F	
	0 = Program	n/erase operation t	to the Flash is co	omplete and inac	tive.		
bit 0	RD: Read Co	ontrol bit					
	1 = Initiates (not clea	a program Flash r ared) in software.	ead. Read takes	s one cycle. RD i	s cleared in hard	lware. The RD bit	can only be set
	0 = Does no	ot initiate a program	n Flash read.				
Note 1:	Unimplemented bit	, read as '1'.					
2:	The WRERR bit is	automatically set b	y hardware whe	en a program me	mory write or era	se operation is st	arted (WR = 1)

REGISTER 11-6: PMCON1: PROGRAM MEMORY CONTROL 1 REGISTER

3: The LWLO bit is ignored during a program memory erase operation (FREE = 1).

18.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

18.4 Secondary Oscillator

Timer1 uses the low-power secondary oscillator circuit on pins SOSCI and SOSCO. The secondary oscillator is designed to use an external 32.768 kHz crystal.

The secondary oscillator circuit is enabled by setting the T1OSCEN bit of the T1CON register. The oscillator will continue to run during Sleep.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to using Timer1. A suitable delay similar to the OST delay can be implemented in software by clearing the TMR1IF bit then presetting the TMR1H:TMR1L register pair to FC00h. The TMR1IF flag will be set when 1024 clock cycles have elapsed, thereby indicating that the oscillator is running and reasonably stable.

18.5 Timer1 Operation in Asynchronous Counter Mode

If control bit T1SYNC of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see Section 18.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode").

Note: When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

18.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

18.6 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 gate circuitry. This is also referred to as Timer1 Gate Enable.

Timer1 gate can also be driven by multiple selectable sources.

18.6.1 TIMER1 GATE ENABLE

The Timer1 Gate Enable mode is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 Gate Enable mode is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate Enable mode is enabled, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 Gate Enable mode is disabled, no incrementing will occur and Timer1 will hold the current count. See Figure 18-3 for timing details.

TABLE 18-3: TIMER1 GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer1 Operation
\uparrow	0	0	Counts
\uparrow	0	1	Holds Count
\uparrow	1	0	Holds Count
\uparrow	1	1	Counts

18.6.2 TIMER1 GATE SOURCE SELECTION

The Timer1 gate source can be selected from one of four different sources. Source selection is controlled by the T1GSS bits of the T1GCON register. The polarity for each available source is also selectable. Polarity selection is controlled by the T1GPOL bit of the T1GCON register.



FIGURE 18-4: TIMER1 GATE TOGGLE MODE







21.2 SPI Mode Overview

The Serial Peripheral Interface (SPI) bus is a synchronous serial data communication bus that operates in Full-Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a Chip Select known as Slave Select.

The SPI bus specifies four signal connections:

- Serial Clock (SCK)
- Serial Data Out (SDO)
- Serial Data In (SDI)
- Slave Select (SS)

Figure 21-1 shows the block diagram of the MSSP module when operating in SPI mode.

The SPI bus operates with a single master device and one or more slave devices. When multiple slave devices are used, an independent Slave Select connection is required from the master device to each slave device.

Figure 21-4 shows a typical connection between a master device and multiple slave devices.

The master selects only one slave at a time. Most slave devices have tri-state outputs so their output signal appears disconnected from the bus when they are not selected. Transmissions involve two shift registers, eight bits in size, one in the master and one in the slave. With either the master or the slave device, data is always shifted out one bit at a time, with the Most Significant bit (MSb) shifted out first. At the same time, a new Least Significant bit (LSb) is shifted into the same register.

Figure 21-5 shows a typical connection between two processors configured as master and slave devices.

Data is shifted out of both shift registers on the programmed clock edge and latched on the opposite edge of the clock.

The master device transmits information out on its SDO output pin which is connected to, and received by, the slave's SDI input pin. The slave device transmits information out on its SDO output pin, which is connected to, and received by, the master's SDI input pin.

To begin communication, the master device first sends out the clock signal. Both the master and the slave devices should be configured for the same clock polarity.

The master device starts a transmission by sending out the MSb from its shift register. The slave device reads this bit from that same line and saves it into the LSb position of its shift register.





21.6.6 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPBUF register. This action will set the Buffer Full flag bit, BF and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted. SCL is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCL is released high. When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the 8th bit is shifted out (the falling edge of the 8th clock), the BF flag is cleared and the master releases SDA. This allows the slave device being addressed to respond with an \overline{ACK} bit during the 9th bit time if an address match occurred, or if data was received properly. The status of ACK is written into the ACKSTAT bit on the rising edge of the 9th clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the 9th clock, the SSPIF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPBUF, leaving SCL low and SDA unchanged (Figure 21-28).

After the write to the SSPBUF, each bit of the address will be shifted out on the falling edge of SCL until all seven address bits and the R/W bit are completed. On the falling edge of the 8th clock, the master will release the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the 9th clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT Status bit of the SSPCON2 register. Following the falling edge of the 9th clock transmission of the address, the SSPIF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPBUF takes place, holding SCL low and allowing SDA to float.

21.6.6.1 BF Status Flag

In Transmit mode, the BF bit of the SSPSTAT register is set when the CPU writes to SSPBUF and is cleared when all eight bits are shifted out.

21.6.6.2 WCOL Status Flag

If the user writes the SSPBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

WCOL must be cleared by software before the next transmission.

21.6.6.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit of the SSPCON2 register is cleared when the slave has sent an Acknowledge (ACK = 0) and is set when the slave does not Acknowledge (ACK = 1). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

21.6.6.4 Typical transmit sequence:

- 1. The user generates a Start condition by setting the SEN bit of the SSPCON2 register.
- 2. SSPIF is set by hardware on completion of the Start.
- 3. SSPIF is cleared by software.
- 4. The MSSP module will wait the required start time before any other operation takes place.
- 5. The user loads the SSPBUF with the slave address to transmit.
- 6. Address is shifted out the SDA pin until all 8 bits are transmitted. Transmission begins as soon as SSPBUF is written to.
- The MSSP module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
- 8. The MSSP module generates an interrupt at the end of the 9th clock cycle by setting the SSPIF bit.
- 9. The user loads the SSPBUF with eight bits of data.
- 10. Data is shifted out the SDA pin until all eight bits are transmitted.
- 11. The MSSP module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
- 12. Steps 8-11 are repeated for all transmitted data bytes.
- 13. The user generates a Stop or Restart condition by setting the PEN or RSEN bits of the SSPCON2 register. Interrupt is generated once the Stop/Restart condition is complete.

21.6.7 I²C MASTER MODE RECEPTION

Master mode reception (Figure 21-29) is enabled by programming the Receive Enable bit, RCEN bit of the SSPCON2 register.

Note:	The MSSP module must be in an Idle
	state before the RCEN bit is set or the
	RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSPSR. After the falling edge of the 8th clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag bit is set, the SSPIF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSPCON2 register.

21.6.7.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

21.6.7.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when eight bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

21.6.7.3 WCOL Status Flag

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

21.6.7.4 Typical Receive Sequence:

- 1. The user generates a Start condition by setting the SEN bit of the SSPCON2 register.
- 2. SSPIF is set by hardware on completion of the Start.
- 3. SSPIF is cleared by software.
- 4. User writes SSPBUF with the slave address to transmit and the R/W bit set.
- 5. Address is shifted out the SDA pin until all 8 bits are transmitted. Transmission begins as soon as SSPBUF is written to.
- 6. The MSSP module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
- 7. The MSSP module generates an interrupt at the end of the 9th clock cycle by setting the SSPIF bit.
- 8. User sets the RCEN bit of the SSPCON2 register and the master clocks in a byte from the slave.
- 9. After the 8th falling edge of SCL, SSPIF and BF are set.
- 10. Master clears SSPIF and reads the received byte from SSPUF, clears BF.
- 11. Master sets ACK value sent to slave in ACKDT bit of the SSPCON2 register and initiates the ACK by setting the ACKEN bit.
- 12. Masters ACK is clocked out to the slave and SSPIF is set.
- 13. User clears SSPIF.
- 14. Steps 8-13 are repeated for each received byte from the slave.
- 15. Master sends a not ACK or Stop to end communication.

21.7 BAUD RATE GENERATOR

The MSSP module has a Baud Rate Generator available for clock generation in both I^2C and SPI Master modes. The Baud Rate Generator (BRG) reload value is placed in the SSPADD register (Register 21-8). When a write occurs to SSPBUF, the Baud Rate Generator will automatically begin counting down.

Once the given operation is complete, the internal clock will automatically stop counting and the clock pin will remain in its last state.

An internal signal "Reload" in Figure 21-40 triggers the value from SSPADD to be loaded into the BRG counter. This occurs twice for each oscillation of the module

clock line. The logic dictating when the reload signal is asserted depends on the mode the MSSP is being operated in.

Table 21-2 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPADD.

EQUATION 21-1: BRG CLOCK FREQUENCY

$$FCLOCK = \frac{FOSC}{(SSPxADD+1)(4)}$$

FIGURE 21-40: BAUD RATE GENERATOR BLOCK DIAGRAM



Note: Values of 0x00, 0x01 and 0x02 are not valid for SSPADD when used as a Baud Rate Generator for I²C. This is an implementation limitation.

TABLE 21-2: MSSP CLOCK RATE W/BRG

Fosc	Fcy	BRG Value	FcLock (2 Rollovers of BRG)
16 MHz	4 MHz	09h	400 kHz ⁽¹⁾
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note 1: The I²C interface does not conform to the 400 kHz I²C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	232
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	74
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	75
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	77
RCREG			EUS	ART Receiv	e Data Reg	gister			225*
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	231
SPBRGL	BRG<7:0>								
SPBRGH	BRG<15:8>								
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	114
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	230

TABLE 22-2: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Legend: — = unimplemented, read as '0'. Shaded cells are not used for asynchronous reception.

* Page provides register information.

	SYNC = 0, BRGH = 1, BRG16 = 0												
BAUD	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fos	Fosc = 1.000 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	
300	—	_		_	_	_	_	_	_	300	0.16	207	
1200	—	_	_	1202	0.16	207	1200	0.00	191	1202	0.16	51	
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25	
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	—	—	_	
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5	
19.2k	19231	0.16	25	19.23k	0.16	12	19.2k	0.00	11	—	—	_	
57.6k	55556	-3.55	8	—	—	—	57.60k	0.00	3	—	—	_	
115.2k	—	—	_	—	—	_	115.2k	0.00	1	_	—		

TABLE 22-4: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 1											
	Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 16.000 MHz			Fosc = 11.0592 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	-0.01	4166	300.0	0.00	3839	300.03	0.01	3332	300.0	0.00	2303
1200	1200	-0.03	1041	1200	0.00	959	1200.5	0.04	832	1200	0.00	575
2400	2399	-0.03	520	2400	0.00	479	2398	-0.08	416	2400	0.00	287
9600	9615	0.16	129	9600	0.00	119	9615	0.16	103	9600	0.00	71
10417	10417	0.00	119	10378	-0.37	110	10417	0.00	95	10473	0.53	65
19.2k	19.23k	0.16	64	19.20k	0.00	59	19.23k	0.16	51	19.20k	0.00	35
57.6k	56.818	-1.36	21	57.60k	0.00	19	58.82k	2.12	16	57.60k	0.00	11
115.2k	113.636	-1.36	10	115.2k	0.00	9	111.11k	-3.55	8	115.2k	0.00	5

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 1											
	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	299.9	-0.02	1666	300.1	0.04	832	300.0	0.00	767	300.5	0.16	207
1200	1199	-0.08	416	1202	0.16	207	1200	0.00	191	1202	0.16	51
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	—	_	_
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5
19.2k	19.23k	0.16	25	19.23k	0.16	12	19.20k	0.00	11	—	_	_
57.6k	55556	-3.55	8	_	_	_	57.60k	0.00	3	_	_	_
115.2k		_	_	_	_	_	115.2k	0.00	1	_	_	_



FIGURE 26-40: IPD, SECONDARY OSCILLATOR, Fosc = 32 kHz, PIC16F1516/7/8/9 ONLY



28.0 PACKAGING INFORMATION

28.1 Package Marking Information



Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.