Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1516t-i-ss

TABLE 1: 28/40/44-PIN ALLOCATION TABLE

I/O	28-Pin SPDIP, SOIC, SSOP	28-Pin QFN, UQFN	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	ADC	Timers	CCP	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	2	27	2	17	19	AN0	—	—	—	$\overline{SS}$(2)	—	—	—
RA1	3	28	3	18	20	AN1	—	—	—	—	—	—	—
RA2	4	1	4	19	21	AN2	—	—	—	—	—	—	—
RA3	5	2	5	20	22	AN3/VREF+	—	—	—	—	—	—	—
RA4	6	3	6	21	23	—	T0CKI	—	—	—	—	—	—
RA5	7	4	7	22	24	AN4	—	—	—	$\overline{SS}$(1)	—	—	VCAP
RA6	10	7	14	29	31	—	—	—	—	—	—	—	OSC2/CLKOUT
RA7	9	6	13	28	30	—	—	—	—	—	—	—	OSC1/CLKIN
RB0	21	18	33	8	8	AN12	—	—	—	—	INT/IOC	Y	—
RB1	22	19	34	9	9	AN10	—	—	—	—	IOC	Y	—
RB2	23	20	35	10	10	AN8	—	—	—	—	IOC	Y	—
RB3	24	21	36	11	11	AN9	—	CCP2(2)	—	—	IOC	Y	—
RB4	25	22	37	12	14	AN11	—	—	—	—	IOC	Y	—
RB5	26	23	38	13	15	AN13	T1G	—	—	—	IOC	Y	—
RB6	27	24	39	14	16	—	—	—	—	—	IOC	Y	ICSPCLK/ICDCLK
RB7	28	25	40	15	17	—	—	—	—	—	IOC	Y	ICSPDAT/ICDDAT
RC0	11	8	15	30	32	—	SOSCO/T1CKI	—	—	—	—	—	—
RC1	12	9	16	31	35	—	SOSCI	CCP2(1)	—	—	—	—	—
RC2	13	10	17	32	36	AN14	—	CCP1	—	—	—	—	—
RC3	14	11	18	33	37	AN15	—	—	—	SCK/SCL	—	—	—
RC4	15	12	23	38	42	AN16	—	—	—	SDI/SDA	—	—	—
RC5	16	13	24	39	43	AN17	—	—	—	SDO	—	—	—
RC6	17	14	25	40	44	AN18	—	—	TX/CK	—	—	—	—
RC7	18	15	26	1	1	AN19	—	—	RX/DT	—	—	—	—
RD0(3)	—	—	19	34	38	AN20	—	—	—	—	—	—	—
RD1(3)	—	—	20	35	39	AN21	—	—	—	—	—	—	—
RD2(3)	—	—	21	36	40	AN22	—	—	—	—	—	—	—
RD3(3)	—	—	22	37	41	AN23	—	—	—	—	—	—	—
RD4(3)	—	—	27	2	2	AN24	—	—	—	—	—	—	—
RD5(3)	—	—	28	3	3	AN25	—	—	—	—	—	—	—
RD6(3)	—	—	29	4	4	AN26	—	—	—	—	—	—	—
RD7(3)	—	—	30	5	5	AN27	—	—	—	—	—	—	—
RE0(3)	—	—	8	23	25	AN5	—	—	—	—	—	—	—
RE1(3)	—	—	9	24	26	AN6	—	—	—	—	—	—	—
RE2(3)	—	—	10	25	27	AN7	—	—	—	—	—	—	—
RE3	1	26	1	16	18	—	—	—	—	—	—	Y	$\overline{MCLR}$/VPP
VDD	20	17	11, 32	7, 26	7, 28	—	—	—	—	—	—	—	—
VSS	8, 19	5, 16	12, 31	6, 27	6, 29	—	—	—	—	—	—	—	—
NC	—	—	—	—	12, 13, 33, 34	—	—	—	—	—	—	—	—

Note 1: Peripheral pin location selected using APFCON register. Default location.

2: Peripheral pin location selected using APFCON register. Alternate location.

3: PIC16(L)F1517/9 only.

3.4.6 SPECIAL FUNCTION REGISTERS SUMMARY

The Special Function registers are listed in Table 3-8.

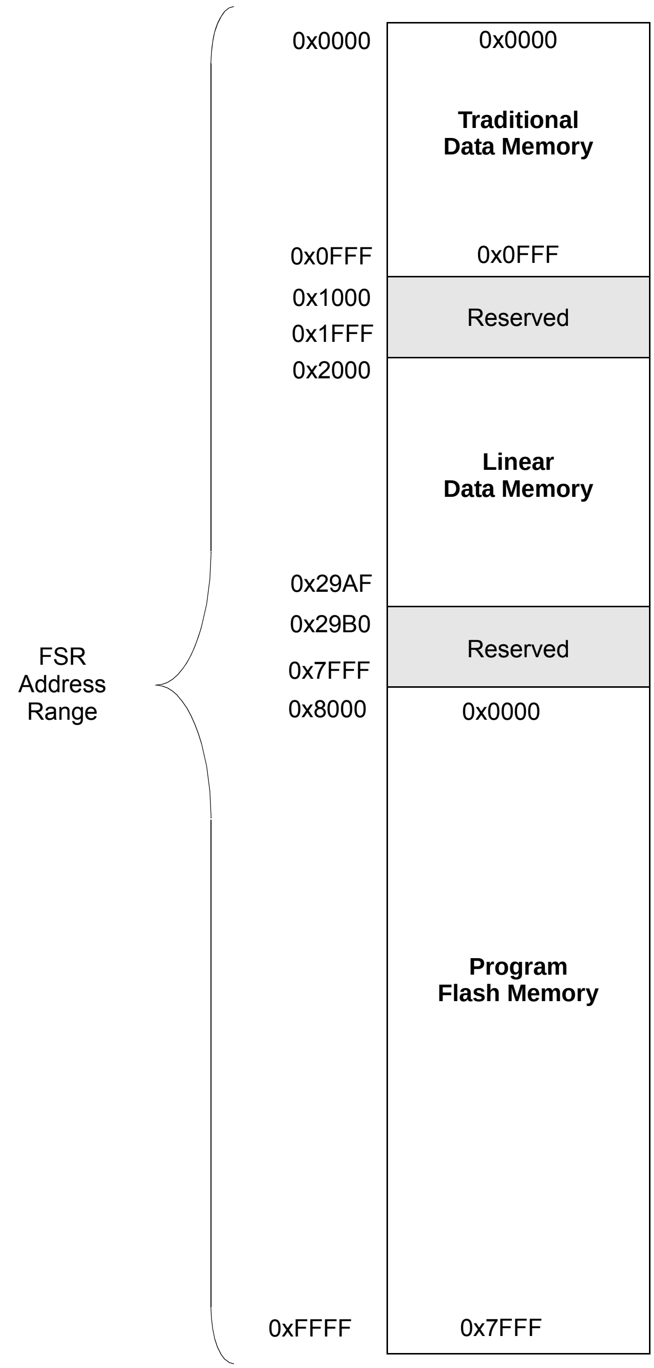
TABLE 3-8: SPECIAL FUNCTION REGISTER SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 0											
00Ch	PORTA	PORTA Data Latch when written: PORTA pins when read								`xxxx xxxx`	`uuuu uuuu`
00Dh	PORTB	PORTB Data Latch when written: PORTB pins when read								`xxxx xxxx`	`uuuu uuuu`
00Eh	PORTC	PORTC Data Latch when written: PORTC pins when read								`xxxx xxxx`	`uuuu uuuu`
00Fh	PORTD	PORTD Data Latch when written: PORTD pins when read								`xxxx xxxx`	`uuuu uuuu`
010h	PORTE	—	—	—	—	RE3	RE2[3]	RE1[3]	RE0[3]	`---- xxxx`	`---- uuuu`
011h	PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	`0000 0000`	`0000 0000`
012h	PIR2	OSFIF	—	—	—	BCLIF	—	—	CCP2IF	`0--- 0--0`	`0--- 0--0`
013h	—	Unimplemented								—	—
014h	—	Unimplemented								—	—
015h	TMR0	Holding Register for the 8-bit Timer0 Count								`xxxx xxxx`	`uuuu uuuu`
016h	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Count								`xxxx xxxx`	`uuuu uuuu`
017h	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Count								`xxxx xxxx`	`uuuu uuuu`
018h	T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	`0000 00-0`	`uuuu uu-u`
019h	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>		`0000 0x00`	`uuuu uxuu`
01Ah	TMR2	Timer 2 Module Register								`0000 0000`	`0000 0000`
01Bh	PR2	Timer 2 Period Register								`1111 1111`	`1111 1111`
01Ch	T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		`-000 0000`	`-000 0000`
01Dh	—	Unimplemented								—	—
01Eh	—	Unimplemented								—	—
01Fh	—	Unimplemented								—	—
Bank 1											
08Ch	TRISA	PORTA Data Direction Register								`1111 1111`	`1111 1111`
08Dh	TRISB	PORTB Data Direction Register								`1111 1111`	`1111 1111`
08Eh	TRISC	PORTC Data Direction Register								`1111 1111`	`1111 1111`
08Fh	TRISD[2]	PORTD Data Direction Register								`1111 1111`	`1111 1111`
090h	TRISE	—	—	—	—	—[3]	TRISE2[2]	TRISE1[2]	TRISE0[2]	`---- 1111`	`---- 1111`
091h	PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	`0000 0000`	`0000 0000`
092h	PIE2	OSFIE	—	—	—	BCLIE	—	—	CCP2IE	`0--- 0--0`	`0--- 0--0`
093h	—	Unimplemented								—	—
094h	—	Unimplemented								—	—
095h	OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			`1111 1111`	`1111 1111`
096h	PCON	STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	`00-1 11qq`	`qq-q qquu`
097h	WDTCON	—	—	WDTPS<4:0>					SWDTEN	`--01 0110`	`--01 0110`
098h	—	Unimplemented								—	—
099h	OSCCON	—	IRCF<3:0>				—	SCS<1:0>		`-011 1-00`	`-011 1-00`
09Ah	OSCSTAT	SOSCR	—	OSTS	HFIOFR	—	—	LFIOFR	HFIOFS	`0-q0 --00`	`q-qq --0q`
09Bh	ADRESL	ADC Result Register Low								`xxxx xxxx`	`uuuu uuuu`
09Ch	ADRESH	ADC Result Register High								`xxxx xxxx`	`uuuu uuuu`
09Dh	ADCON0	—	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON	`-000 0000`	`-000 0000`
09Eh	ADCON1	ADFM	ADCS<2:0>			—	—	ADPREF<1:0>		`0000 --00`	`0000 --00`
09Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: PIC16F1516/7/8/9 only.
2: PIC16(L)F1517/9 only.
3: Unimplemented, read as '1'.

FIGURE 3-9: INDIRECT ADDRESSING



Note: Not all memory regions are completely implemented. Consult device memory tables for memory limits.

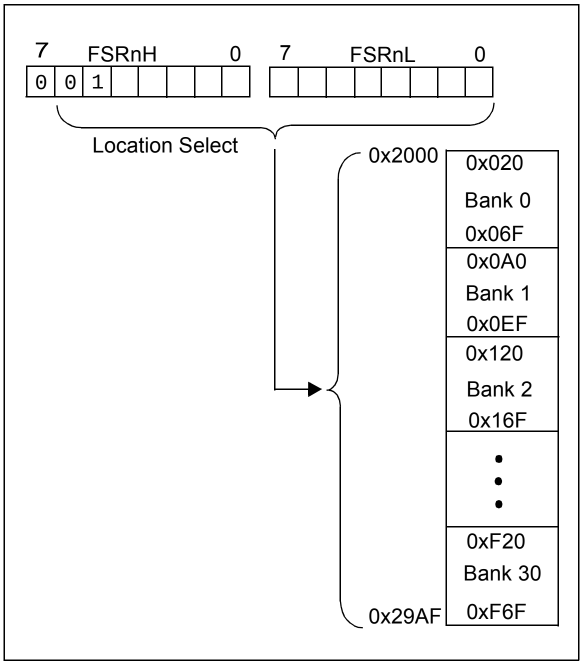
3.7.2 LINEAR DATA MEMORY

The linear data memory is the region from FSR address 0x2000 to FSR address 0x29AF. This region is a virtual region that points back to the 80-byte blocks of GPR memory in all the banks.

Unimplemented memory reads as 0x00. Use of the linear data memory region allows buffers to be larger than 80 bytes because incrementing the FSR beyond one bank will go directly to the GPR memory of the next bank.

The 16 bytes of common memory are not included in the linear data memory region.

FIGURE 3-11: LINEAR DATA MEMORY MAP



3.7.3 PROGRAM FLASH MEMORY

To make constant data access easier, the entire program Flash memory is mapped to the upper half of the FSR address space. When the MSB of FSRnH is set, the lower 15 bits are the address in program memory which will be accessed through INDF. Only the lower eight bits of each memory location is accessible via INDF. Writing to the program Flash memory cannot be accomplished via the FSR/INDF interface. All instructions that access program Flash memory via the FSR/INDF interface will require one additional instruction cycle to complete.

FIGURE 3-12: PROGRAM FLASH MEMORY MAP

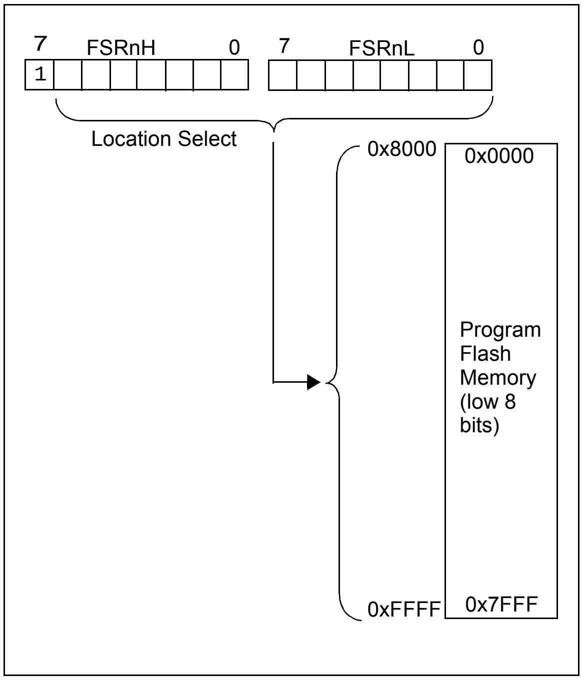
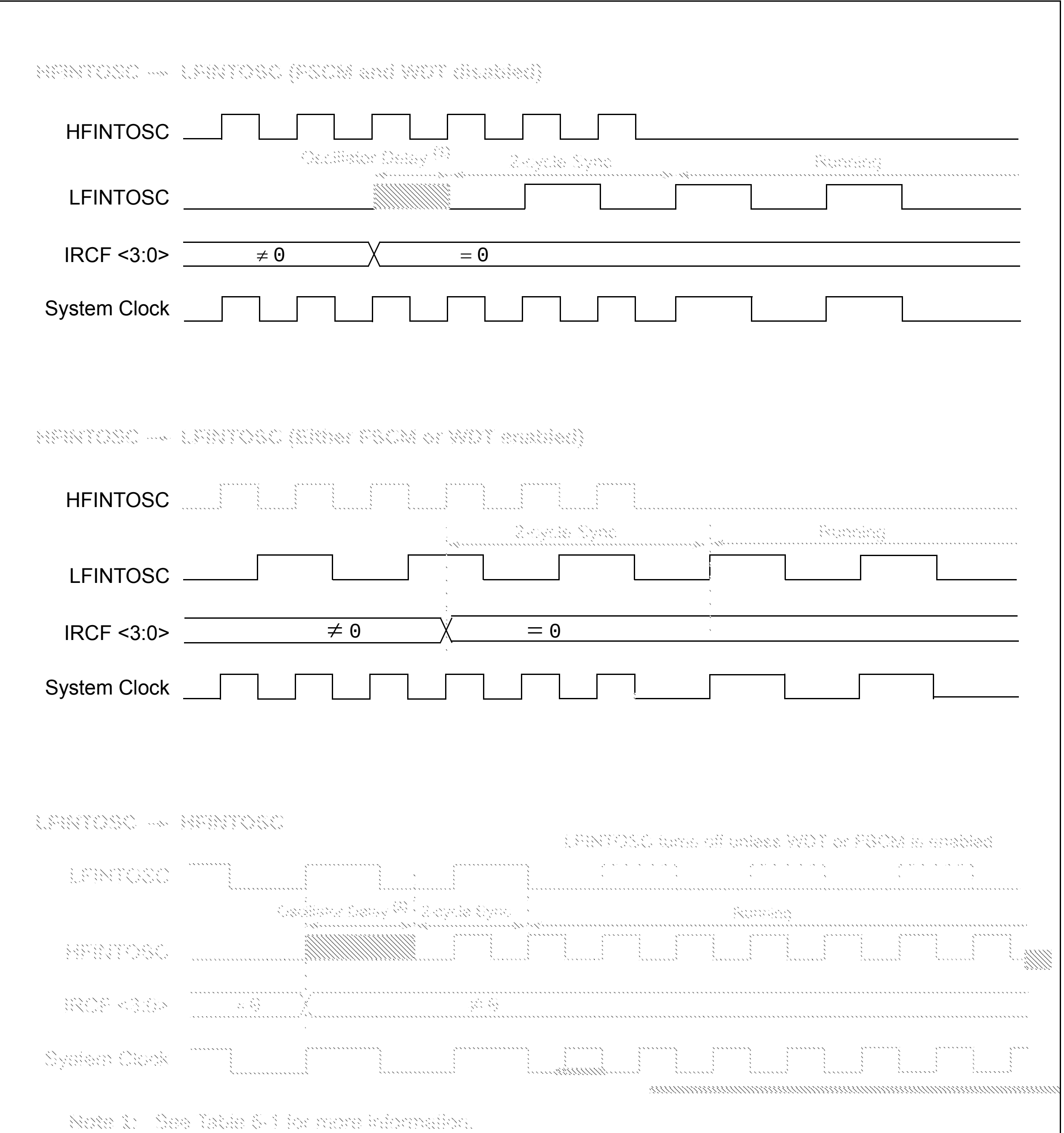


FIGURE 5-7: INTERNAL OSCILLATOR SWITCH TIMING



5.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bits of the OSCCON register. The following clock sources can be selected using the SCS bits:

- Default system oscillator determined by FOSC bits in Configuration Words
- Secondary oscillator 32 kHz crystal
- Internal Oscillator Block (INTOSC)

5.3.1 SYSTEM CLOCK SELECT (SCS) BITS

The System Clock Select (SCS) bits of the OSCCON register selects the system clock source that is used for the CPU and peripherals.

- When the SCS bits of the OSCCON register = `00`, the system clock source is determined by value of the FOSC<2:0> bits in the Configuration Words.
- When the SCS bits of the OSCCON register = `01`, the system clock source is the secondary oscillator.
- When the SCS bits of the OSCCON register = `1x`, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<3:0> bits of the OSCCON register. After a Reset, the SCS bits of the OSCCON register are always cleared.

> **Note:** Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bits of the OSCCON register. The user can monitor the OSTS bit of the OSCSTAT register to determine the current system clock source.

When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 5-1.

5.3.2 OSCILLATOR START-UP TIMER STATUS (OSTS) BIT

The Oscillator Start-up Timer Status (OSTS) bit of the OSCSTAT register indicates whether the system clock is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Words, or from the internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes. The OSTS does not reflect the status of the secondary oscillator.

5.3.3 SECONDARY OSCILLATOR

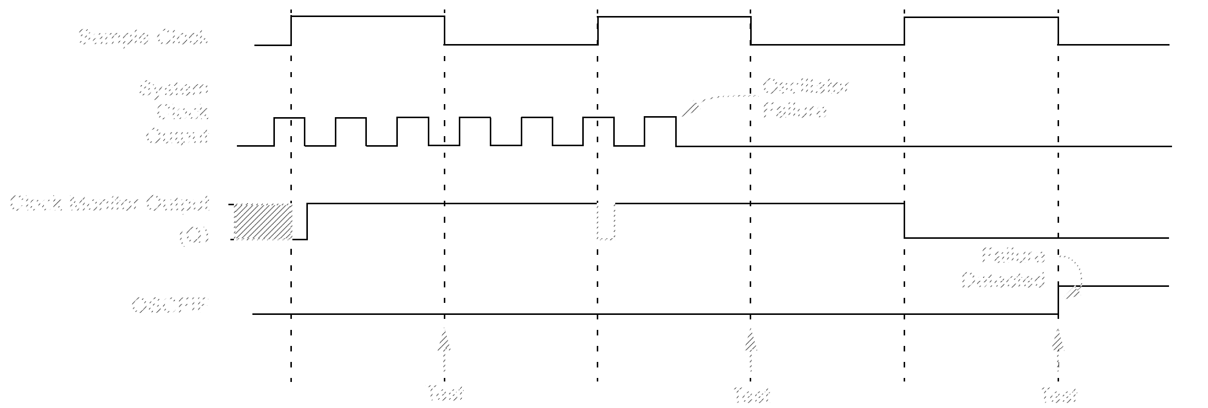
The secondary oscillator is a separate crystal oscillator associated with the Timer1 peripheral. It is optimized for timekeeping operations with a 32.768 kHz crystal connected between the SOSCO and SOSCI device pins.

The secondary oscillator is enabled using the T1OSCEN control bit in the T1CON register. See **Section 18.0 “Timer1 Module with Gate Control”** for more information about the Timer1 peripheral.

5.3.4 SECONDARY OSCILLATOR READY (SOSCR) BIT

The user must ensure that the secondary oscillator is ready to be used before it is selected as a system clock source. The Secondary Oscillator Ready (SOSCR) bit of the OSCSTAT register indicates whether the secondary oscillator is ready to be used. After the SOSCR bit is set, the SCS bits can be configured to select the secondary oscillator.

FIGURE 5-10: FSCM TIMING DIAGRAM



Note: The system clock is normally at a much higher frequency than the sample clock. The relative frequencies in this example have been chosen for clarity.

7.1 Operation

Interrupts are disabled upon any device Reset. They are enabled by setting the following bits:

- GIE bit of the INTCON register
- Interrupt Enable bit(s) for the specific interrupt event(s)
- PEIE bit of the INTCON register (if the Interrupt Enable bit of the interrupt event is contained in the PIEx register)

The INTCON, PIR1 and PIR2 registers record individual interrupts via interrupt flag bits. Interrupt flag bits will be set, regardless of the status of the GIE, PEIE and individual interrupt enable bits.

The following events happen when an interrupt event occurs while the GIE bit is set:

- Current prefetched instruction is flushed
- GIE bit is cleared
- Current Program Counter (PC) is pushed onto the stack
- Critical registers are automatically saved to the shadow registers (See **Section 7.5 "Automatic Context Saving"**)
- PC is loaded with the interrupt vector 0004h

The firmware within the Interrupt Service Routine (ISR) should determine the source of the interrupt by polling the interrupt flag bits. The interrupt flag bits must be cleared before exiting the ISR to avoid repeated interrupts. Because the GIE bit is cleared, any interrupt that occurs while executing the ISR will be recorded through its interrupt flag, but will not cause the processor to redirect to the interrupt vector.

The `RETFIE` instruction exits the ISR by popping the previous address from the stack, restoring the saved context from the shadow registers and setting the GIE bit.

For additional information on a specific interrupt's operation, refer to its peripheral chapter.

Note 1:	Individual interrupt flag bits are set, regardless of the state of any other enable bits.
2:	All interrupts will be ignored while the GIE bit is cleared. Any interrupt occurring while the GIE bit is clear will be serviced when the GIE bit is set again.

7.2 Interrupt Latency

Interrupt latency is defined as the time from when the interrupt event occurs to the time code execution at the interrupt vector begins. The latency for synchronous interrupts is three or four instruction cycles. For asynchronous interrupts, the latency is three to five instruction cycles, depending on when the interrupt occurs. See Figure 7-2 and Figure 7-3 for more details.

REGISTER 7-3: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

R/W-0/0	U-0	U-0	U-0	R/W-0/0	U-0	U-0	R/W-0/0
OSFIE	—	—	—	BCLIE	—	—	CCP2IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **OSFIE:** Oscillator Fail Interrupt Enable bit
1 = Enables the Oscillator Fail interrupt
0 = Disables the Oscillator Fail interrupt

bit 6-4 **Unimplemented:** Read as ‘0’

bit 3 **BCLIE:** MSSP Bus Collision Interrupt Enable bit
1 = Enables the MSSP Bus Collision Interrupt
0 = Disables the MSSP Bus Collision Interrupt

bit 2-1 **Unimplemented:** Read as ‘0’

bit 0 **CCP2IE:** CCP2 Interrupt Enable bit
1 = Enables the CCP2 interrupt
0 = Disables the CCP2 interrupt

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

16.2.6 ADC CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
   - Disable pin output driver (Refer to the TRIS register)
   - Configure pin as analog (Refer to the ANSEL register)
   - Disable weak pull-ups, either globally (Refer to the OPTION_REG register) or individually (Refer to the appropriate WPUx register)
2. Configure the ADC module:
   - Select ADC conversion clock
   - Configure voltage reference
   - Select ADC input channel
   - Turn on ADC module
3. Configure ADC interrupt (optional):
   - Clear ADC interrupt flag
   - Enable ADC interrupt
   - Enable peripheral interrupt
   - Enable global interrupt[1]
4. Wait the required acquisition time[2].
5. Start conversion by setting the GO/$\overline{\text{DONE}}$ bit.
6. Wait for ADC conversion to complete by one of the following:
   - Polling the GO/$\overline{\text{DONE}}$ bit
   - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result.
8. Clear the ADC interrupt flag (required if interrupt is enabled).

> **Note 1:** The global interrupt can be disabled if the user is attempting to wake up from Sleep and resume in-line code execution.
>
> **2:** Refer to **Section 16.4 "ADC Acquisition Requirements"**.

EXAMPLE 16-1: ADC CONVERSION

```
;This code block configures the ADC
;for polling, Vdd and Vss references, Frc
;clock and AN0 input.
;
;Conversion start & polling for completion
; are included.
;
BANKSEL   ADCON1       ;
MOVLW     B'11110000'  ;Right justify, Frc
                       ;clock
MOVWF     ADCON1       ;Vdd and Vss Vref
BANKSEL   TRISA        ;
BSF       TRISA,0      ;Set RA0 to input
BANKSEL   ANSEL        ;
BSF       ANSEL,0      ;Set RA0 to analog
BANKSEL   WPUA
BCF       WPUA, 0      ;Disable weak pull-
                       up on RA0
BANKSEL   ADCON0       ;
MOVLW     B'00000001'  ;Select channel AN0
MOVWF     ADCON0       ;Turn ADC On
CALL      SampleTime   ;Acquisiton delay
BSF       ADCON0,ADGO  ;Start conversion
BTFSC     ADCON0,ADGO  ;Is conversion done?
GOTO      $-1          ;No, test again
BANKSEL   ADRESH       ;
MOVF      ADRESH,W     ;Read upper 2 bits
MOVWF     RESULTHI     ;store in GPR space
BANKSEL   ADRESL       ;
MOVF      ADRESL,W     ;Read lower 8 bits
MOVWF     RESULTLO     ;Store in GPR space
```

REGISTER 16-5: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	—	—	—	ADRES<9:8>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Reserved**: Do not use.

bit 1-0 **ADRES<9:8>**: ADC Result Register bits
Upper two bits of 10-bit conversion result

REGISTER 16-6: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ADRES<7:0>**: ADC Result Register bits
Lower eight bits of 10-bit conversion result

22.3 Register Definitions: EUSART Control

REGISTER 22-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-1/1	R/W-0/0
CSRC	TX9	TXEN(1)	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Don’t care
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit(1)
1 = Transmit enabled
0 = Transmit disabled

bit 4 **SYNC:** EUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **SENDB:** Send Break Character bit
Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed
Synchronous mode:
Don’t care

bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0 **TX9D:** Ninth bit of Transmit Data
Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode.

TABLE 24-3: INSTRUCTION SET (CONTINUED)

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
CONTROL OPERATIONS									
BRA	k	Relative Branch	2	11	001k	kkkk	kkkk		
BRW	–	Relative Branch with W	2	00	0000	0000	1011		
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk		
CALLW	–	Call Subroutine with W	2	00	0000	0000	1010		
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
RETFIE	k	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	0100	kkkk	kkkk		
RETURN	–	Return from Subroutine	2	00	0000	0000	1000		
INHERENT OPERATIONS									
CLRWDT	–	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$, $\overline{PD}$	
NOP	–	No Operation	1	00	0000	0000	0000		
OPTION	–	Load OPTION_REG register with W	1	00	0000	0110	0010		
RESET	–	Software device Reset	1	00	0000	0000	0001		
SLEEP	–	Go into Standby mode	1	00	0000	0110	0011	$\overline{TO}$, $\overline{PD}$	
TRIS	f	Load TRIS register with W	1	00	0000	0110	0fff		
C-COMPILER OPTIMIZED									
ADDFSR	n, k	Add Literal k to FSRn	1	11	0001	0nkk	kkkk		
MOVIW	n mm	Move Indirect FSRn to W with pre/post inc/dec modifier, mm	1	00	0000	0001	0nmm	Z	**2, 3**
	k[n]	Move INDFn to W, Indexed Indirect.	1	11	1111	0nkk	kkkk	Z	**2**
MOVWI	n mm	Move W to Indirect FSRn with pre/post inc/dec modifier, mm	1	00	0000	0001	1nmm		**2, 3**
	k[n]	Move W to INDFn, Indexed Indirect.	1	11	1111	1nkk	kkkk		**2**

Note 1: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

2: If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.

3: See Table in the MOVIW and MOVWI instruction descriptions.

25.0 ELECTRICAL SPECIFICATIONS

25.1 Absolute Maximum Ratings(†)

Ambient temperature under bias .... -40°C to +125°C
Storage temperature .... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS}, PIC16F1516/7/8/9 .... -0.3V to +6.5V
Voltage on V_{DD} with respect to V_{SS}, PIC16LF1516/7/8/9 .... -0.3V to +4.0V
Voltage on $\overline{MCLR}$ with respect to Vss .... -0.3V to +9.0V
Voltage on all other pins with respect to V_{SS} .... -0.3V to (V_{DD} + 0.3V)
Total power dissipation(2) .... 800 mW
Maximum current

- on V_{SS} pin for 28-Pin devices(1)
  - -40°C ≤ T_A ≤ +85°C .... 350 mA
  - +85°C ≤ T_A ≤ +125°C .... 120 mA
- on V_{DD} pin for 28-Pin devices(1)
  - -40°C ≤ T_A ≤ +85°C .... 250 mA
  - +85°C ≤ T_A ≤ +125°C .... 85 mA
- on V_{SS} pin for 40/44-Pin devices(1)
  - -40°C ≤ T_A ≤ +85°C .... 350 mA
  - +85°C ≤ T_A ≤ +125°C .... 120 mA
- on V_{DD} pin for 40/44-Pin devices(1)
  - -40°C ≤ T_A ≤ +85°C .... 350 mA
  - +85°C ≤ T_A ≤ +125°C .... 120 mA

Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD}) .... ± 20 mA
Maximum output current sunk by any I/O pin .... 50 mA
Maximum output current sourced by any I/O pin .... 50 mA

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Table 25-5 to calculate device specifications.

2: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{Ol} \times I_{OL})$

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

25.4 DC Characteristics: Supply Current (IDD)

PIC16LF1516/7/8/9	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended
PIC16F1516/7/8/9	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions: VDD	Conditions: Note
	Supply Current (IDD)(1, 2, 3)						
D010		—	8.0	14	μA	1.8	FOSC = 32 kHz LP Oscillator -40°C ≤ TA ≤ +85°C
		—	12.0	31	μA	3.0	
D010		—	11	28	μA	2.3	FOSC = 32 kHz LP Oscillator -40°C ≤ TA ≤ +85°C
		—	13	38	μA	3.0	
		—	14	45	μA	5.0	
D011		—	60	95	μA	1.8	FOSC = 1 MHz XT Oscillator
		—	110	180	μA	3.0	
D011		—	92	170	μA	2.3	FOSC = 1 MHz XT Oscillator
		—	140	230	μA	3.0	
		—	170	350	μA	5.0	
D012		—	150	240	μA	1.8	FOSC = 4 MHz XT Oscillator
		—	260	430	μA	3.0	
D012		—	190	450	μA	2.3	FOSC = 4 MHz XT Oscillator
		—	310	500	μA	3.0	
		—	370	650	μA	5.0	
D013		—	25	31	μA	1.8	FOSC = 500 kHz EC Oscillator Low-Power mode
		—	35	50	μA	3.0	
D013		—	25	40	μA	2.3	FOSC = 500 kHz EC Oscillator Low-Power mode
		—	35	55	μA	3.0	
		—	40	60	μA	5.0	
D014		—	120	210	μA	1.8	FOSC = 4 MHz EC Oscillator Medium-Power mode
		—	210	380	μA	3.0	
D014		—	160	250	μA	2.3	FOSC = 4 MHz EC Oscillator Medium-Power mode
		—	260	380	μA	3.0	
		—	330	480	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: 0.1 μF capacitor on VCAP pin, PIC16F1516/7/8/9 only.

4: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

25.5 DC Characteristics: Power-Down Currents (IPD)

PIC16LF1516/7/8/9	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended
PIC16F1516/7/8/9	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Device Characteristics	Min.	Typ†	Max. +85°C	Max. +125°C	Units	Conditions VDD	Conditions Note
	Power-down Currents (IPD)(2, 4)							
D022	Base IPD	—	0.02	1.0	8.0	μA	1.8	WDT, BOR, FVR, and SOSC disabled, all Peripherals Inactive
		—	0.03	2.0	9.0	μA	3.0	
D022	Base IPD	—	0.20	3.0	10	μA	2.3	WDT, BOR, FVR, and SOSC disabled, all Peripherals Inactive, Low-power regulator active
		—	0.30	4.0	12	μA	3.0	
		—	0.47	6.0	15	μA	5.0	
D023		—	0.50	6.0	14	μA	1.8	LPWDT Current **(Note 1)**
		—	0.80	7.0	17	μA	3.0	
D023		—	0.50	6.0	15	μA	2.3	LPWDT Current **(Note 1)**
		—	0.77	7.0	20	μA	3.0	
		—	0.85	8.0	22	μA	5.0	
D023A		—	8.5	23	25	μA	1.8	FVR current **(Note 1)**
		—	8.5	24	27	μA	3.0	
D023A		—	18	26	30	μA	2.3	FVR current **(Note 1)**
		—	19	27	37	μA	3.0	
		—	20	29	45	μA	5.0	
D024		—	8.0	17	20	μA	3.0	BOR Current **(Note 1)**
D024		—	8.0	17	30	μA	3.0	BOR Current **(Note 1)**
		—	9.0	20	40	μA	5.0	
D024A		—	0.30	4.0	8.0	μA	3.0	LPBOR Current
D024A		—	0.30	4.0	14	μA	3.0	LPBOR Current **(Note 1)**
		—	0.45	8.0	17	μA	5.0	
D025		—	0.3	5.0	9.0	μA	1.8	SOSC Current **(Note 1)**
		—	0.5	8.5	12	μA	3.0	
D025		—	1.1	6.0	10	μA	2.3	SOSC Current **(Note 1)**
		—	1.3	8.5	20	μA	3.0	
		—	1.4	10	25	μA	5.0	
D026		—	0.10	1.0	9.0	μA	1.8	ADC Current **(Note 1, 3)**, no conversion in progress
		—	0.10	2.0	10	μA	3.0	
D026		—	0.16	3.0	10	μA	2.3	ADC Current **(Note 1, 3)**, no conversion in progress
		—	0.40	4.0	11	μA	3.0	
		—	0.50	6.0	16	μA	5.0	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral Δ current can be determined by subtracting the base IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

3: ADC clock source is FRC.

4: VREGPM = 1, PIC16F1516/7/8/9 only.

FIGURE 26-27: IDD TYPICAL, HS OSCILLATOR, PIC16LF1516/7/8/9 ONLY

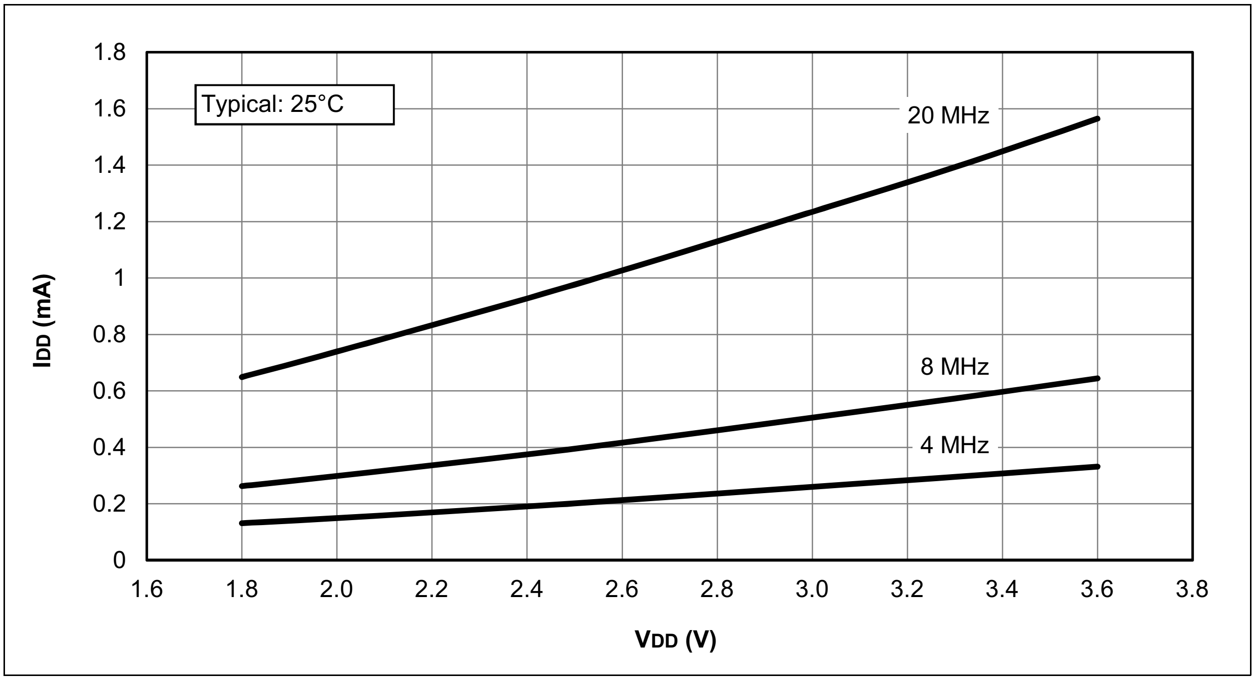


FIGURE 26-28: IDD MAXIMUM, HS OSCILLATOR, PIC16LF1516/7/8/9 ONLY

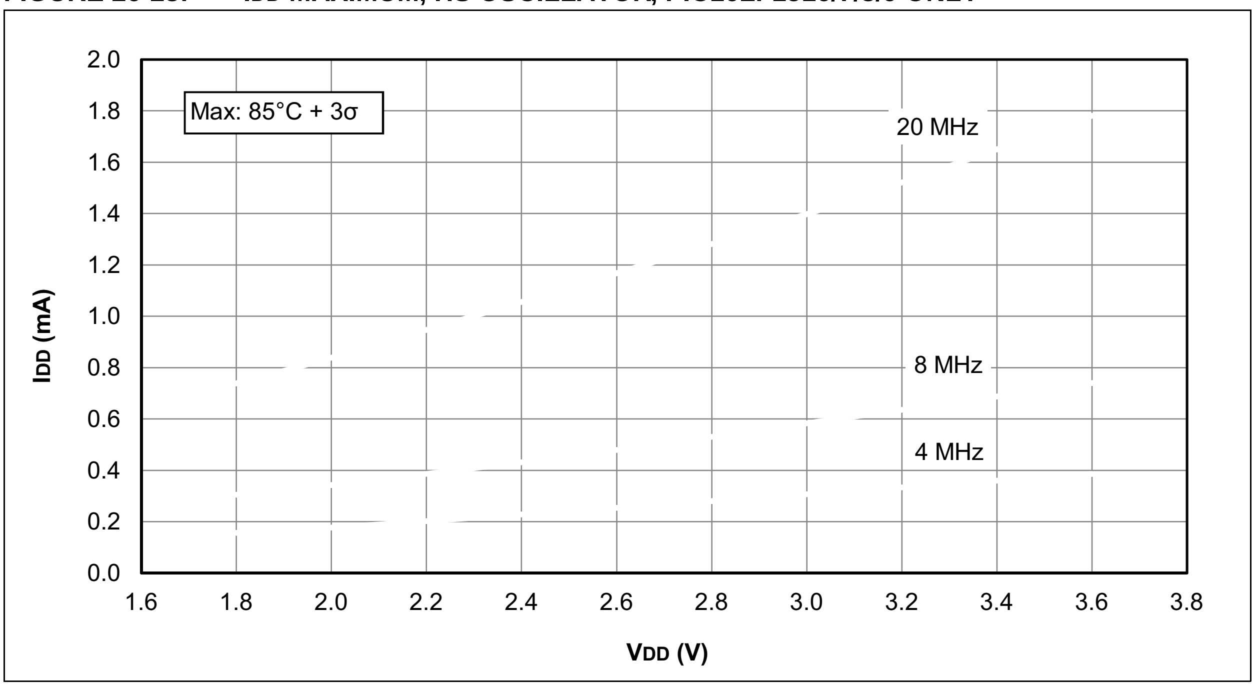


FIGURE 26-57: WDT TIME-OUT PERIOD

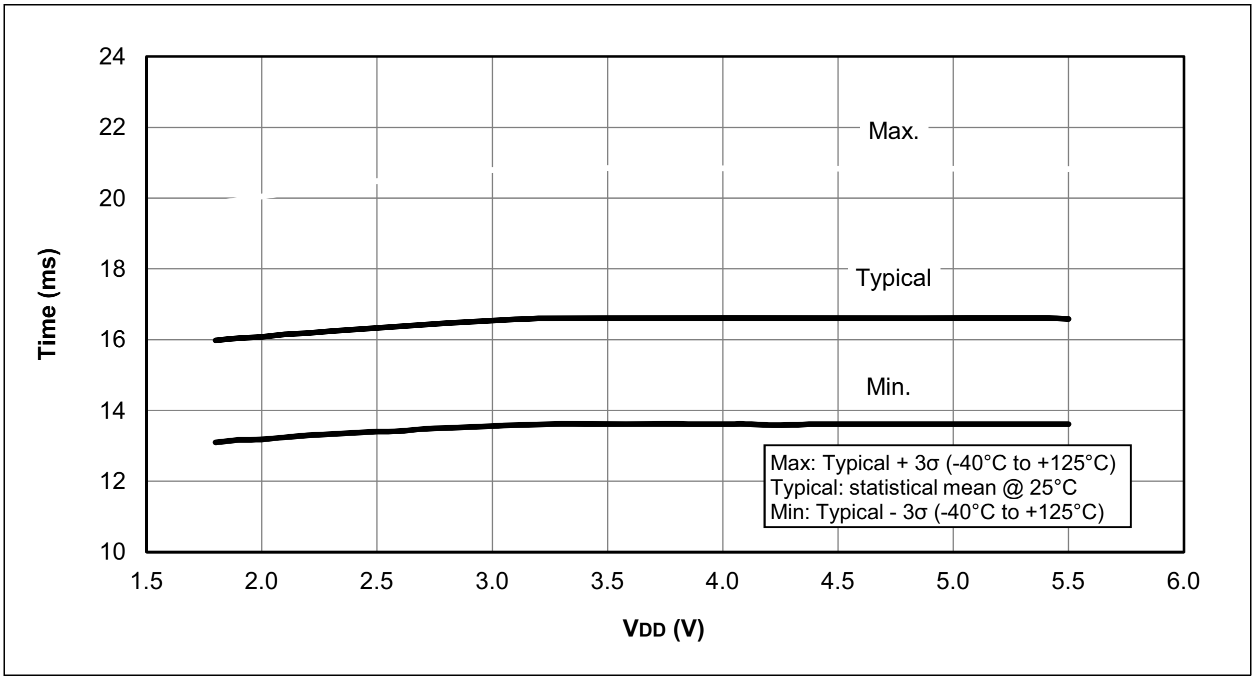
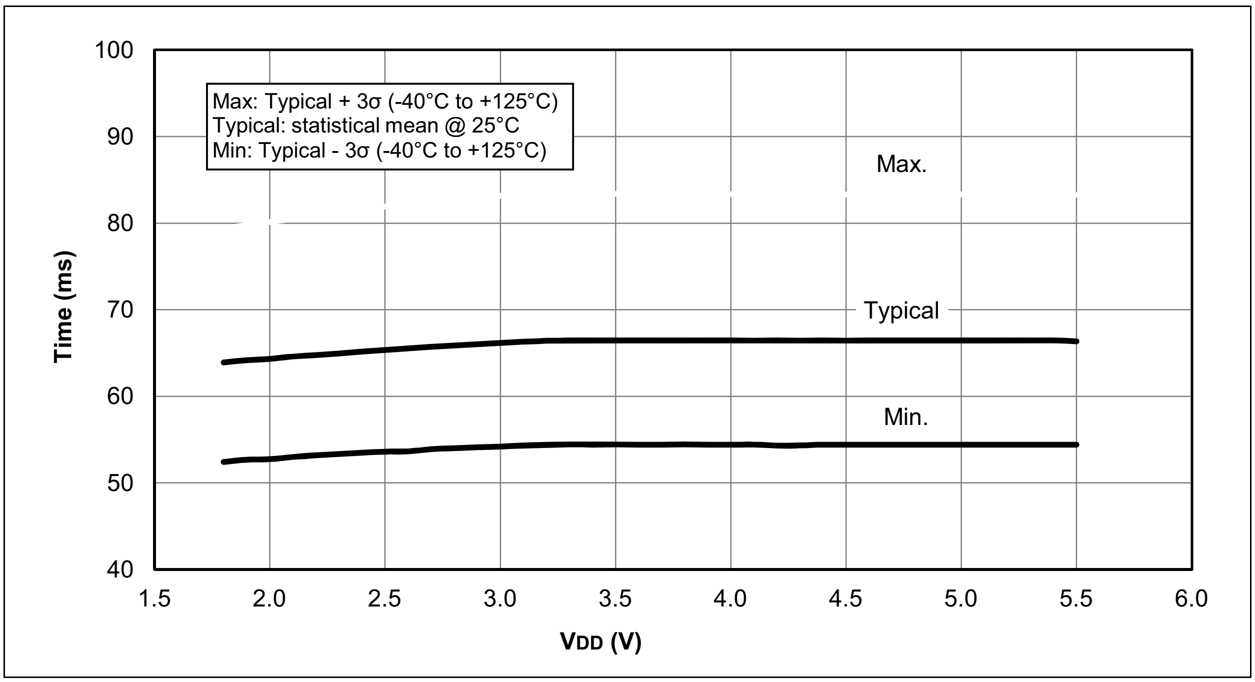
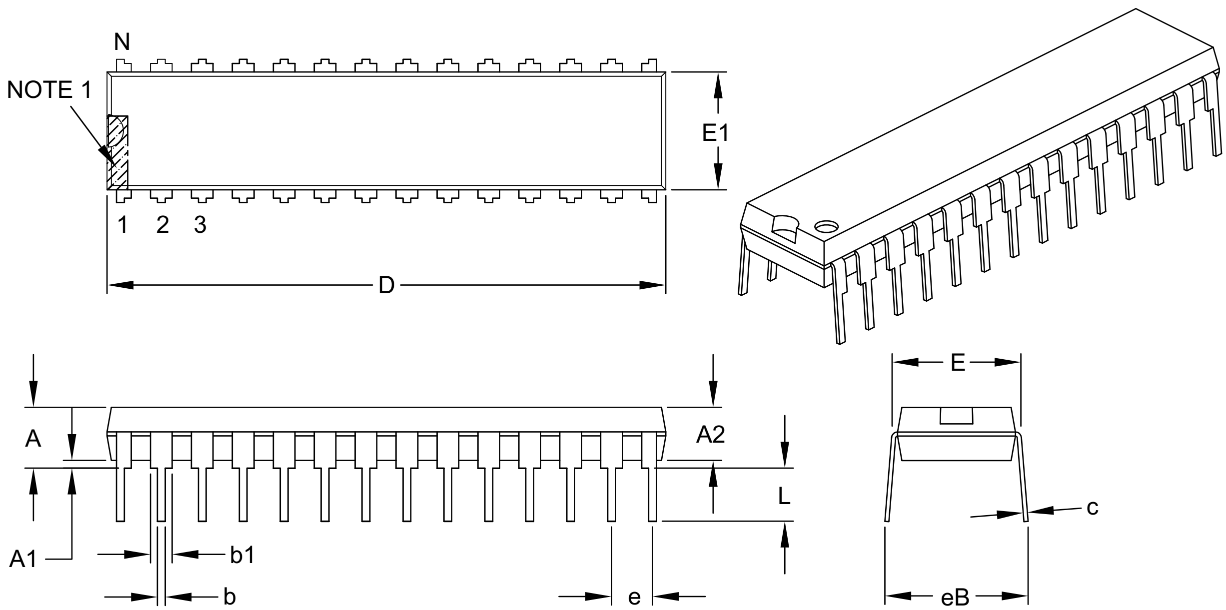


FIGURE 26-58: PWRT PERIOD



28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

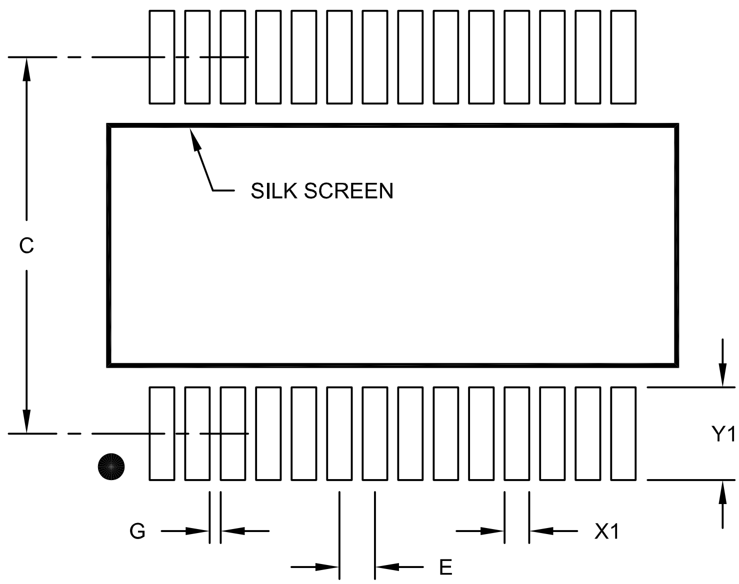
Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A