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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1518-i-mv

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### 3.4.6 SPECIAL FUNCTION REGISTERS SUMMARY

The Special Function registers are listed in Table 3-8.

#### **TABLE 3-8:** SPECIAL FUNCTION REGISTER SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Banl	k 0										
00Ch	PORTA	PORTA Dat	a Latch whe	n written: P	ORTA pins wh	nen read				xxxx xxxx	uuuu uuuu
00Dh	PORTB	PORTB Dat	ta Latch whe	en written: P	ORTB pins wl	hen read				xxxx xxxx	uuuu uuuu
00Eh	PORTC	PORTC Da	PORTC Data Latch when written: PORTC pins when read								
00Fh	PORTD	PORTD Da	ta Latch whe	en written: P	ORTD pins w	hen read				xxxx xxxx	uuuu uuuu
010h	PORTE	_	_	_	_	RE3	RE2 <sup>(3)</sup>	RE1 <sup>(3)</sup>	RE0 <sup>(3)</sup>	xxxx	uuuu
011h	PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
012h	PIR2	OSFIF	_	_	_	BCLIF	_	_	CCP2IF	00	00
013h	—	Unimpleme	nted							_	_
014h	—	Unimpleme	nted							—	_
015h	TMR0	Holding Re	gister for the	8-bit Timer	) Count					xxxx xxxx	uuuu uuuu
016h	TMR1L	Holding Re	gister for the	Least Signi	ficant Byte of	the 16-bit TN	/IR1 Count			xxxx xxxx	uuuu uuuu
017h	TMR1H	Holding Re	gister for the	Most Signif	icant Byte of	the 16-bit TM	R1 Count			xxxx xxxx	uuuu uuuu
018h	T1CON	TMR1C	:S<1:0>	T1CKF	PS<1:0>	T1OSCEN	T1SYNC	_	TMR10N	0000 00-0	uuuu uu-u
019h	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T <u>1GGO</u> / DONE	T1GVAL	T1GS	S<1:0>	0000 0x00	uuuu uxuu
01Ah	TMR2	Timer 2 Module Register 0000									0000 0000
01Bh	PR2	Timer 2 Per	iod Register							1111 1111	1111 1111
01Ch	T2CON	_		T2OUT	PS<3:0>		TMR2ON	T2CKP	S<1:0>	-000 0000	-000 0000
01Dh	_	Unimpleme	nted							_	_
01Eh	_	Unimpleme	nted							_	_
01Fh	_	Unimpleme	nted							_	_
Ban	k 1										
08Ch	TRISA	PORTA Dat	a Direction I	Register						1111 1111	1111 1111
08Dh	TRISB	PORTB Da	ta Direction	Register						1111 1111	1111 1111
08Eh	TRISC	PORTC Da	ta Direction	Register						1111 1111	1111 1111
08Fh	TRISD <sup>(2)</sup>	PORTD Da	ta Direction	Register						1111 1111	1111 1111
090h	TRISE	_		—	—	_(3)	TRISE2(2)	TRISE1(2)	TRISE0(2)	1111	1111
091h	PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
092h	PIE2	OSFIE	_	_	_	BCLIE	_	_	CCP2IE	00	0 00
093h	—	Unimpleme	nted		•					_	_
094h	_	Unimpleme	nted							_	_
095h	OPTION_REG	WPUEN	INTEDG	TMR0CS	TMR0SE	PSA		PS<2:0>		1111 1111	1111 1111
096h	PCON	STKOVF	STKUNF	_	RWDT	RMCLR	RI	POR	BOR	00-1 11qq	qq-q qquu
097h	WDTCON	_	_		v	VDTPS<4:0>			SWDTEN	01 0110	01 0110
098h	_	Unimpleme	nted							_	_
099h	OSCCON	_		IRCF	<3:0>		_	SCS	<1:0>	-011 1-00	-011 1-00
09Ah	OSCSTAT	SOSCR	_	OSTS	HFIOFR		_	LFIOFR	HFIOFS	0-q000	q-qq0q
09Bh	ADRESL	ADC Result	t Register Lo	W						xxxx xxxx	uuuu uuuu
09Ch	ADRESH	ADC Result	t Register Hi	gh						xxxx xxxx	uuuu uuuu
09Dh	ADCON0	—			CHS<4:0>			GO/DONE	ADON	-000 0000	-000 0000
09Eh	ADCON1	ADFM		ADCS<2:0>	<b>`</b>	_	_	ADPRE	F<1:0>	000000	000000
09Fh	—	Unimpleme	nted							—	—

Legend:

x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'. PIC16F1516/7/8/9 only.

Note 1:

2: 3: PIC16(L)F1517/9 only.

Unimplemented, read as '1'.

### FIGURE 5-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



- Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
  - 2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.
  - **3:** For oscillator design assistance, reference the following Microchip Applications Notes:
    - AN826, Crystal Oscillator Basics and Crystal Selection for rfPIC<sup>®</sup> and PIC<sup>®</sup> Devices (DS00826)
    - AN849, Basic PIC<sup>®</sup> Oscillator Design (DS00849)
    - AN943, Practical PIC<sup>®</sup> Oscillator Analysis and Design (DS00943)
    - AN949, Making Your Oscillator Work (DS00949)

### FIGURE 5-4:

#### CERAMIC RESONATOR OPERATION (XT OR HS MODE)



#### 5.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended, unless either FSCM or Two-Speed Start-up are enabled. In this case, code will continue to execute at the selected INTOSC frequency while the OST is counting. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-Up mode can be selected (see **Section 5.4 "Two-Speed Clock Start-up Mode"**).

#### 8.2 Low-Power Sleep Mode

The PIC16F1516/7/8/9 device contains an internal Low Dropout (LDO) voltage regulator, which allows the device I/O pins to operate at voltages up to 5.5V while the internal device logic operates at a lower voltage. The LDO and its associated reference circuitry must remain active when the device is in Sleep mode. The PIC16F1516/7/8/9 allows the user to optimize the operating current in Sleep, depending on the application requirements.

A Low-Power Sleep mode can be selected by setting the VREGPM bit of the VREGCON register. With this bit set, the LDO and reference circuitry are placed in a low-power state when the device is in Sleep.

## 8.2.1 SLEEP CURRENT VS. WAKE-UP TIME

In the default operating mode, the LDO and reference circuitry remain in the normal configuration while in Sleep. The device is able to exit Sleep mode quickly since all circuits remain active. In Low-Power Sleep mode, when waking up from Sleep, an extra delay time is required for these circuits to return to the normal configuration and stabilize.

The Low-Power Sleep mode is beneficial for applications that stay in Sleep mode for long periods of time. The normal mode is beneficial for applications that need to wake from Sleep quickly and frequently.

#### 8.2.2 PERIPHERAL USAGE IN SLEEP

Some peripherals that can operate in Sleep mode will not operate properly with the Low-Power Sleep mode selected. The LDO will remain in the normal power mode when those peripherals are enabled. The Low-Power Sleep mode is intended for use with these peripherals:

- Brown-Out Reset (BOR)
- Watchdog Timer (WDT)
- External interrupt pin/Interrupt-on-change pins
- Timer1 (with external clock source)
- CCP (Capture mode)
- Note: The PIC16LF1516/7/8/9 does not have a configurable Low-Power Sleep mode. PIC16LF1516/7/8/9 is an unregulated device and is always in the lowest power state when in Sleep, with no wake-up time penalty. This device has a lower maximum VDD and I/O voltage than the PIC16F1516/7/8/9. See Section 25.0 "Electrical Specifications" for more information.

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	
LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	
bit 7							bit 0	
Legend:								
R = Readable b	oit	W = Writable	bit	U = Unimplemented bit, read as '0'				
u = Bit is unchanged x = Bit is unknown			iown	-n/n = Value at POR and BOR/Value at all other Resets				
'1' = Bit is set		'0' = Bit is clea	ared					

#### REGISTER 12-4: LATA: PORTA DATA LATCH REGISTER

#### LATA<7:0>: PORTA Output Latch Value bits<sup>(1)</sup> bit 7-4

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is the return of actual I/O pin values.

#### REGISTER 12-5: ANSELA: PORTA ANALOG SELECT REGISTER

U-0	U-0	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	ANSA5	—	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	Unimplemented: Read as '0'
bit 5	<ul> <li>ANSA5: Analog Select between Analog or Digital Function on pins RA5, respectively</li> <li>0 = Digital I/O. Pin is assigned to port or digital special function.</li> <li>1 = Analog input. Pin is assigned as analog input<sup>(1)</sup>. Digital input buffer disabled.</li> </ul>
bit 4	Unimplemented: Read as '0'
hit 2 0	ANSA 2:05 · Appled Select between Appled or Digital Eurotian on ping BA-2:05, reaped

- ANSA<3:0>: Analog Select between Analog or Digital Function on pins RA<3:0>, respectively bit 3-0 0 = Digital I/O. Pin is assigned to port or digital special function.
  - 1 = Analog input. Pin is assigned as analog input<sup>(1)</sup>. Digital input buffer disabled.
- Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

ADC Clock	Period (TAD)	Device Frequency (Fosc)						
ADC Clock Source	ADCS<2:0>	20 MHz	16 MHz	8 MHz	4 MHz	1 MHz		
Fosc/2	000	100 ns <sup>(2)</sup>	125 ns <sup>(2)</sup>	250 ns <sup>(2)</sup>	500 ns <sup>(2)</sup>	2.0 μs		
Fosc/4	100	200 ns <sup>(2)</sup>	250 ns <sup>(2)</sup>	500 ns <sup>(2)</sup>	1.0 μs	4.0 μs		
Fosc/8	001	400 ns <sup>(2)</sup>	0.5 μs <sup>(2)</sup>	1.0 μs	2.0 μs	8.0 μs <sup>(3)</sup>		
Fosc/16	101	800 ns	1.0 μs	2.0 μs	4.0 μs	16.0 μs <b><sup>(3)</sup></b>		
Fosc/32	010	1.6 μs	2.0 μs	4.0 μs	8.0 μs <sup>(3)</sup>	32.0 μs <sup>(3)</sup>		
Fosc/64	110	3.2 μs	4.0 μs	8.0 μs <sup>(3)</sup>	16.0 μs <sup>(3)</sup>	64.0 μs <sup>(3)</sup>		
Frc	x11	1.0-6.0 μs <sup>(1,4)</sup>						

#### TABLE 16-1: ADC CLOCK PERIOD (TAD) Vs. DEVICE OPERATING FREQUENCIES

Legend: Shaded cells are outside of recommended range.

Note 1: The FRC source has a typical TAD time of 1.6  $\mu$ s for VDD.

**2:** These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

**4:** The ADC clock period (TAD) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock FOSC. However, the FRC oscillator source must be used when conversions are to be performed with the device in Sleep mode.

#### FIGURE 16-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES



### 19.5 Register Definitions: Timer2 Control

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0				
—		T2OUTPS<3:0>			TMR2ON	T2CKP	S<1:0>				
bit 7							bit (				
Legend:											
R = Readabl	e bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'					
u = Bit is unc	hanged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all	other Resets				
'1' = Bit is se	t	'0' = Bit is clea	ared								
			- 1								
bit /	Unimpleme	nted: Read as	0' <b>.</b>								
bit 6-3	T2OUTPS<	3:0>: Timer2 Ou	tput Postscale	er Select bits							
	1111 = 1:16	Postscaler									
	1110 = 1.15	1110 = 1:15 POSISCAIER									
	1101 - 1.14 1100 = 1.13	1100 = 1.14  Fusisual									
	1011 = 1:12	1011 = 1:12 Postscaler									
	1010 = 1:11	1010 = 1:11 Postscaler									
	1001 <b>= 1:10</b>	1:10 Postscaler									
	1000 <b>= 1:9  </b>	Postscaler									
	0111 <b>= 1:8</b>	Postscaler									
	0110 = 1:7	Postscaler									
	0101 = 1.6										
	0100 = 1.51										
	0011 = 1.41	Postscaler									
	0001 = 1:2	Postscaler									
	0000 = 1:1	Postscaler									
bit 2	TMR2ON: T	imer2 On bit									
	1 = Timer2	1 = Timer2 is ON									
	0 = Timer2	is OFF									
bit 1-0	T2CKPS<1:	0>: Timer2 Cloc	k Prescale Se	elect bits							
	11 = Presca	ler is 64									
	10 = Presca	ler is 16									
	01 = Presca	ler is 4									
	00 = Presca	ler is 1									

#### REGISTER 19-1: T2CON: TIMER2 CONTROL REGISTER

# PIC16(L)F1516/7/8/9

During each SPI clock cycle, a full-duplex data transmission occurs. This means that while the master device is sending out the MSb from its shift register (on its SDO pin) and the slave device is reading this bit and saving it as the LSb of its shift register, that the slave device is also sending out the MSb from its shift register (on its SDO pin) and the master device is reading this bit and saving it as the LSb of its shift register.

After eight bits have been shifted out, the master and slave have exchanged register values.

If there is more data to exchange, the shift registers are loaded with new data and the process repeats itself.

Whether the data is meaningful or not (dummy data), depends on the application software. This leads to three scenarios for data transmission:

- Master sends useful data and slave sends dummy data.
- Master sends useful data and slave sends useful data.
- Master sends dummy data and slave sends useful data.

Transmissions may involve any number of clock cycles. When there is no more data to be transmitted, the master stops sending the clock signal and it deselects the slave.

Every slave device connected to the bus that has not been selected through its slave select line must disregard the clock and transmission signals and must not transmit out any data of its own.



### FIGURE 21-4: SPI MASTER AND MULTIPLE SLAVE CONNECTION

#### 21.2.1 SPI MODE REGISTERS

The MSSP module has five registers for SPI mode operation. These are:

- MSSP STATUS register (SSPSTAT)
- MSSP Control register 1 (SSPCON1)
- MSSP Control register 3 (SSPCON3)
- MSSP Data Buffer register (SSPBUF)
- MSSP Address register (SSPADD)
- MSSP Shift register (SSPSR) (Not directly accessible)

SSPCON1 and SSPSTAT are the control and STA-TUS registers in SPI mode operation. The SSPCON1 register is readable and writable. The lower six bits of the SSPSTAT are read-only. The upper two bits of the SSPSTAT are read/write. In one SPI master mode, SSPADD can be loaded with a value used in the Baud Rate Generator. More information on the Baud Rate Generator is available in **Section 21.7 "Baud Rate Generator"**.

SSPSR is the shift register used for shifting data in and out. SSPBUF provides indirect access to the SSPSR register. SSPBUF is the buffer register to which data bytes are written, and from which data bytes are read.

In receive operations, SSPSR and SSPBUF together create a buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPBUF and the SSPIF interrupt is set.

During transmission, the SSPBUF is not buffered. A write to SSPBUF will write to both SSPBUF and SSPSR.

When one device is transmitting a logical one, or letting the line float, and a second device is transmitting a logical zero, or holding the line low, the first device can detect that the line is not a logical one. This detection, when used on the SCL line, is called clock stretching. Clock stretching gives slave devices a mechanism to control the flow of data. When this detection is used on the SDA line, it is called arbitration. Arbitration ensures that there is only one master device communicating at any single time.

#### 21.3.1 CLOCK STRETCHING

When a slave device has not completed processing data, it can delay the transfer of more data through the process of clock stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCL connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

#### 21.3.2 ARBITRATION

Each master device must monitor the bus for Start and Stop bits. If the device detects that the bus is busy, it cannot begin a new message until the bus returns to an Idle state.

However, two master devices may try to initiate a transmission on or about the same time. When this occurs, the process of arbitration begins. Each transmitter checks the level of the SDA data line and compares it to the level that it expects to find. The first transmitter to observe that the two levels do not match, loses arbitration, and must stop transmitting on the SDA line.

For example, if one transmitter holds the SDA line to a logical one (lets it float) and a second transmitter holds it to a logical zero (pulls it low), the result is that the SDA line will be low. The first transmitter then observes that the level of the line is different than expected and concludes that another transmitter is communicating.

The first transmitter to notice this difference is the one that loses arbitration and must stop driving the SDA line. If this transmitter is also a master device, it also must stop driving the SCL line. It then can monitor the lines for a Stop condition before trying to reissue its transmission. In the meantime, the other device that has not noticed any difference between the expected and actual levels on the SDA line continues with its original transmission. It can do so without any complications, because so far, the transmission appears exactly as expected with no other transmitter disturbing the message. Slave Transmit mode can also be arbitrated, when a master addresses multiple slaves, but this is less common.

If two master devices are sending a message to two different slave devices at the address stage, the master sending the lower slave address always wins arbitration. When two master devices send messages to the same slave address, and addresses can sometimes refer to multiple slaves, the arbitration process must continue into the data stage.

Arbitration usually occurs very rarely, but it is a necessary process for proper multi-master support.

#### 21.4 I<sup>2</sup>C MODE OPERATION

All MSSP I<sup>2</sup>C communication is byte oriented and shifted out MSb first. Six SFR registers and two interrupt flags interface the module with the PIC<sup>®</sup> microcontroller and user software. Two pins, SDA and SCL, are exercised by the module to communicate with other external I<sup>2</sup>C devices.

#### 21.4.1 BYTE FORMAT

All communication in  $I^2C$  is done in 9-bit segments. A byte is sent from a master to a slave or vice-versa, followed by an Acknowledge bit sent back. After the 8th falling edge of the SCL line, the device outputting data on the SDA changes that pin to an input and reads in an acknowledge value on the next clock pulse.

The clock signal, SCL, is provided by the master. Data is valid to change while the SCL signal is low, and sampled on the rising edge of the clock. Changes on the SDA line while the SCL line is high define special conditions on the bus, explained below.

#### 21.4.2 DEFINITION OF I<sup>2</sup>C TERMINOLOGY

There is language and terminology in the description of  $I^2C$  communication that have definitions specific to  $I^2C$ . That word usage is defined below and may be used in the rest of this document without explanation. This table was adapted from the Philips  $I^2C$  specification.

#### 21.4.3 SDA AND SCL PINS

Selection of any I<sup>2</sup>C mode with the SSPEN bit set, forces the SCL and SDA pins to be open-drain. These pins should be set by the user to inputs by setting the appropriate TRIS bits.

**Note:** Data is tied to output zero when an I<sup>2</sup>C mode is enabled.

#### 21.4.4 SDA HOLD TIME

The hold time of the SDA pin is selected by the SDAHT bit of the SSPCON3 register. Hold time is the time SDA is held valid after the falling edge of SCL. Setting the SDAHT bit selects a longer 300 ns minimum hold time and may help on buses with large capacitance.

Term	Description
Transmitter	The device which shifts data out onto the bus.
Receiver	The device which shifts data in from the bus.
Master	The device that initiates a transfer, generates clock signals and termi- nates a transfer.
Slave	The device addressed by the mas- ter.
Multi-master	A bus with more than one device that can initiate data transfers.
Arbitration	Procedure to ensure that only one master at a time controls the bus. Winning arbitration ensures that the message is not corrupted.
Synchronization	Procedure to synchronize the clocks of two or more devices on the bus.
Idle	No master is controlling the bus, and both SDA and SCL lines are high.
Active	Any time one or more master devices are controlling the bus.
Addressed Slave	Slave device that has received a matching address and is actively being clocked by a master.
Matching Address	Address byte that is clocked into a slave that matches the value stored in SSPADD.
Write Request	Slave receives a matching address with $R/\overline{W}$ bit clear, and is ready to clock in data.
Read Request	Master sends an address byte with the $R/\overline{W}$ bit set, indicating that it wishes to clock data out of the Slave. This data is the next and all following bytes until a Restart or Stop.
Clock Stretching	When a device on the bus hold SCL low to stall communication.
Bus Collision	Any time the SDA line is sampled low by the module while it is out- putting and expected high state.

#### TABLE 21-1: I<sup>2</sup>C BUS TERMS

#### 21.4.5 START CONDITION

The  $I^2C$  specification defines a Start condition as a transition of SDA from a high to a low state while SCL line is high. A Start condition is always generated by the master and signifies the transition of the bus from an Idle to an Active state. Figure 21-12 shows wave forms for Start and Stop conditions.

A bus collision can occur on a Start condition if the module samples the SDA line low before asserting it low. This does not conform to the  $I^2C$  Specification that states no bus collision can occur on a Start.

#### 21.4.6 STOP CONDITION

A Stop condition is a transition of the SDA line from low-to-high state while the SCL line is high.

Note:	At least one SCL low time must appear							
	before a Stop is valid, therefore, if the SDA							
	line goes low then high again while the SCL							
	line stays high, only the Start condition is							
	detected.							

#### 21.4.7 RESTART CONDITION

A Restart is valid any time that a Stop would be valid. A master can issue a Restart if it wishes to hold the bus after terminating the current transfer. A Restart has the same effect on the slave that a Start would, resetting all slave logic and preparing it to clock in an address. The master may want to address the same or another slave. Figure 21-13 shows the wave form for a Restart condition.

In 10-bit Addressing Slave mode a Restart is required for the master to clock data out of the addressed slave. Once a slave has been fully addressed, matching both high and low address bytes, the master can issue a Restart and the high address byte with the  $R/\overline{W}$  bit set. The slave logic will then hold the clock and prepare to clock out data.

After a full match with  $R/\overline{W}$  clear in 10-bit mode, a prior match flag is set and maintained. Until a Stop condition, a high address with  $R/\overline{W}$  clear, or high address match fails.

#### 21.4.8 START/STOP CONDITION INTERRUPT MASKING

The SCIE and PCIE bits of the SSPCON3 register can enable the generation of an interrupt in Slave modes that do not typically support this function. Slave modes where interrupt on Start and Stop detect are already enabled, these bits will have no effect.

#### 22.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCSTA register which resets the EUSART. Clearing the CREN bit of the RCSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note:	If all receive characters in the receive								
	FIFO have framing errors, repeated reads								
	of the RCREG will not clear the FERR bit.								

#### 22.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCSTA register or by resetting the EUSART by clearing the SPEN bit of the RCSTA register.

#### 22.1.2.6 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCSTA register is the 9th and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

#### 22.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the 9th data bit set will be transferred to the receive FIFO buffer, thereby setting the RCIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.







## TABLE 22-5:SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER<br/>TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	232
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	74
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	75
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	77
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	231
SPBRGL				BRG	<7:0>				233*
SPBRGH				BRG<	15:8>				233*
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	114
TXREG	EUSART Transmit Data Register								222*
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	230

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous master transmission.

# PIC16(L)F1516/7/8/9

CALL	Call Subroutine		
Syntax:	[ <i>label</i> ] CALL k		
Operands:	$0 \leq k \leq 2047$		
Operation:	$\begin{array}{l} (PC)+1 \rightarrow TOS, \\ k \rightarrow PC<10:0>, \\ (PCLATH<6:3>) \rightarrow PC<14:11> \end{array}$		
Status Affected:	None		
Description:	Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The 11-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a 2-cycle instruc- tion.		

CLRWDT	Clear Watchdog Timer
Syntax:	[label] CLRWDT
Operands:	None
Operation:	$00h \rightarrow WDT$ $0 \rightarrow \underline{WDT} \text{ prescaler,}$ $1 \rightarrow \underline{TO}$ $1 \rightarrow \overline{PD}$
Status Affected:	TO, PD
Description:	CLRWDT instruction resets the Watch- dog Timer. It also resets the prescaler of the WDT Status bits TO and PD are set.

CALLW	Subroutine Call With W	COMF	Complement f	
Syntax:	[ label ] CALLW	Syntax:	[ <i>label</i> ] COMF f,d	
Operands:	None	Operands:	$0 \le f \le 127$	
Operation:	(PC) +1 $\rightarrow$ TOS, (W) $\rightarrow$ PC<7:0>, (PCLATH<6:0>) $\rightarrow$ PC<14:8>	Operation: Status Affected:	$\vec{(f)} \rightarrow (destination)$	
Status Affected:	None	Description:	The contents of register 'f' are com- plemented. If 'd' is '0', the result is	
Description:	Subroutine call with W. First, the return address (PC + 1) is pushed onto the return stack. Then, the contents of W is loaded into PC<7:0>, and the contents of PCLATH into PC<14:8>. CALLW is a 2-cycle instruction.		stored in W. If 'd' is '1', the result is stored back in register 'f'.	

CLRF	Clear f	
Syntax:	[label] CLRF f	
Operands:	$0 \leq f \leq 127$	
Operation:	$\begin{array}{l} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$	
Status Affected:	Z	
Description:	The contents of register 'f' are cleared and the Z bit is set.	

DECF	Decrement f
Syntax:	[label] DECF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d  \in  [0,1] \end{array}$
Operation:	(f) - 1 $\rightarrow$ (destination)
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

CLRW	Clear W
Syntax:	[label] CLRW
Operands:	None
Operation:	$\begin{array}{l} \text{00h} \rightarrow (\text{W}) \\ 1 \rightarrow \text{Z} \end{array}$
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

### 25.0 ELECTRICAL SPECIFICATIONS

### 25.1 Absolute Maximum Ratings<sup>(†)</sup>

Ambient temperature under bias	40°C to +125°C		
Storage temperature	65°C to +150°C		
Voltage on VDD with respect to Vss, PIC16F1516/7/8/9	0.3V to +6.5V		
Voltage on VDD with respect to Vss, PIC16LF1516/7/8/9	0.3V to +4.0V		
Voltage on MCLR with respect to Vss	0.3V to +9.0V		
Voltage on all other pins with respect to Vss	0.3V to (VDD + 0.3V)		
Total power dissipation <sup>(2)</sup>			
Maximum current			
on Vss pin for 28-Pin devices <sup>(1)</sup>			
-40°C $\leq$ TA $\leq$ +85°C			
on VDD pin for 28-Pin devices <sup>(1)</sup>			
-40°C $\leq$ Ta $\leq$ +85°C	250 mA 85 mA		
on Vss pin for 40/44-Pin devices <sup>(1)</sup>			
-40°C $\leq$ Ta $\leq$ +85°C	350 mA 120 mA		
on VDD pin for 40/44-Pin devices <sup>(1)</sup>			
-40°C $\leq$ Ta $\leq$ +85°C	350 mA 120 mA		
Clamp current, Ik (VPIN < 0 or VPIN > VDD)	± 20 mA		
Maximum output current sunk by any I/O pin	50 mA		
Maximum output current sourced by any I/O pin			

**Note 1:** Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Table 25-5 to calculate device specifications.

2: Power dissipation is calculated as follows: PDIS = VDD x {IDD  $-\sum$  IOH} +  $\sum$  {(VDD - VOH) x IOH} +  $\sum$ (VOI x IOL)

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

#### FIGURE 25-15: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



#### TABLE 25-11: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$						
Param. No.         Symbol         Characteristic         Min.         Max.         Units         Conditions						Conditions
US125	TDTV2CKL	SYNC RCV (Master and Slave) Data-hold before CK $\downarrow$ (DT hold time)	10		ns	
US126	TCKL2DTL	Data-hold after CK $\downarrow$ (DT hold time)	15		ns	

# PIC16(L)F1516/7/8/9







FIGURE 26-6: IDD MAXIMUM, XT AND EXTRC OSCILLATOR, PIC16F1516/7/8/9 ONLY

# PIC16(L)F1516/7/8/9





FIGURE 26-10: IDD, EC OSCILLATOR, LOW-POWER MODE, FOSC = 500 kHz, PIC16F1516/7/8/9 ONLY





### Package Marking Information (Continued)

Leger	nd: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the eve be carrie characters	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available s for customer-specific information.

28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-152A Sheet 1 of 2

#### 40-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) - 5x5 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension Limits		MIN	NOM	MAX	
Contact Pitch	E	0.40 BSC			
Optional Center Pad Width	W2			3.80	
Optional Center Pad Length	T2			3.80	
Contact Pad Spacing	C1		5.00		
Contact Pad Spacing	C2		5.00		
Contact Pad Width (X40)	X1			0.20	
Contact Pad Length (X40)	Y1			0.75	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2156B

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