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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	95
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	121-VFBGA, CSBGA
Supplier Device Package	121-CSPBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65p04f-tcb121i

Overview

The SiliconBlue Technologies iCE65P P-Series programmable logic family is specifically designed to deliver the lowest static and dynamic power consumption of any comparable CPLD or FPGA device. iCE65P FPGAs are designed specifically for cost-sensitive, high-volume applications. iCE65P FPGA are fully user-programmable and can self-configure from a configuration image stored in on-chip, nonvolatile configuration memory (NVCM) or stored in an external commodity SPI serial Flash PROM or downloaded from an external processor over an SPI-like serial port.

The three iCE65P components, highlighted in Table 1, deliver from approximately 3,500 to 12,000 logic cells and flip-flops while consuming a fraction of the power of comparable programmable logic devices. Each iCE65P device includes between 20 or more RAM blocks, each with 4Kbits of storage, for on-chip data storage and data buffering.

As pictured in Figure 1, each iCE65P device consists of five primary architectural elements.

- An array of Programmable Logic Blocks (PLBs)
  - Each PLB contains eight Logic Cells (LCs); each Logic Cell consists of …
    - A fast, four-input look-up table (LUT4) capable of implementing any combinational logic function of up to four inputs, regardless of complexity
    - A 'D'-type flip-flop with an optional clock-enable and set/reset control
    - Fast carry logic to accelerate arithmetic functions such as adders, subtracters, comparators, and counters.
  - Common clock input with polarity control, clock-enable input, and optional set/reset control input to the PLB is shared among all eight Logic Cells
- Two-port, 4Kbit RAM blocks (RAM4K)
  - 256x16 default configuration; selectable data width using programmable logic resources
  - Simultaneous read and write access; ideal for FIFO memory and data buffering applications
  - RAM contents pre-loadable during configuration
- Four I/O banks with independent supply voltage, each with multiple Programmable Input/Output (PIO) blocks
  - LVCMOS I/O standards and LVDS outputs supported in all banks
  - I/O Bank 3 supports additional SSTL, MDDR, LVDS, and SubLVDS I/O standards
- One or more Phase-Locked Loops (PLL)
  - Very low power
  - Clock multiplication and division
  - Phase shifting in fixed 90° increments
  - Static or dynamic phase shifting
- Programmable interconnections between the blocks
  - Flexible connections between all programmable logic functions
  - Eight dedicated low-skew, high-fanout clock distribution networks

Packaging Options

iCE65P components are available in a variety of package options to support specific application requirements. The available options, including the number of available user-programmable I/O pins (PIOs), are listed in Table 2. Fully-tested Known-Good Die (KGD) DiePlus™ are available for die stacking and highly space-conscious applications. All iCE65P devices are provided exclusively in Pb-free, RoHS-compliant packages.

Table 2: **iCE65P Family Packaging Options, Maximum I/O per Package**

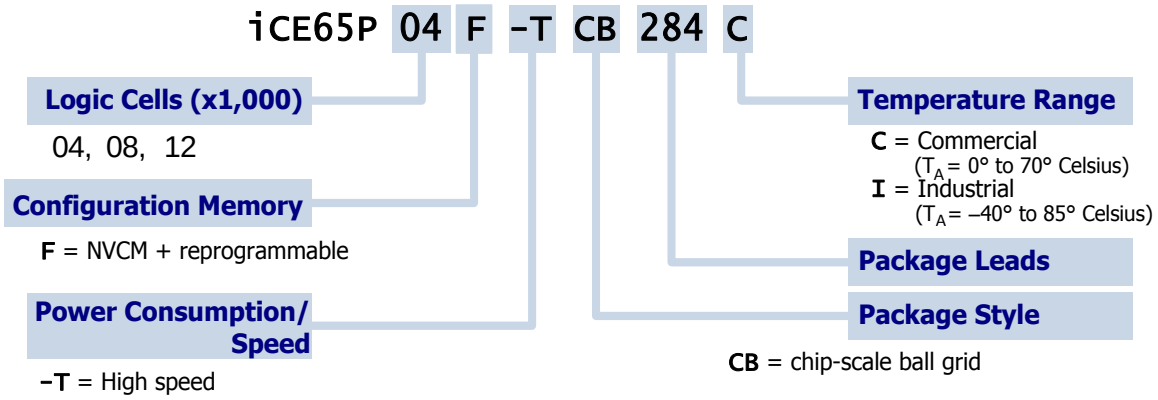
Package	Board Area (mm)	Package Code	Ball/Lead Pitch (mm)	iCE65P04	iCE65P08	iCE65P12
121-ball chip-scale BGA	6 x 6	CB121	0.5	95 *(13)*		
196-ball chip-scale BGA	8 x 8	CB196		148 *(18)*		
284-ball chip-scale BGA	12 x 12	CB284		174 *(20)*		
DiePlus known good die	See die data sheet	DI	—	174 *(20)*		

Feature-rich versions of the end application mount a larger iCE65P device on the circuit board. Low-end versions mount a smaller iCE65P device.

Ordering Information

Figure 2 describes the iCE65P ordering codes for all packaged components. See the separate DiePlus data sheets when ordering die-based products.

Figure 2: **iCE65P Ordering Codes (packaged, non-die components)**



iCE65P devices come standard in the higher speed "**-T**" version.

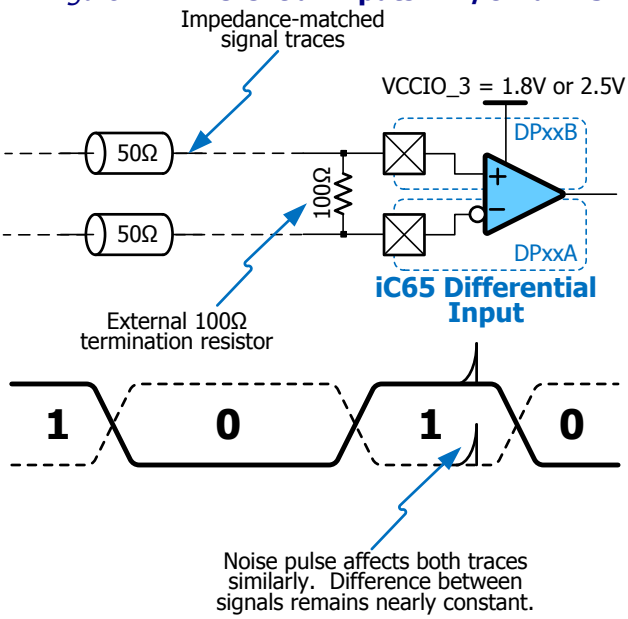
iCE65P devices are available in two operating temperature ranges, one for typical commercial applications, the other with an extended temperature range for industrial and telecommunications applications. The ordering code also specifies the device package option, as described further in Table 2.

Programmable Logic Block (PLB)

Generally, a logic design for an iCE65P component is created using a high-level hardware description language such as Verilog or VHDL. The SiliconBlue Technologies development software then synthesizes the high-level description into equivalent functions built using the programmable logic resources within each iCE65P device. Both sequential and combinational functions are constructed from an array of Programmable Logic Blocks (PLBs). Each PLB contains eight Logic Cells (LCs), as pictured in Figure 3, and share common control inputs, such as clocks, reset, and enable controls.

PLBs are connected to one another and other logic functions using the rich Programmable Interconnect resources.

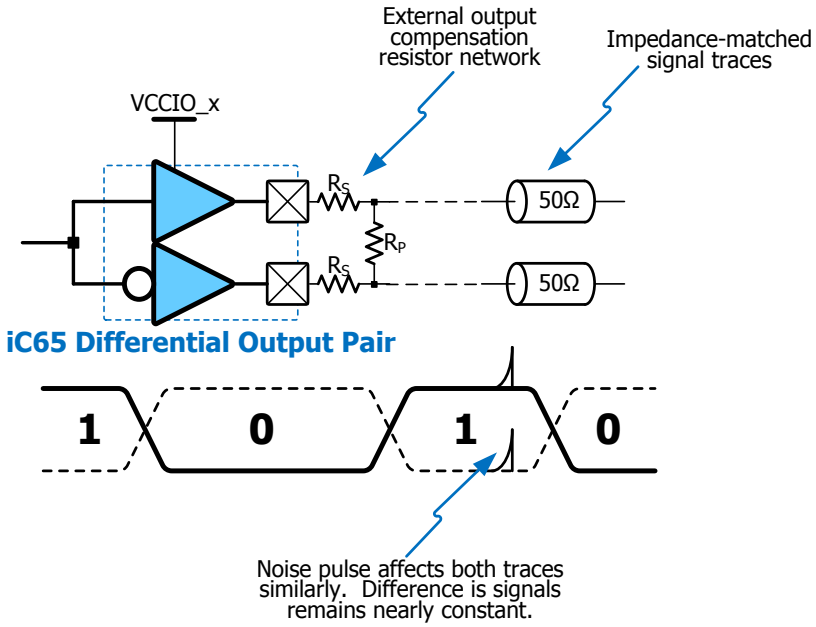
Figure 7: **Differential Inputs in I/O Bank 3**



Differential Outputs in Any Bank

Differential outputs are built using a pair of single-ended PIO pins as shown in Figure 8. Each differential I/O pair requires a three-resistor termination network to adjust output characteristic to match those for the specific differential I/O standard. The output characteristics depend on the values of the parallel resistors (RP) and series resistor (RS). Differential outputs must be located in the same I/O tile.

Figure 8: **Differential Output Pair**



For electrical characteristics, see "Differential Outputs" on page 75.

The PIO pins that make up a differential output pair are indicated with a blue bounding box in the in the tables in "Die Cross Reference" starting on page 67.

Input Signal Path

As shown in Figure 6, a signal from a package pin optionally feeds directly into the device, or is held in an input register. The input signal connects to the programmable interconnect resources through the IN signal. Table 9 describes the input behavior, assuming that the output path is not used or if a bidirectional I/O, that the output driver is in its high-impedance state (Hi-Z). Table 9 also indicates the effect of the Power-Saving I/O Bank iCEgate Latch and the Input Pull-Up Resistors on I/O Banks 0, 1, and 2.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Power-Saving I/O Bank iCEgate Latch

To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control. As shown in Figure 9, the iCEgate HOLD control signal captures the external value from the associated asynchronous input. The HOLD signal prevents switching activity on the PIO pad from affecting internal logic or programmable interconnect. Minimum power consumption occurs when there is no switching. However, individual pins within the I/O bank can bypass the iCEgate latch and directly feed into the programmable interconnect, remaining active during low-power operation. This behavior is described in Table 9. The decision on which asynchronous inputs use the iCEgate feature and which inputs bypass it is determined during system design. In other words, the iCEgate function is part of the source design used to create the iCE65P configuration image.

Figure 9: **Power-Saving iCEgate Latch**

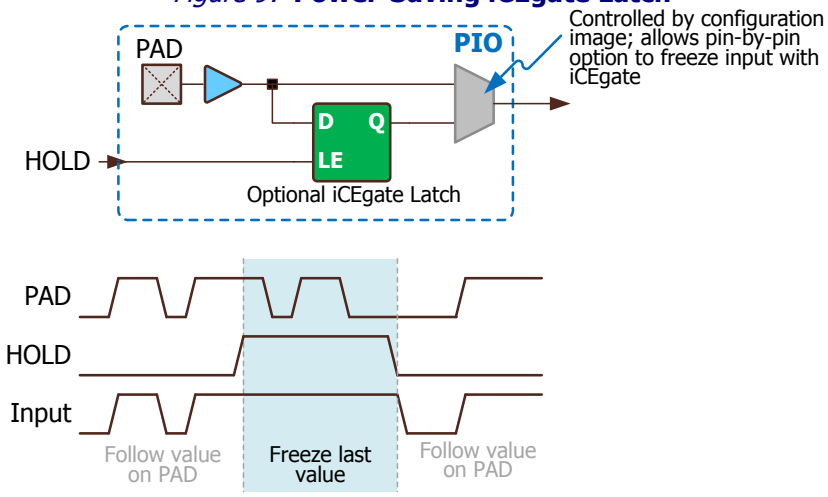


Table 9: **PIO Non-Registered Input Operations**

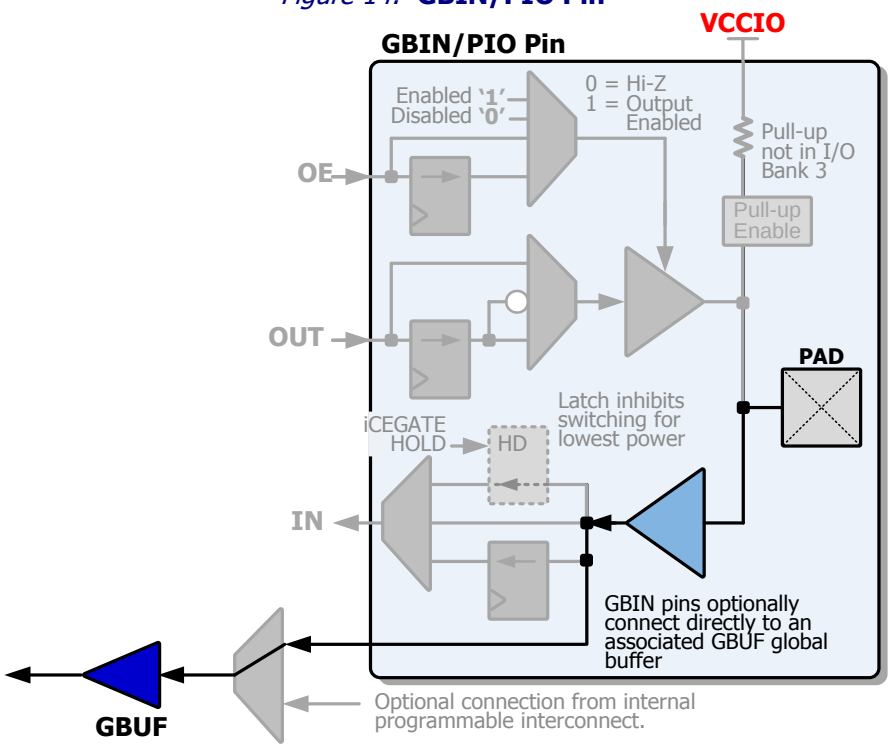
Operation	HOLD	Bitstream Setting		PAD	IN
	iCEgate Latch	Controlled by iCEgate?	Input Pull-Up Enabled?	Pin Value	Input Value to Interconnect
Data Input	0	X	X	PAD	PAD Value
Pad Floating, No Pull-up	0	X	No	Z	(Undefined)
Pad Floating, Pull-up	0	X	Yes	Z	1
Data Input, Latch Bypassed	X	No	X	PAD	PAD Value
Pad Floating, No Pull-up, Latch Bypassed	X	No	No	Z	(Undefined)
Pad Floating, Pull-up, Latch Bypassed	X	No	Yes	Z	1
Low Power Mode, Hold Last Value	1	Yes	X	X	Last Captured PAD Value

There are four iCEgate HOLD controls, one per each I/O bank. The iCEgate HOLD control input originates within the interconnect fabric, near the middle of the I/O edge. Consequently, the HOLD signal is optionally controlled externally through a PIO pin or from other logic within the iCE65P device.

Table 14: **Global Buffer Input Ball Number by Package**

Global Buffer Input (GBIN)	I/O Bank	Package Code		
		`P04 CB121	**`P04 CB196**	**`P04 CB284**
GBIN0	0	D6	A7	E10
GBIN1		C6	E7	E11
GBIN2	1	F9	F10	L18
GBIN3		F8	G12	K18
GBIN4	2	L9	L7	V12
GBIN5		L8	P5	V11
GBIN6	3	F4	H1	M5
GBIN7		D3	G1	L5

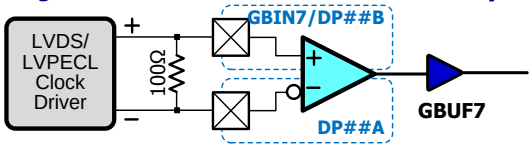
Figure 14: **GBIN/PIO Pin**



Differential Global Buffer Input

All eight global buffer inputs support single-ended I/O standards such as LVCMOS. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct SubLVDS, LVDS, or LVPECL differential clock input, as shown in Figure 15. The GBIN7 and its associated differential I/O pad accept a differential clock signal. A 100 Ω termination resistor is required across the two pads. Optionally, swap the outputs from the LVDS or LVPECL clock driver to invert the clock as it enters the iCE65P device.

Figure 15: **LVDS or LVPECL Clock Input**



Voltage Controlled Oscillator Supply Inputs

The phase-locked loop (PLL) uses separate analog supply inputs for the voltage-controlled oscillator (VCO).

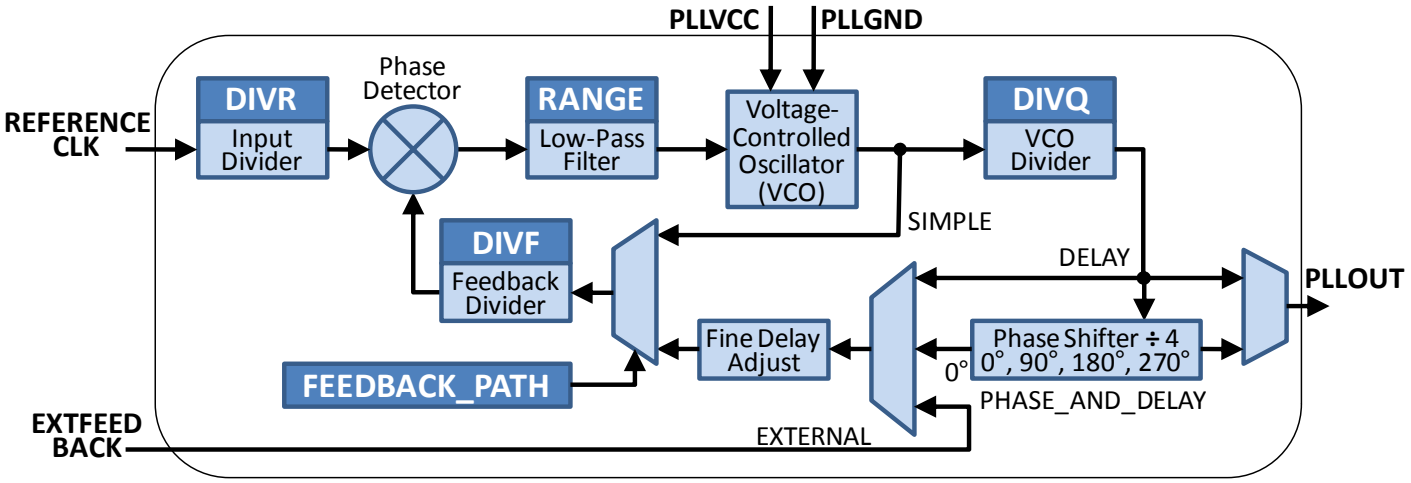
Table 19: **PLL Supply Ball Numbers by Package**

ColdBoot Select	Package Code		
	CB121	**CB196**	**CB284**
PLLGND	L6	M6	Y9
PLLVCC	L7	N6	Y10

Clock Multiplication and Division

The PLL optionally multiplies and/or divides the input reference clock to generate a PLLOUT output clock of another frequency. The output frequency depends on the frequency of the REFERENCLK input clock and the settings for the DIVR, DIVF, DIVQ, RANGE, and FEEDBACK_PATH attribute settings, as indicated in Figure 17.

Figure 17: **PLL Frequency Synthesis**



The PLL's phase detector and Voltage Controlled Oscillator (VCO) synthesize a new output clock frequency based on the attribute settings. The VCO is an analog circuit and has independent voltage supply and ground connections labeled PLLVCC and PLLGND.

The simplest method to determine the optimal settings for a specific application is to use the Frequency Synthesis Spreadsheet

PLLOUT Frequency for All Modes Except FEEDBACK_PATH = SIMPLE

For all the FEEDBACK_PATH modes, except SIMPLE, the PLLOUT frequency is the result of Equation 2.

$$F_{PLLOUT} = \frac{F_{REFERNCECLK} \bullet (DIVF + 1)}{DIVR + 1} \qquad \text{[Equation 2]}$$

PLLOUT Frequency for FEEDBACK_PATH = SIMPLE

If the SIMPLE feedback mode, the PLL feedback signal taps directly from the output of the VCO, before the final divider stage. Consequently, the PLL output frequency has an additions divider step, DIVQ, contributed by the final divider step as shown in Equation 3. (DIVF, DIVQ and DIVR are binary)

$$F_{PLLOUT} = \frac{F_{REFERNCECLK} \bullet (DIVF + 1)}{2^{(DIVQ)} \bullet (DIVR + 1)} \qquad \text{[Equation 3]}$$

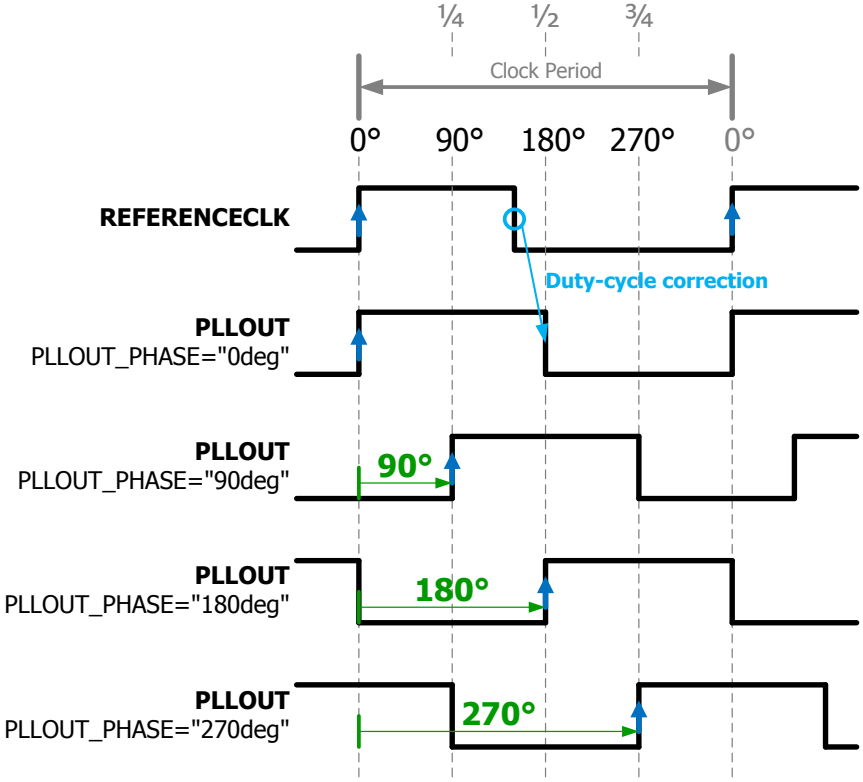
Fixed Quadrant Phase Shift

The PLL optional phase feature shifts the PLLOUT output by a specified quadrant or quarter clock cycle as shown in Figure 18 and Table 20. The quadrant phase shift option is only available when the FEEDBACK_PATH attribute is set to PHASE_AND_DELAY.

Table 20: **PLL Phase Shift Options**

PLLOUT_PHASE	Duty Cycle Correction	Phase Shift (Degrees)	Fraction Clock Cycle
NONE	No	0°	None
0deg	Yes	0°	None
90deg	Yes	90°	Quarter Cycle
180deg	Yes	180°	Half Cycle
270deg	Yes	270°	Three-quarter Cycle

Figure 18: **Fixed Quadrant Phase Shift Control (PLLOUT_PHASE)**



Unlike the Fine Delay Adjustment, the quadrant phase shifter always shifts by a fixed phase angle. The resulting phase shift, measured in delay, depends on the clock period and the PLLOUT_PHASE phase shift setting, as shown in Equation 4.

$$Delay = \frac{Phase\_Shift}{360^{\circ}} \bullet Clock\_Period \qquad \text{[Equation 4]}$$

Fine Delay Adjustment

As shown in Figure 19, the PLL provides an optional fine delay adjustment that controls the delay of the PLLOUT output relative to the input reference clock, to an external feedback signal, or relative to the selected quadrant phase shifted clock. The delay is adjusted by selecting one or more of the 16 delay taps. Each tap is approximately 165 ps.

The fine delay adjustment option is available when the FEEDBACK_PATH attribute is set to DELAY, PHASE_AND_DELAY, or EXTERNAL, as shown in Figure 19 and Figure 17.

RAM

Each iCE65P device includes multiple high-speed synchronous RAM blocks (RAM4K), each 4Kbit in size. As shown in Table 23 a single iCE65P integrates between 16 to 96 such blocks. Each RAM4K block is generically a 256-word deep by 16-bit wide, two-port register file, as illustrated in Figure 20. The input and output connections, to and from a RAM4K block, feed into the programmable interconnect resources.

Figure 20: **RAM4K Memory Block**

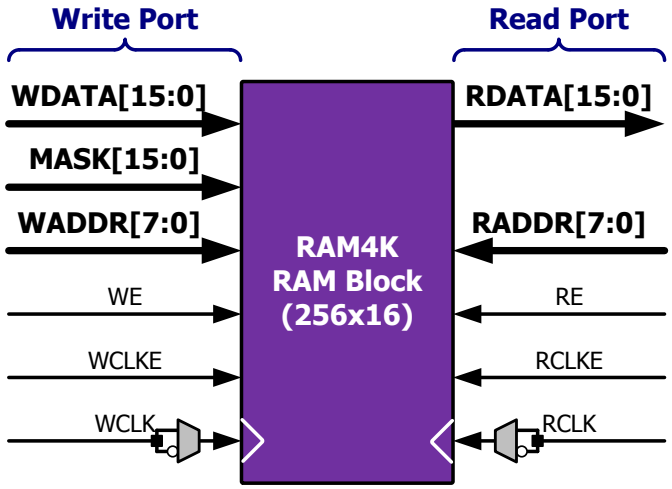


Table 23: **RAM4K Blocks per Device**

Device	RAM4K Blocks	Default Configuration	RAM Bits per Block	Block RAM Bits
iCE65P04	20	256 x 16	4K (4,096)	80K

Using programmable logic resources, a RAM4K block implements a variety of logic functions, each with configurable input and output data width.

- Random-access memory (RAM)
  - Single-port RAM with a common address, enable, and clock control lines
  - Two-port RAM with separate read and write control lines, address inputs, and enable
- Register file and scratchpad RAM
- First-In, First-Out (FIFO) memory for data buffering applications
- Circuit buffer
- A 256-deep by 16-wide ROM with registered outputs, contents loaded during configuration
  - Sixteen different 8-input look-up tables
  - Function or waveform tables such as sine, cosine, etc.
  - Correlators or pattern matching operations
- Counters, sequencers

As pictured in Figure 20, a RAM4K block has separate write and read ports, each with independent control signals. Table 24 lists the signals for both ports. Additionally, the write port has an active-Low bit-line write-enable control; optionally mask write operations on individual bits. By default, input and output data is 16 bits wide, although the data width is configurable using programmable logic and, if needed, multiple RAM4K blocks.

The WCLK and RCLK inputs optionally connect to one of the following clock sources.

- The output from any one of the eight Global Buffers, or
- A connection from the general-purpose interconnect fabric

When self-loading from NVCM or from an SPI Flash PROM, the FPGA supports an additional configuration option called Cold Boot mode. When this option is enabled in the configuration bitstream, the iCE65P FPGA boots normally from power-on or a master reset (CRESET_B = Low pulse), but monitors the value on two PIO pins that are borrowed during configuration, as shown in Figure 30. These pins, labeled PIO2/CBSEL0 and PIO2/CBSEL1, tell the FPGA which of the four possible SPI configurations to load into the device. Table 35 provides the pin or ball locations for these pins.

- Load from initial location, either from NVCM or from address 0 in SPI Flash PROM. For Cold Boot or Warm Boot applications, the initial configuration image contains the cold boot/warm boot applet.
- Check if Cold Boot configuration feature is enabled in the bitstream.
  - If not enabled, FPGA configures normally.
  - If Cold Boot is enabled, then the FPGA reads the logic values on pins CBSEL[1:0]. The FPGA uses the value as a vector and then reads from the indicated vector address.
  - At the selected CBSEL[1:0] vector address, there is a starting address for the selected configuration image.
    - For SPI Flash PROMs, the new address is a 24-bit start address in Flash.
    - If the selected bitstream is in NVCM, then the address points to the internal NVCM.
- Using the new start address, the FPGA restarts reading configuration memory from the new location.

Table 35: **ColdBoot Select Ball Numbers by Package**

ColdBoot Select	Package Code		
	CB121	**CB196**	**CB284**
PIO2/CBSEL0	H6	L9	R13
PIO2/CBSEL1	J6	P10	V14

When creating the initial configuration image, the SiliconBlue development software loads the start address for up to four configuration images in the bitstream. The value on the CBSEL[1:0] pins tell the configuration controller to read a specific start address, then to load the configuration image stored at the selected address. The multiple bitstreams are stored either in the SPI Flash or in the internal NVCM.

After configuration, the CBSEL[1:0] pins become normal PIO pins available to the application.

The Cold Boot feature allows the iCE65P to be reprogrammed for special application requirements such as the following.

- A normal operating mode and a self-test or diagnostics mode.
- Different applications based on switch settings.
- Different applications based on a card-slot ID number.

Warm Boot Configuration Option

The Warm Boot configuration is similar to the Cold Boot feature, but is completely under the control of the FPGA application.

A special design primitive, SB_WARMBOOT, allows an FPGA application to choose between four configuration images using two internal signal ports, S1 and S0, as shown in Figure 30. These internal signal ports connect to programmable interconnect, which in turn can connect to PLB logic and/or PIO pins.

After selecting the desired configuration image, the application then asserts the internal signal BOOT port High to force the FPGA to restart the configuration process from the specified vector address stored in PROM.

Time-Out and Retry

When configuring from external SPI Flash, the iCE65P device looks for a synchronization word. If the device does not find a synchronization word within its timeout period, the device automatically attempts to restart the configuration process from the very beginning. This feature is designed to address any potential power-sequencing issues that may occur between the iCE65P device and the external PROM.

Supported JTAG Commands

The JTAG interface supports the IEEE 1149.1 mandatory instructions, including EXTEST, SAMPLE/PRELOAD, and BYPASS.

Package and Pinout Information

Maximum User I/O Pins by Package and by I/O Bank

Table 41 lists the maximum number of user-programmable I/O pins by package, with additional detail showing user I/O pins by I/O bank. In some cases, a smaller iCE65P device is packaged in a larger package with unconnected (N.C.) pins or balls, resulting in fewer overall I/O pins. See Table 2 and Table 42 for device-specific I/O counts by package.

Table 41: **User I/O by Package, by I/O Bank**

	Package Code		
	CB121	**CB196**	**CB284**
Package Leads	121	196	284
Package Area (mm)	6 x 6	8 x 8	12 x 12
Ball Array (balls)	11 x 11	14 x 14	22 x 22
Ball/Lead Pitch (mm)	0.5	0.5	0.5
Maximum user I/O, all I/O banks	**95**	**148**	**220**
PIO Pins in Bank 0	25	37	60
PIO Pins in Bank 1	21	38	55
PIO Pins in Bank 2	23	33	51
PIO Pins in Bank 3	26	36	50
PIO Pins in SPI Interface	4	4	4

Maximum User I/O by Device and Package

Table 42 lists the maximum available user I/O by device and by and package type. Not all devices are available in all packages. Similarly, smaller iCE65P devices may have unconnected balls in some packages. Devices sharing a common package have similar footprints.

Table 42: **Maximum User I/O by Device and Package**

Package	Device
	iCE65P04
CB121	95
CB196	148
CB284	174

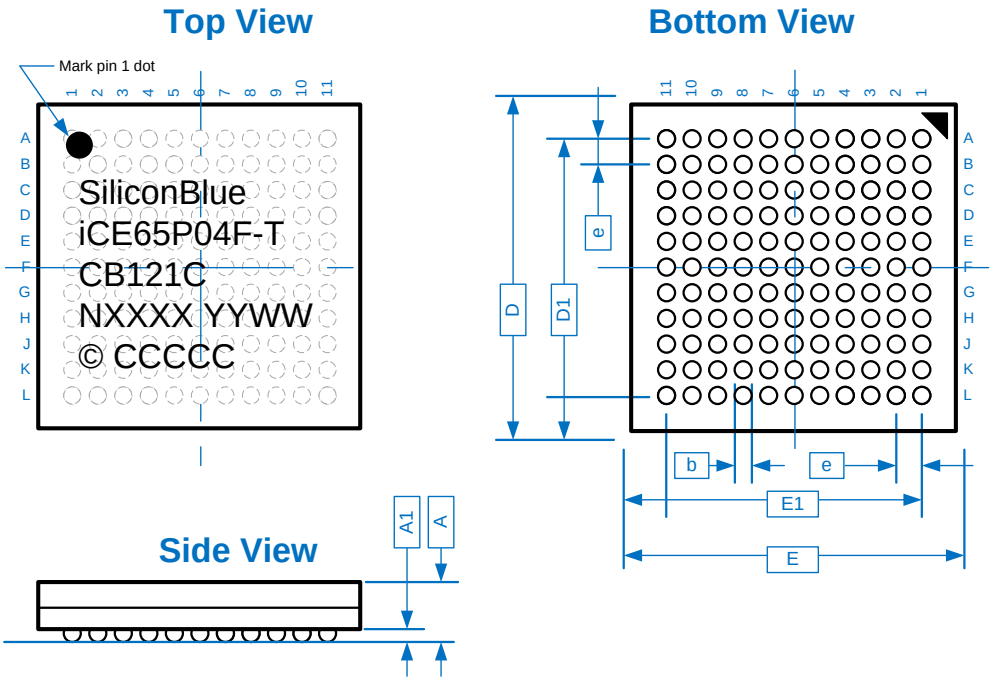
Signal Name	Direction	I/O Bank	Pull-up during Config	Description
PLLVCC	Supply	PLL	N/A	Analog voltage supply for Phase Lock Loop (PLL). If unused, tie to ground.
TDI	Input	1	No	JTAG Test Data Input. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TMS	Input	1	No	JTAG Test Mode Select. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TCK	Input	1	No	JTAG Test Clock. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TDO	Output	1	No	JTAG Test Data Output.
TRST_B	Input	1	No	JTAG Test Reset, active Low. Keep Low during normal operation; High for JTAG operation.
VCC	Supply	All	N/A	Internal core voltage supply. All must be connected.
VCCIO_0	Supply	0	N/A	Voltage supply to I/O Bank 0. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
VCCIO_1	Supply	1	N/A	Voltage supply to I/O Bank 1. All such pins or balls on the package must be connected. Required to guarantee a valid input voltage on TRST_B JTAG pin.
VCCIO_2	Supply	2	N/A	Voltage supply to I/O Bank 2. All such pins or balls on the package must be connected. Required input to the Power-On Reset (POR) circuit.
VCCIO_3	Supply	3	N/A	Voltage supply to I/O Bank 3. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
SPI_VCC	Supply	SPI	N/A	SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM. Required input to the Power-On Reset (POR) circuit.
VPP_FAST	Supply	All	N/A	Direct programming voltage supply. If unused, leave floating or unconnected during normal operation.
VPP_2V5	Supply	All	N/A	Programming supply voltage. When the iCE65P device is active, VPP_2V5 must be in the valid range between 2.3 V to 3.47 V to release the Power-On Reset circuit, even if the application is not using the NVCM.
VREF	Voltage Reference	3	N/A	Input reference voltage in I/O Bank 3 for the SSTL I/O standard. This pin only appears on the CB284 package and for die-based products.

N/A = Not Applicable

Package Mechanical Drawing

Figure 36: **CB121 Package Mechanical Drawing**

CB121: 6 x 6 mm, 121-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			11		Columns
Number of Ball Rows	Y			11		Rows
Number of Signal Balls		n		121		Balls
Body Size	X	E	5.90	6.00	6.10	mm
	Y	D	5.90	6.00	6.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.2	—	0.3	
Edge Ball Center to Center	X	E1	—	5.00	—	
	Y	D1	—	5.00	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.12	—	0.20	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65P04F	Part number
	-T	Power/Speed
3	CB121C	Package type
	ENG	Engineering
4	NXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
54	45

CB196 Chip-Scale Ball-Grid Array

The CB196 package is a chip-scale, fully-populated, ball-grid array with 0.5 mm ball pitch.

Footprint Diagram

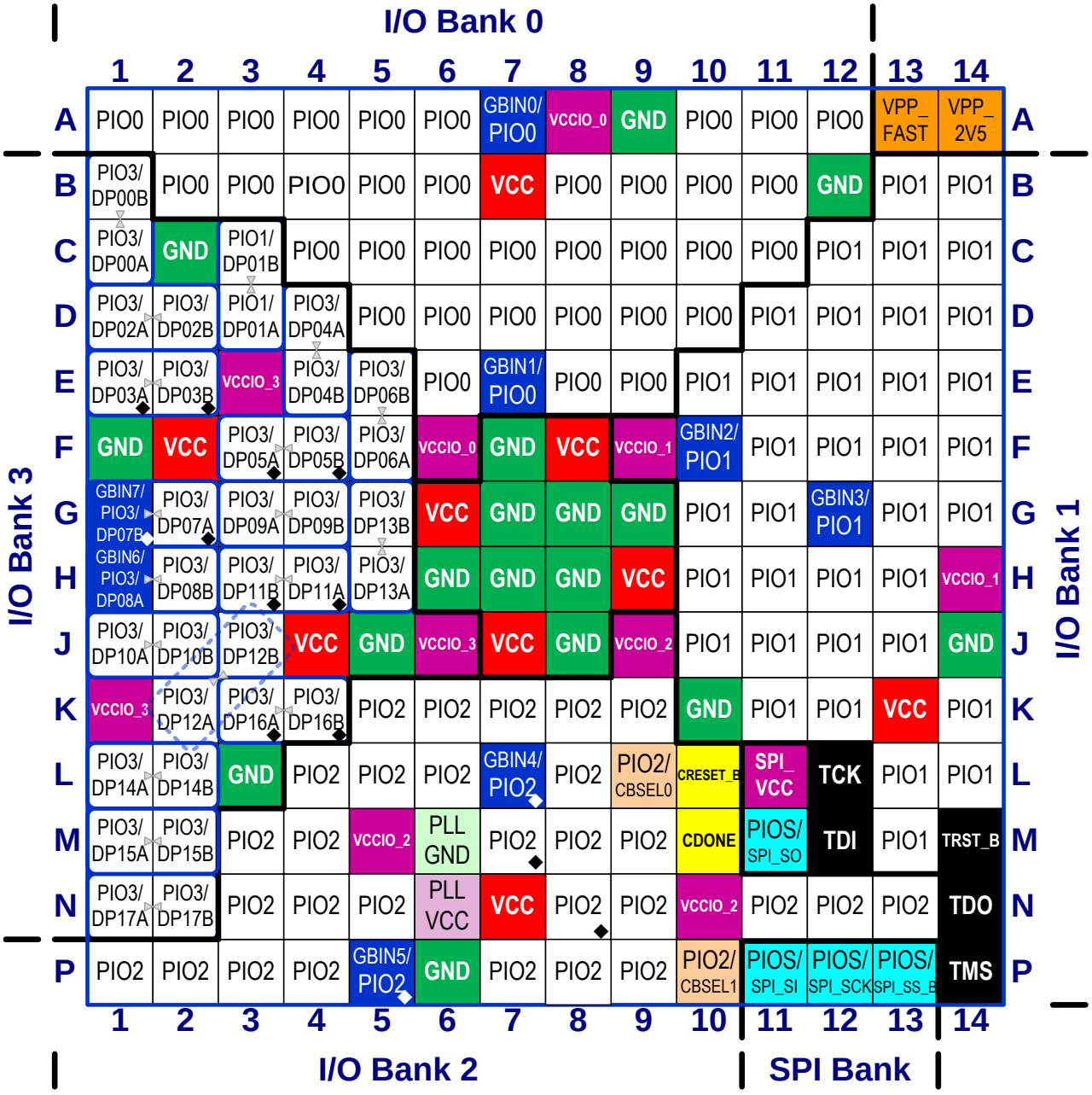
Figure 37 shows the iCE65P04 chip-scale BGA footprint for the 8 x 8 mm CB196 package.

Figure 34 shows the conventions used in the diagram.

Also see Table 47 for a complete, detailed pinout for the 196-ball chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 37: **iCE65P04 CB196 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 47 provides a detailed pinout table for the iCE65P04 in the CB196 chip-scale BGA package. Pins are generally arranged by I/O bank, then by ball function.

Table 47: **iCE65P04 CB196 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	A7	GBIN	0
GBIN1/PIO0	E7	GBIN	0
PIO0	A1	PIO	0
PIO0	A2	PIO	0
PIO0	A3	PIO	0
PIO0	A4	PIO	0
PIO0	A5	PIO	0
PIO0	A6	PIO	0
PIO0	A10	PIO	0
PIO0	A11	PIO	0
PIO0	A12	PIO	0
PIO0	B2	PIO	0
PIO0	B3	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B6	PIO	0
PIO0	B8	PIO	0
PIO0	B9	PIO	0
PIO0	B10	PIO	0
PIO0	B11	PIO	0
PIO0	C4	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	C10	PIO	0
PIO0	C11	PIO	0
PIO0	D5	PIO	0
PIO0	D6	PIO	0
PIO0	D7	PIO	0
PIO0	D8	PIO	0
PIO0	D9	PIO	0
PIO0	D10	PIO	0
PIO0	E6	PIO	0
PIO0	E8	PIO	0
PIO0	E9	PIO	0
VCCIO_0	A8	VCCIO	0
VCCIO_0	F6	VCCIO	0
GBIN2/PIO1	F10	GBIN	1
GBIN3/PIO1	G12	GBIN	1
PIO1	B13	PIO	1
PIO1	B14	PIO	1
PIO1	C12	PIO	1
PIO1	C13	PIO	1
PIO1	C14	PIO	1
PIO1	D11	PIO	1
PIO1	D12	PIO	1
PIO1	D13	PIO	1
PIO1	D14	PIO	1
PIO1	E10	PIO	1

Ball Function	Ball Number	Pin Type	Bank
PIO3/DP16A (◆)	***iCE65P04:*** K3	DPIO	3
PIO3/DP16B (◆)	***iCE65P08:*** K4	DPIO	3
PIO3/DP17A	N1	DPIO	3
PIO3/DP17B	N2	DPIO	3
VCCIO_3	E3	VCCIO	3
VCCIO_3	J6	VCCIO	3
VCCIO_3	K1	VCCIO	3
PIOS/SPI_SO	M11	SPI	SPI
PIOS/SPI_SI	P11	SPI	SPI
PIOS/SPI_SCK	P12	SPI	SPI
PIOS/SPI_SS_B	P13	SPI	SPI
SPI_VCC	L11	SPI	SPI
PLLGND	M6	PLLGND	PLL
PLLVCC	N6	PLLVCC	PLL
GND	A9	GND	GND
GND	B12	GND	GND
GND	C2	GND	GND
GND	F1	GND	GND
GND	F7	GND	GND
GND	G7	GND	GND
GND	G8	GND	GND
GND	G9	GND	GND
GND	H6	GND	GND
GND	H7	GND	GND
GND	H8	GND	GND
GND	J5	GND	GND
GND	J8	GND	GND
GND	J14	GND	GND
GND	K10	GND	GND
GND	L3	GND	GND
GND	P6	GND	GND
VCC	B7	VCC	VCC
VCC	F2	VCC	VCC
VCC	F8	VCC	VCC
VCC	G6	VCC	VCC
VCC	H9	VCC	VCC
VCC	J4	VCC	VCC
VCC	J7	VCC	VCC
VCC	K13	VCC	VCC
VCC	N7	VCC	VCC
VPP_2V5	A14	VPP	VPP
VPP_FAST	A13	VPP	VPP

Package Mechanical Drawing

Figure 38: **CB196 Package Mechanical Drawing**

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO0_17	C9	C18	217	2,087.00	2,962.80
PIO0_18	B9	C17	218	2,052.00	2,860.80
PIO0_19	D8	C16	219	2,017.00	2,962.80
PIO0_20	C8	C15	220	1,982.00	2,860.80
PIO0_21	E8	C14	221	1,947.00	2,962.80
PIO0_22	B8	C13	222	1,912.00	2,860.80
GBIN1/PIO0_23	E7	E11	223	1,877.00	2,962.80
GND	B12	C12	224	1,842.00	2,860.80
GND	—	—	225	1,807.00	2,962.80
GBIN0/PIO0_24	A7	E10	226	1,772.00	2,860.80
PIO0_25	D7	C11	227	1,737.00	2,962.80
PIO0_26	C7	C10	228	1,702.00	2,860.80
PIO0_27	E6	C9	229	1,667.00	2,962.80
VCC	B7	C8	230	1,632.00	2,860.80
VCC	—	—	231	1,597.00	2,962.80
PIO0_28	A6	C7	232	1,562.00	2,860.80
PIO0_29	B6	C6	233	1,527.00	2,962.80
PIO0_30	A5	C5	234	1,492.00	2,860.80
PIO0_31	D6	C4	235	1,457.00	2,962.80
GND	F7	K11	236	1,422.00	2,860.80
GND	—	—	237	1,387.00	2,962.80
PIO0_32	—	C3	238	1,352.00	2,860.80
PIO0_33	—	A7	239	1,317.00	2,962.80
PIO0_34	—	A6	240	1,282.00	2,860.80
PIO0_35	—	A5	241	1,247.00	2,962.80
PIO0_36	C6	G11	242	1,212.00	2,860.80
VCCIO_0	F6	K10	243	1,177.00	2,962.80
VCCIO_0	F6	K10	244	1,142.00	2,860.80
PIO0_37	C5	H11	245	1,107.00	2,962.80
PIO0_38	B5	G10	246	1,072.00	2,860.80
PIO0_39	A4	E9	247	1,037.00	2,962.80
PIO0_40	B4	H10	248	1,002.00	2,860.80
PIO0_41	D5	G9	249	967.00	2,962.80
PIO0_42	A3	E8	250	917.00	2,860.80
GND	G7	L11	251	867.00	2,962.80
PIO0_43	B3	H9	252	817.00	2,860.80
PIO0_44	C4	G8	253	767.00	2,962.80
PIO0_45	A2	E7	254	717.00	2,860.80
PIO0_46	A1	E6	255	667.00	2,962.80
PIO0_47	B2	E5	256	617.00	2,860.80

Electrical Characteristics

All parameter limits are specified under worst-case supply voltage, junction temperature, and processing conditions.

Absolute Maximum Ratings

Stresses beyond those listed under Table 50 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 50: **Absolute Maximum Ratings**

Symbol	Description	Minimum	Maximum	Units
VCC	Core supply Voltage	–0.5	1.42	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply			V
VPP_FAST	Optional fast NVCM programming supply			V
VCCIO_0 **VCCIO_1** **VCCIO_2** **SPI_VCC**	I/O bank supply voltage (I/O Banks 0, 1, and 2 plus SPI interface)	–0.5	4.00	V
VCCIO_3	I/O Bank 3 supply voltage	–0.5	3.60	V
VIN_0 **VIN_1** **VIN_2** **VIN_SPI**	Voltage applied to PIO pin within a specific I/O bank (I/O Banks 0, 1, and 2 plus SPI interface)	–1.0	5.5	V
VIN_3 **VIN_VREF**	Voltage applied to PIO pin within I/O Bank 3	–0.5	3.60	V
VCCPLL	Analog voltage supply to the Phase Locked Loop (PLL)	–0.5	3.60	V
$\mathbf{I_{OUT}}$	DC output current per pin	—	20	mA
$\mathbf{T_J}$	Junction temperature	–55	125	°C
$\mathbf{T_{STG}}$	Storage temperature, no bias	–65	150	°C

Recommended Operating Conditions

Table 51: **Recommended Operating Conditions**

Symbol	Description		Minimum	Nominal	Maximum	Units
VCC	Core supply voltage	High Performance, low-power	1.14	1.20	1.26	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply	Release from Power-on Reset	1.30	—	3.47	V
		Configure from NVCM	2.30	—	3.47	V
		NVCM programming	2.30	—	3.00	V
VPP_FAST	Optional fast NVCM programming supply		Leave unconnected in application			
SPI_VCC	SPI interface supply voltage		1.71	—	3.47	V
VCCIO_0 VCCIO_1 VCCIO_2 VCCIO_3 SPI_VCC	I/O standards, all banks	**LVCMOS33**	2.70	3.30	3.47	V
		LVCMOS25, LVDS	2.38	2.50	2.63	V
		LVCMOS18, SubLVDS	1.71	1.80	1.89	V
		LVCMOS15	1.43	1.50	1.58	V
VCCIO_3	I/O standards only available in I/O Bank 3	**SSTL2**	2.38	2.50	2.63	V
		SSTL18	1.71	1.80	1.89	V
		MDDR	1.71	1.80	1.89	V
VCCPLL	Analog voltage supply to the Phase Locked Loop (PLL)		1.71	2.50	2.63	V
T_A	Ambient temperature	Commercial (C)	0	—	70	°C
		Industrial (I)	–40	—	85	°C
$\mathbf{T_{PROG}}$	NVCM programming temperature		10	25	30	°C

NOTE:

VPP_FAST is only used for fast production programming. Leave floating or unconnected in application. When the iCE65P device is active, VPP_2V5 must be connected to a valid voltage.

I/O Characteristics

Table 52: **PIO Pin Electrical Characteristics**

Symbol	Description	Conditions	Minimum	Nominal	Maximum	Units
I_I	Input pin leakage current	V_{IN} = $VCCIO_{max}$ to 0 V			±10	µA
I_{OZ}	Three-state I/O pin (Hi-Z) leakage current	V_O = $VCCIO_{max}$ to 0 V			±10	µA
C_{PIO}	PIO pin input capacitance			6		pF
C_{GBIN}	GBIN global buffer pin input capacitance			6		pF
R_{PULLUP}	Internal PIO pull-up resistance during configuration	VCCIO = 3.3V		40		kΩ
		VCCIO = 2.5V		50		kΩ
		VCCIO = 1.8V		90		kΩ
		VCCIO = 1.5V				kΩ
		VCCIO = 1.2V				kΩ
V_{HYST}	Input hysteresis	VCCIO = 1.5V to 3.3V		50		mV

NOTE: All characteristics are characterized and may or may not be tested on each pin on each device.

Single-ended I/O Characteristics

Table 53: **I/O Characteristics (I/O Banks 0, 1, 2 and SPI only)**

I/O Standard	Nominal I/O Bank Supply Voltage	Input Voltage (V)		Output Voltage (V)		Output Current at Voltage (mA)	
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{OL}	I_{OH}
LVCMOS33	3.3V	0.80	2.00	0.4	2.40	8	8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	6	6
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	1.40	4	4
LVCMOS15	1.5V	Not supported: Use I/O Bank 3 and SPI Bank		0.4	1.20	2	2

Table 54: **I/O Characteristics (I/O Bank 3 only)**

I/O Standard	Supply Voltage	Input Voltage (V)		Output Voltage (V)		I/O Attribute Name	mA at Voltage
		Max. V_{IL}	Min. V_{IH}	Max. V_{OL}	Min. V_{OH}		I_{OL}, I_{OH}
LVCMOS33	3.3V	0.80	2.20	0.4	2.40	SL_LVCMOS33_8	±8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	SB_LVCMOS25_16	±16
						SB_LVCMOS25_12	±12
						SB_LVCMOS25_8 *	±8
						SB_LVCMOS25_4	±4
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_LVCMOS18_10	±10
						SB_LVCMOS18_8	±8
						SB_LVCMOS18_4 *	±4
						SB_LVCMOS18_2	±2
LVCMOS15	1.5V	35% VCCIO	65% VCCIO	25% VCCIO	75% VCCIO	SB_LVCMOS15_4	±4
						SB_LVCMOS15_2 *	±2
MDDR	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_MDDR10	±10
						SB_MDDR8	±8
						SB_MDDR4 *	±4
						SB_MDDR2	±2
SSTL2 (Class 2)	2.5V	VREF–0.180	VREF+0.180	0.35	VTT+0.430	SB_SSTL2_CLASS_2	±16.2
SSTL2 (Class 1)				0.54		SB_SSTL2_CLASS_1	±8.1
SSTL18 (Full)	1.8V	VREF–0.125	VREF+0.125	0.28	VTT+0.280	SB_SSTL18_FULL	±13.4
SSTL18 (Half)				VTT–0.475	VTT+0.475	SB_SSTL18_HALF	±6.7

NOTES:
SSTL2 and SSTL18 I/O standards require the VREF input pin, which is only available on the CB284 package and for die-based products.

RAM4K Block

Table 59 provides timing information for the logic in a RAM4K block, which includes the paths shown in Figure 50.

Figure 50: **RAM4K Timing Circuit**

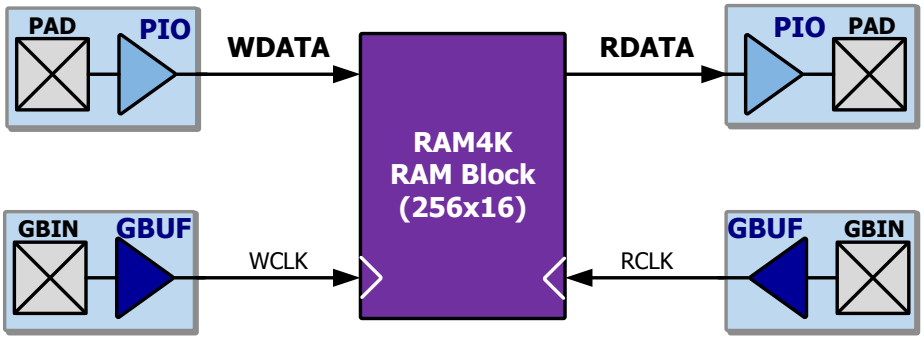


Table 59: **Typical RAM4K Block Timing**

Symbol	From	To	Description	Power/Speed Grade: –T Nominal VCC: 1.2 V Typ.	Units
Write Setup/Hold Time					
t_{SUWD}	PIO input	GBIN input	Minimum write data setup time on PIO inputs before active clock edge on GBIN input, include interconnect delay.	0.8	ns
t_{HDWD}	GBIN input	PIO input	Minimum write data hold time on PIO inputs after active clock edge on GBIN input, including interconnect delay.	0	ns
Read Clock-Output-Time					
t_{CKORD}	RCLK clock input	PIO output	Clock-to-output delay from RCLK input pin, through RAM4K RDATA output flip-flop to PIO output pad, including interconnect delay.	7.3	ns
t_{GBCKRM}	GBIN input	RCLK clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to the RCLK clock input.	2.6	ns
Write and Read Clock Characteristics					
t_{RMWCKH}	WCLK RCLK	WCLK RCLK	Write clock High time	0.54	ns
t_{RMWCKL}			Write clock Low time	0.63	ns
t_{RMWCYC}			Write clock cycle time	1.27	ns
F_{WMAX}			Sustained write clock frequency	256	MHz

Phase-Locked Loop (PLL) Block

Table 59 provides timing information for the Phase-Locked Loop (PLL) block shown in Figure 50.

Figure 51: **Phase-Locked Loop (PLL)**

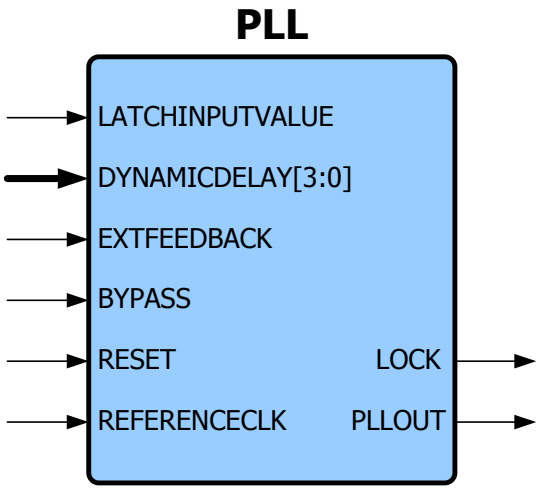


Table 60: **Phase-Locked Loop (PLL) Block Timing**

Symbol	From	To	Description	Power/Speed Grade: –T Nominal VCC: 1.2 V Min.	Typical	Max.	Units
Frequency Range							
F_{REF}			Input clock frequency range	10	—	133	MHz
F_{OUT}			Output clock frequency range (cannot exceed maximum frequency supported by global buffers)	10	—	533	MHz
Duty Cycle							
PLL_{IJ}			Input duty cycle	35	—	65	%
Tw_{HI}			Input clock high time	2.5	—	—	ns
Tw_{LOW}			Input clock low time	2.5	—	—	ns
PLL_{OJD}			Output duty cycle (divided frequency)	45	—	55	%
PLL_{OJM}			Output duty cycle (undivided frequency)	40	—	60	%
Fine Delay							
t_{FDTAP}			Fine delay adjustment, per tap		165		ps
PLL_{TAPS}			Fine delay adjustment settings	0	—	15	taps
PLL_{FDAM}			Maximum delay adjustment		2.5		ns
Jitter							
PLL_{IPJ}			Input clock period jitter	—	—	+/- 300	ps
PLL_{OPJ}			PLLOUT output period jitter	—	1% or ≤ 100	+/- 1.1% output period or ≥ 110	ps
Lock/Reset Time							
t_{LOCK}			PLL lock time after receive stable, monotonic REFERENCECLK input	—	—	50	µs
tw_{RST}			Minimum reset pulse width	20	—	—	ns

Notes:

1. Output jitter performance is affected by input jitter. A clean reference clock < 100ps jitter must be used to ensure best jitter performance.
2. The output jitter specification refers to the intrinsic jitter of the PLL.