Lattice Semiconductor Corporation - ICE65P04F-TCB196C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	148
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	196-VFBGA, CSPBGA
Supplier Device Package	196-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65p04f-tcb196c

Logic Cell (LC)

Each iCE65P device contains thousands of Logic Cells (LCs), as listed in Table 1. Each Logic Cell includes three primary logic elements, shown in Figure 3.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, of up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

The output from a Logic Cell is available to all inputs to all eight Logic Cells within the Programmable Logic Block. Similarly, the Logic Cell output feeds into the **Error! Reference source not found.** fabric to connect to other eatures on the iCE65P device.

Look-Up Table (LUT4)

The four-input Look-Up Table (LUT4) function implements any and all combinational logic functions, regardless of complexity, of between zero and four inputs. Zero-input functions include "High" (1) and "Low" (0). The LUT4 function has four inputs, labeled I0, I1, I2, and I3. Three of the four inputs are shared with the Carry Logic function, as shown in Figure 3. The bottom-most LUT4 input connects either to the I3 input or to the Carry Logic output from the previous Logic Cell.

The output from the LUT4 function connects to the flip-flop within the same Logic Cell. The LUT4 output or the flip-flop output then connects to the programmable interconnect.

For detailed LUT4 internal timing, see Table 57.

'D'-style Flip-Flop (DFF)

The 'D'-style flip-flop (DFF) optionally stores state information for the application.

Figure 3: **Programmable Logic Block and Logic Cell**

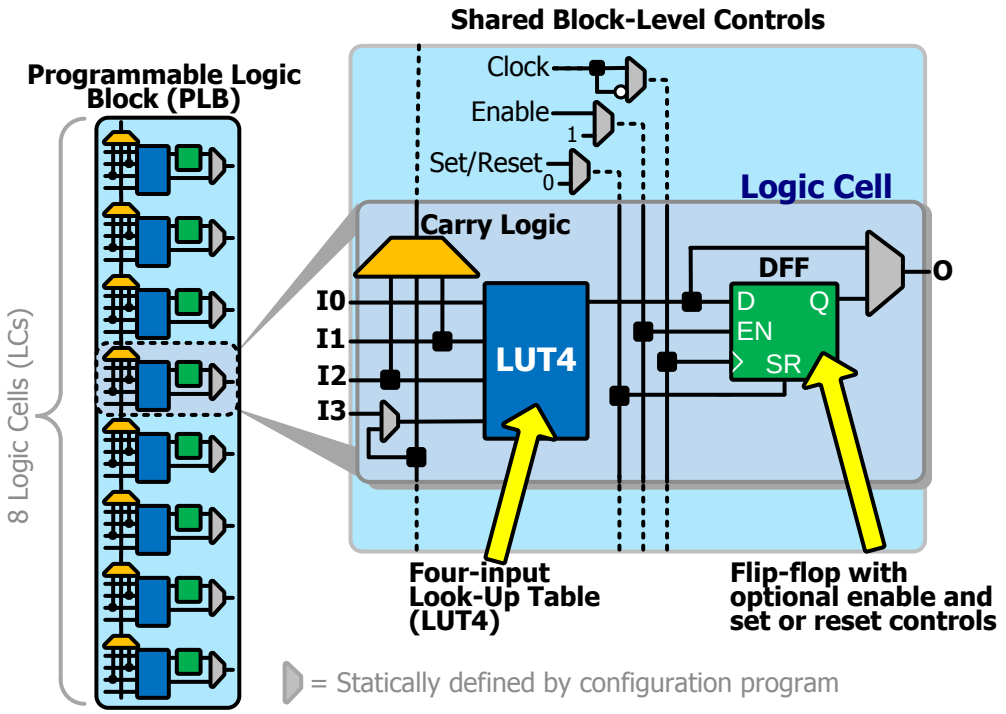


Table 4: **Flip-flop Packing/Sharing within a PLB**

Group	Active Clock Edge	Clock Enable	Set or Reset Control (Sync. or Async)
1	↑	None (always enabled)	None
2	↓		
3	↑		PLB set/reset control
4	↓		
5	↑	Selective (controlled by PLB clock enable)	None
6	↓		
7	↑		PLB set/reset control
8	↓		

For detailed flip-flop internal timing, see Table 57.

Carry Logic

The dedicated Carry Logic within each Logic Cell primarily accelerates and improves the efficiency of arithmetic logic such as adders, accumulators, subtracters, incrementers, decrementers, counters, ALUs, and comparators. The Carry Logic also supports wide combinational logic functions.

$$COUT = I1 \bullet I2 + CIN \bullet I1 + CIN \bullet I2 \qquad \text{[Equation 1]}$$

Equation 1 and Figure 4 describe the Carry Logic structure within a Logic Cell. The Carry Logic shares inputs with the associated Look-Up Table (LUT4). The LUT4's I1 and I2 inputs directly feed the Carry Logic; inputs I0 and I3 do not. A signal cascades between Logic Cells within the Programmable Logic Block. The carry input from the previous adjacent Logic Cell optionally provides an alternate input to the LUT4 function, supplanting the I3 input.

Low-Power Disable

To save power and prevent unnecessary signal switching, the Carry Logic function within a Logic Cell is disabled if not used. The output of a Logic Cell's Carry Logic is forced High.

PLB Carry Input and Carry Output Connections

As shown in Figure 4, each Programmable Logic Block has a carry input signal that can be initialized High, Low, or come from the carry output signal from PLB immediately below.

Similarly, the Carry Logic output from the Programmable Logic Block connects to the PLB immediately above, which allows the Carry Logic to span across multiple PLBs in a column. As shown in Figure 5, the Carry Logic chain can be tapped mid-way through a chain or a PLB by feeding the value through a LUT4 function.

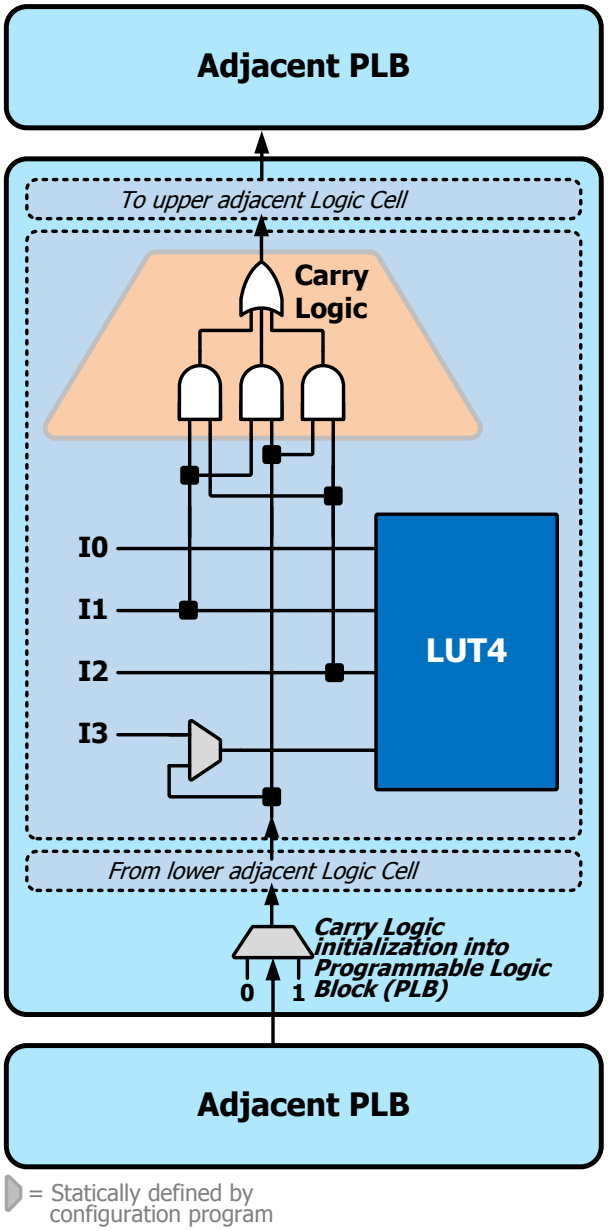
Adder Example

Figure 5 shows an example design that uses the Carry Logic. The example is a 2-bit adder, which can be expanded into an adder of arbitrary size. The LUT4 function within a Logic Cell is programmed to calculate the sum of the two input values and the carry input, `A[i] + B[i] + CARRY_IN[i-1] = SUM[i]`.

The Carry Logic generates the carry value to feed the next bit in the adder. The calculated carry value replaces the I3 input to the next LUT4 in the upper Logic Cell.

If required by the application, the carry output from the final stage of the adder is available by passing it through the final LUT4.

Figure 4: **Carry Logic Structure within a Logic Cell and between PLBs**



Input Signal Path

As shown in Figure 6, a signal from a package pin optionally feeds directly into the device, or is held in an input register. The input signal connects to the programmable interconnect resources through the IN signal. Table 9 describes the input behavior, assuming that the output path is not used or if a bidirectional I/O, that the output driver is in its high-impedance state (Hi-Z). Table 9 also indicates the effect of the Power-Saving I/O Bank iCEgate Latch and the Input Pull-Up Resistors on I/O Banks 0, 1, and 2.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Power-Saving I/O Bank iCEgate Latch

To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control. As shown in Figure 9, the iCEgate HOLD control signal captures the external value from the associated asynchronous input. The HOLD signal prevents switching activity on the PIO pad from affecting internal logic or programmable interconnect. Minimum power consumption occurs when there is no switching. However, individual pins within the I/O bank can bypass the iCEgate latch and directly feed into the programmable interconnect, remaining active during low-power operation. This behavior is described in Table 9. The decision on which asynchronous inputs use the iCEgate feature and which inputs bypass it is determined during system design. In other words, the iCEgate function is part of the source design used to create the iCE65P configuration image.

Figure 9: **Power-Saving iCEgate Latch**

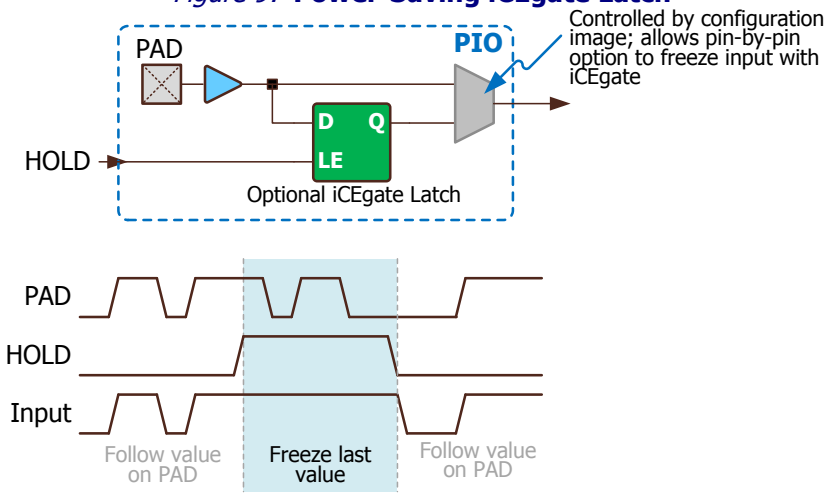


Table 9: **PIO Non-Registered Input Operations**

Operation	HOLD	Bitstream Setting		PAD	IN
	iCEgate Latch	Controlled by iCEgate?	Input Pull-Up Enabled?	Pin Value	Input Value to Interconnect
Data Input	0	X	X	PAD	PAD Value
Pad Floating, No Pull-up	0	X	No	Z	(Undefined)
Pad Floating, Pull-up	0	X	Yes	Z	1
Data Input, Latch Bypassed	X	No	X	PAD	PAD Value
Pad Floating, No Pull-up, Latch Bypassed	X	No	No	Z	(Undefined)
Pad Floating, Pull-up, Latch Bypassed	X	No	Yes	Z	1
Low Power Mode, Hold Last Value	1	Yes	X	X	Last Captured PAD Value

There are four iCEgate HOLD controls, one per each I/O bank. The iCEgate HOLD control input originates within the interconnect fabric, near the middle of the I/O edge. Consequently, the HOLD signal is optionally controlled externally through a PIO pin or from other logic within the iCE65P device.

Global Routing Resources

Global Buffers

Each iCE65P component has eight global buffer routing connections, illustrated in Figure 13.

There are eight high-drive buffers, connected to the eight low-skew, global lines. These lines are designed primarily for clock distribution but are also useful for other high-fanout signals such as set/reset and enable signals. The global buffers originate either from the Global Buffer Inputs (GBINx) or from programmable interconnect. The associated GBINx pin represents the best pin to drive a global buffer from an external source. However, the application with an iCE65P FPGA can also drive a global buffer via any other PIO pin or from internal logic using the programmable interconnect.

If not used in an application, individual global buffers are turned off to save power.

Figure 13: **High-drive, Low-skew, High-fanout Global Buffer Routing Resources**

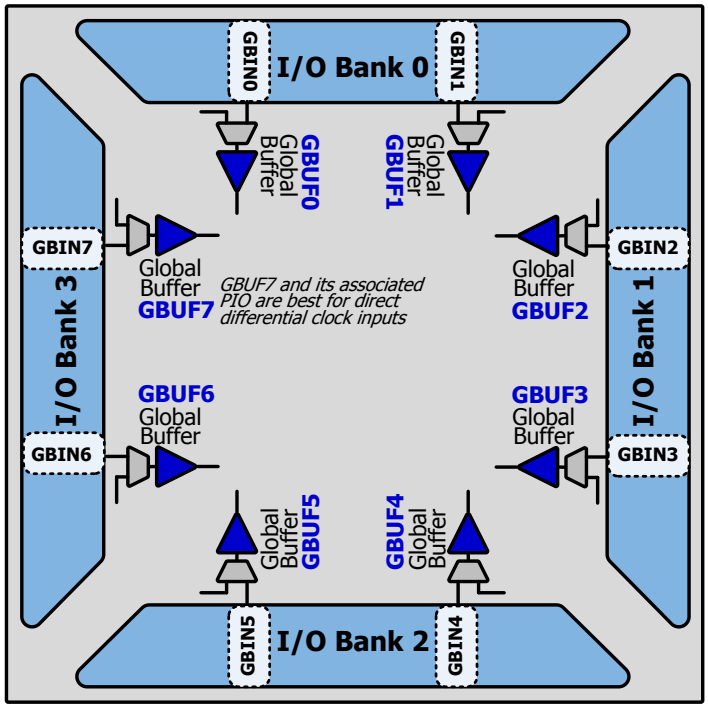


Table 11 lists the connections between a specific global buffer and the inputs on a Programmable Logic Block (PLB). All global buffers optionally connect to all clock inputs. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input.

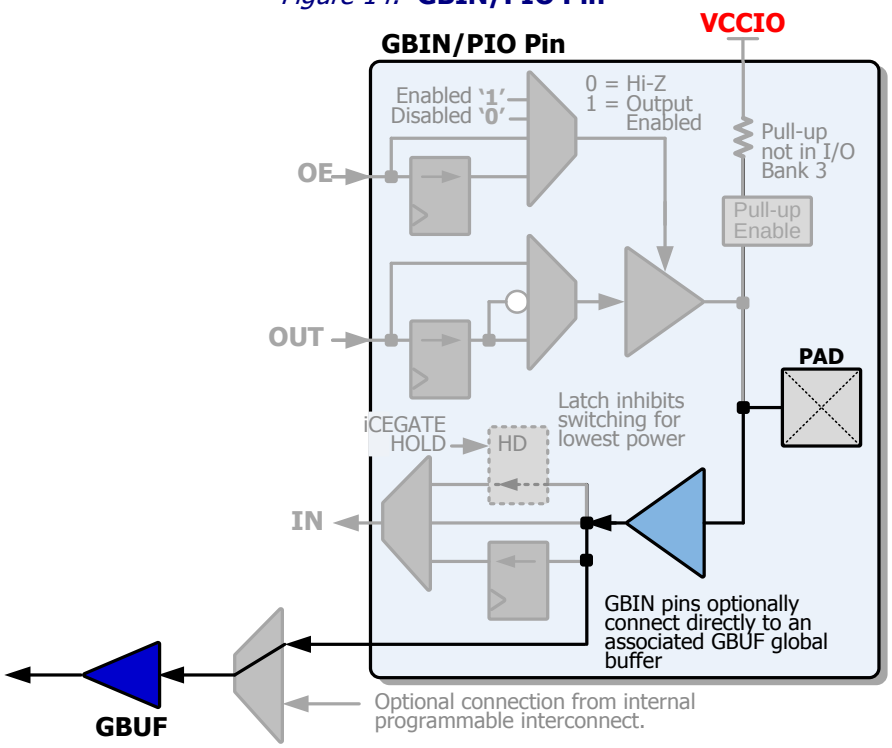
Table 11: **Global Buffer (GBUF) Connections to Programmable Logic Block (PLB)**

Global Buffer	LUT Inputs	Clock	Clock Enable	Reset
GBUF0	Yes, any 4 of 8 GBUF buffers	Yes	Yes	No
GBUF1		Yes	No	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	No	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	No	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	No	Yes

Table 14: **Global Buffer Input Ball Number by Package**

Global Buffer Input (GBIN)	I/O Bank	Package Code		
		`P04 CB121	**`P04 CB196**	**`P04 CB284**
GBIN0	0	D6	A7	E10
GBIN1		C6	E7	E11
GBIN2	1	F9	F10	L18
GBIN3		F8	G12	K18
GBIN4	2	L9	L7	V12
GBIN5		L8	P5	V11
GBIN6	3	F4	H1	M5
GBIN7		D3	G1	L5

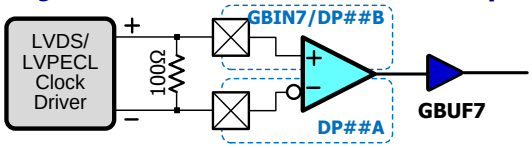
Figure 14: **GBIN/PIO Pin**



Differential Global Buffer Input

All eight global buffer inputs support single-ended I/O standards such as LVCMOS. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct SubLVDS, LVDS, or LVPECL differential clock input, as shown in Figure 15. The GBIN7 and its associated differential I/O pad accept a differential clock signal. A 100 Ω termination resistor is required across the two pads. Optionally, swap the outputs from the LVDS or LVPECL clock driver to invert the clock as it enters the iCE65P device.

Figure 15: **LVDS or LVPECL Clock Input**



Nonvolatile Configuration Memory (NVCM)

All standard iCE65P devices have an internal, nonvolatile configuration memory (NVCM). The NVCM is large enough to program a complete iCE65P device, including initializing all RAM4K block locations (MAXIMUM column in Table 28). The NVCM memory also has very high programming yield due to extensive error checking and correction (ECC) circuitry.

The NVCM is ideal for cost-sensitive, high-volume production applications, saving the cost and board space associated with an external configuration PROM. Furthermore, the NVCM provides exceptional design security, protecting critical intellectual property (IP). The NVCM contents are entirely contained within the iCE65P device and are not readable once protected by the one-time programmable Security bits. Furthermore, there is no observable difference between a programmed or un-programmed memory cell using optical or electron microscopy.

The NVCM memory has a programming interface similar to a 25-series SPI serial Flash PROM. Consequently, it can be programmed using standard device programmers before or after circuit board assembly or programmed in-system from a microprocessor or other intelligent controller.

Configuration Control Signals

The iCE65P configuration process is self-timed and controlled by a few internal signals and device I/O pins, as described in Table 29.

Table 29: **iCE65P Configuration Control Signals**

Signal Name	Direction	Description
POR	Internal control	Internal Power-On Reset (POR) circuit.
OSC	Internal control	Internal configuration oscillator.
CRESET_B	Input	Configuration Reset input. Active-Low. No internal pull-up resistor.
CDONE	Open-drain Output	Configuration Done output. Permanent, weak pull-up resistor to VCCIO_2.

The Power-On Reset circuit, POR, automatically resets the iCE65P component to a known state during power-up (cold boot). The POR circuit monitors the relevant voltage supply inputs, as shown in Figure 25. Once all supplies exceed their minimum thresholds, the configuration controller can start the configuration process.

The configuration controller begins configuring the iCE65P device, clocked by the Internal Oscillator, OSC. The OSC oscillator continues controlling configuration unless the iCE65P device is configured using the SPI Peripheral Configuration Interface.

Figure 24: **iCE65P Configuration Control Pins**

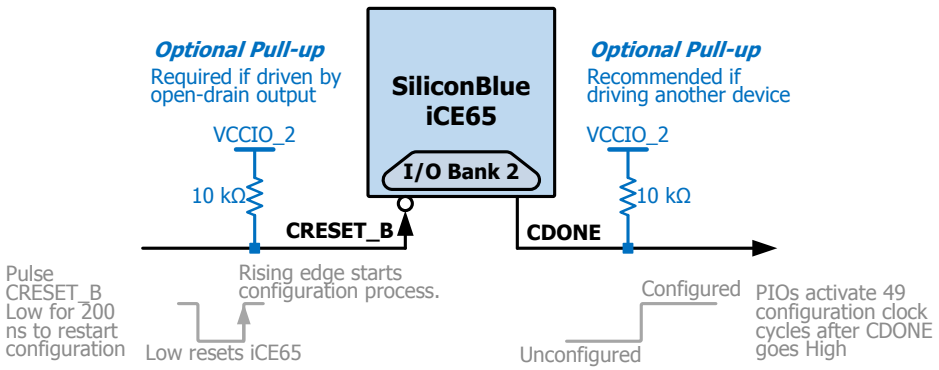


Figure 24 shows the two iCE65P configuration control pins, CRESET_B and CDONE. Table 30 lists the Ball numbers for the configuration control pins by package. When driven Low for at least 200 ns, the dedicated Configuration Reset input, CRESET_B, resets the iCE65P device. When CRESET_B returns High, the iCE65P FPGA restarts the configuration process from its power-on conditions (Cold Boot). The CRESET_B pin is a pure input with no internal pull-up resistor. If driven by open-drain driver or un-driven, then connect the CRESET_B pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

Table 30: **Configuration Control Ball Numbers by Package**

Configuration Control Pins	Package Code		
	CB121	**CB196**	**CB284**
CRESET_B	K7	L10	R14
CDONE	J7	M10	T14

The iCE65P device signals the end of the configuration process by actively turning off the internal pull-down transistor on the Configuration Done output pin, CDONE. The pin has a permanent, weak internal pull-up resistor to the VCCIO_2 rail. If the iCE65P device drives other devices, then optionally connect the CDONE pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

The PIO pins activate according to their configured function after 49 configuration clock cycles. The internal oscillator is the configuration clock source for the SPI Master Configuration Interface and when configuring from Nonvolatile Configuration Memory (NVCM). When using the SPI Peripheral Configuration Interface, the configuration clock source is the SPI_SCK clock input pin.

Internal Oscillator

During SPI Master or NVCM configuration mode, the controlling clock signal is generated from an internal oscillator. The oscillator starts operating at the Default frequency. During the configuration process, however, bit settings within the configuration bitstream can specify a higher-frequency mode in order to maximize SPI bandwidth and reduce overall configuration time. See Table 61: Internal Oscillator Frequency on page 81 for the specified oscillator frequency range.

Using the SPI Master Configuration Interface, internal oscillator controls all the interface timing and clocks the SPI serial Flash PROM via the SPI_SCK clock output pin.

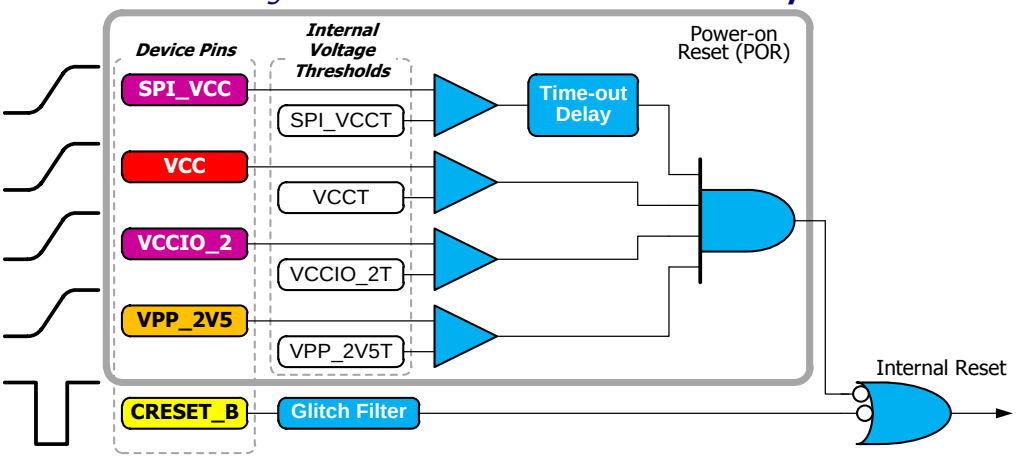
The oscillator output, which also supplies the SPI SCK clock output during the SPI Flash configuration process, has a 50% duty cycle.

Internal Device Reset

Figure 25 presents the various signals that internally reset the iCE65P internal logic.

- Power-On Reset (POR)
- CRESET_B Pin
- JTAG Interface

Figure 25: **iCE65P Internal Reset Circuitry**



Power-On Reset (POR)

The Power-on Reset (POR) circuit monitors specific voltage supply inputs and holds the device in reset until all the relevant supplies exceed the internal voltage thresholds. The SPI_VCC supply also has an additional time-out delay to allow an attached SPI serial PROM to power up properly. Table 31 shows the POR supply inputs. The Nonvolatile Configuration Memory (NVCM) requires that the VPP_2V5 supply be connected, even if the application does not use the NVCM.

Table 31: **Power-on Reset (POR) Voltage Resources**

Supply Rail	iCE65P Production Devices
VCC	Yes
SPI_VCC	Yes
VCCIO_1	No
VCCIO_2	Yes
VPP_2V5	Yes

CRESET_B Pin

The CRESET_B pin resets the iCE65P internal logic when Low.

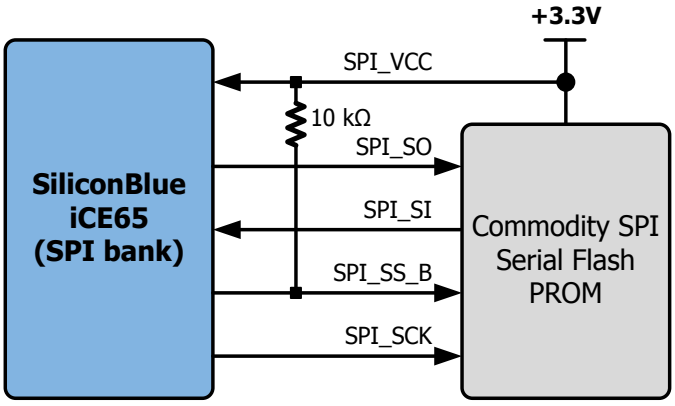
JTAG Interface

Specific command sequences also reset the iCE65P internal logic.

SPI Master Configuration Interface

All iCE65P devices, including those with NVCM, can be configured from an external, commodity SPI serial Flash PROM, as shown in Figure 26. The SPI configuration interface is essentially its own independent I/O bank, powered by the VCC_SPI supply input. Presently, most commercially-available SPI serial Flash PROMs require a 3.3V supply.

Figure 26: **iCE65P SPI Master Configuration Interface**



The SPI configuration interface is used primarily during development before mass production, where the configuration is then permanently programmed in the NVCM configuration memory. However, the SPI interface can also be the primary configuration interface allowing easy in-system upgrades and support for multiple configuration images.

The SPI control signals are defined in Table 32. Table 33 lists the SPI interface ball or pins numbers by package.

Table 32: **SPI Master Configuration Interface Pins (SPI_SS_B High before Configuration)**

Signal Name	Direction	Description
SPI_VCC	Supply	SPI Flash PROM voltage supply input.
SPI_SO	Output	SPI Serial Output from the iCE65P device.
SPI_SI	Input	SPI Serial Input to the iCE65P device, driven by the select SPI serial Flash PROM.
SPI_SS_B	Output	SPI Slave Select output from the iCE65P device. Active Low.
SPI_SCK	Output	SPI Slave Clock output from the iCE65P device.

Enabling SPI Configuration Interface

To enable the SPI configuration mode, the SPI_SS_B pin must be allowed to float High. The SPI_SS_B pin has an internal pull-up resistor. If SPI_SS_B is Low, then the iCE65P component defaults to the SPI Slave configuration mode.

SPI Master Configuration Process

The iCE65P SPI Master Configuration Interface supports a variety of modern, high-density, low-cost SPI serial Flash PROMs. Most modern SPI PROMs include a power-saving Deep Power-down mode. The iCE65P component exploits this mode for additional system power savings.

The iCE65P SPI interface starts by driving SPI_SS_B Low, and then sends a Release from Power-down command to the SPI PROM, hexadecimal command code 0xAB. Figure 27 provides an example waveform. This initial command wakes up the SPI PROM if it is already in Deep Power-down mode. If the PROM is not in Deep Power-down mode, the extra command has no adverse affect other than that it requires a few additional microseconds during the configuration process. The iCE65P device transmits data on the SPI_SO output, on the falling edge of the SPI_SCK output. The SPI PROM does not provide any data to the iCE65P device's SPI_SI input. After sending the last command bit, the iCE65P device de-asserts SPI_SS_B High, completing the command. The iCE65P device then waits a minimum of 10 µS before sending the next SPI PROM command.

Figure 27: **SPI Release from Deep Power-down Command**

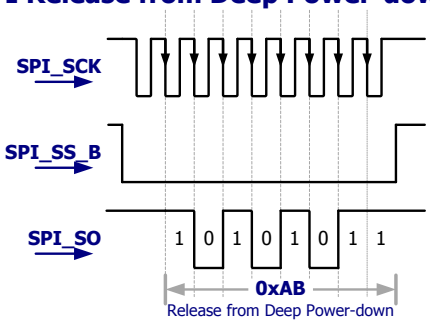
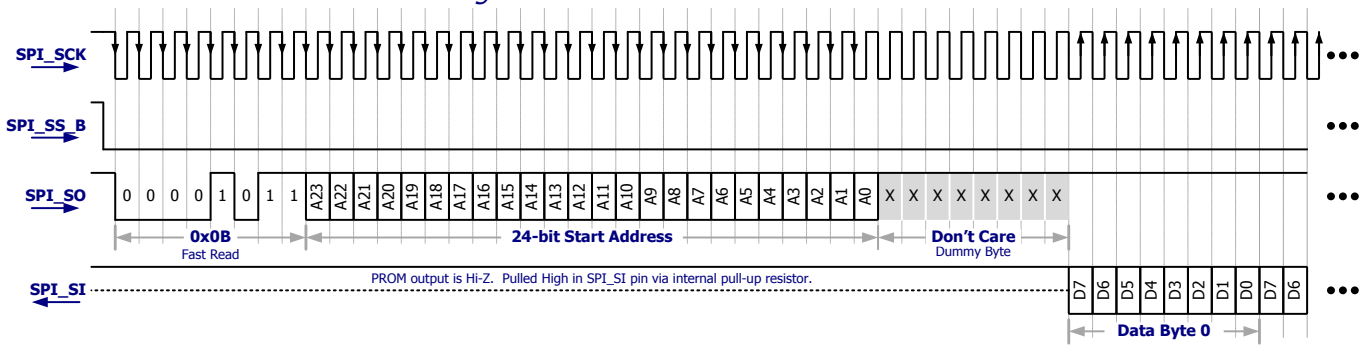


Figure 28 illustrates the next command issued by the iCE65P device. The iCE65P SPI interface again drives SPI_SS_B Low, followed by a Fast Read command, hexadecimal command code 0x0B, followed by a 24-bit start address, transmitted on the SPI_SO output. The iCE65P device provides data on the falling edge of SPI_SS_B. Upon initial power-up, the start address is always 0x00_0000. After waiting eight additional clock cycles, the iCE65P device begins reading serial data from the SPI PROM. Before presenting data, the SPI PROM's serial data output is high-impedance. The SPI_SI input pin has an internal pull-up resistor and sees high-impedance as logic '1'.

Figure 28: **SPI Fast Read Command**



The external SPI PROM supplies data on the falling edge of the iCE65P device's SPI_SCK clock output. The iCE65P device captures each PROM data value on the SPI_SI input, using the rising edge of the SPI_SCK clock signal. The SPI PROM data starts at the 24-bit address presented by the iCE65P device. PROM data is serially output, byte by byte, with most-significant bit, D7, presented first. The PROM automatically increments an internal byte counter as long as the PROM is selected and clocked.

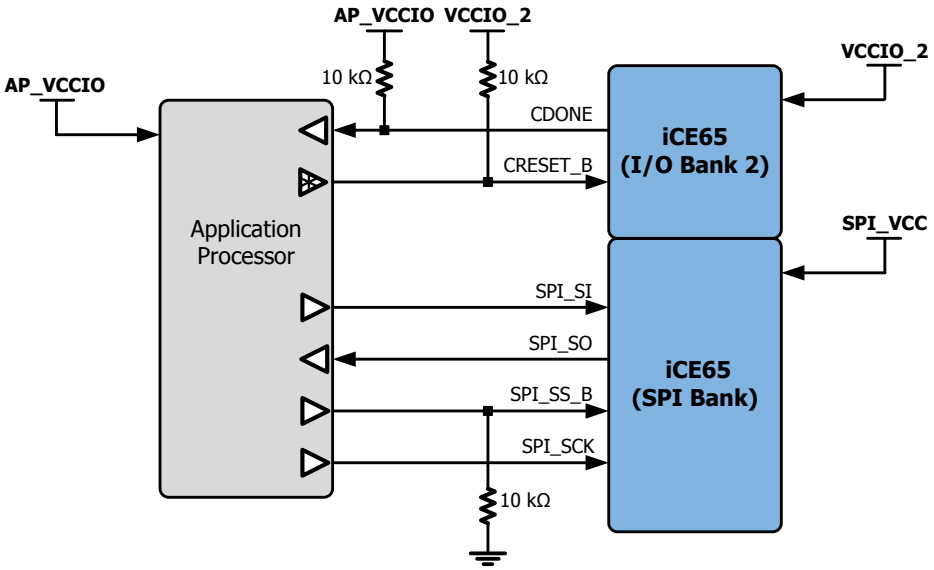
The iCE65P device attempts to reconfigure six times. If not successful after six attempts, the iCE65P FPGA automatically goes into low-power mode.

SPI Peripheral Configuration Interface

Using the SPI peripheral configuration interface, an application processor (AP) serially writes a configuration image to an iCE65P FPGA using the iCE65's SPI interface, as shown in Figure 26. The iCE65's SPI configuration interface is a separate, independent I/O bank, powered by the VCC_SPI supply input. Typically, VCC_SPI is the same voltage as the application processor's I/O. The configuration control signals, CDONE and CRESET_B, are supplied by the separate I/O Bank 2 voltage input, VCCIO_2.

This same SPI peripheral interface supports programming for the iCE65's Nonvolatile Configuration Memory (NVCM).

Figure 31: **iCE65P SPI Peripheral Configuration Interface**



The SPI control signals are defined in Table 32.

Table 36: **SPI Peripheral Configuration Interface Pins (SPI_SS_B Low when CRESET_B Released)**

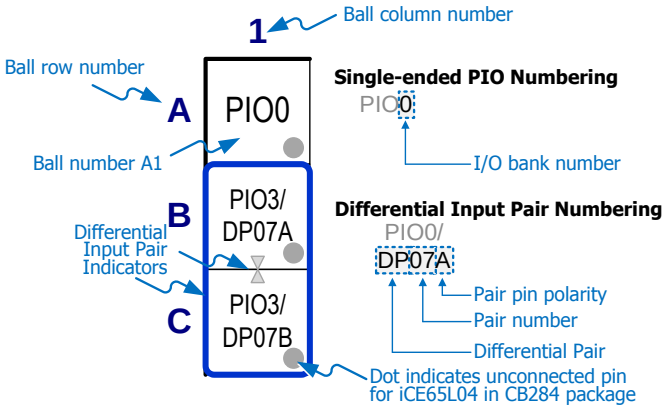
Signal Name	Direction	iCE65P I/O Supply	Description
CDONE	AP ← iCE65	VCCIO_2	Configuration Done output from iCE65. Connect to a 10kΩ pull-up resistor to the application processor I/O voltage, AP_VCC.
CRESET_B	AP → iCE65		Configuration Reset input on iCE65. Typically driven by AP using an open-drain driver, which also requires a 10kΩ pull-up resistor to VCCIO_2.
SPI_VCC	Supply	SPI_VCC	SPI Flash PROM voltage supply input.
SPI_SI	AP → iCE65		SPI Serial Input to the iCE65P FPGA, driven by the application processor.
SPI_SO	AP ← iCE65		SPI Serial Output from CE65 device to the application processor. Not actually used during SPI peripheral mode configuration but required if the SPI interface is also used to program the NVCM.
SPI_SS_B	AP → iCE65		SPI Slave Select output from the application processor. Active Low. Optionally hold Low prior to configuration using a 10kΩ pull-down resistor to ground.
SPI_SCK	AP → iCE65		SPI Slave Clock output from the application processor.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

iCE65P Package Footprint Diagram Conventions

Figure 34 illustrates the naming conventions used in the following footprint diagrams. Each PIO pin is associated with an I/O Bank. PIO pins in I/O Bank 3 that support differential inputs are also numbered by differential input pair.

Figure 34: **CS and CB Package Footprint Diagram Conventions**



Pinout Differences between iCE65P04 and iCE65L04

The iCE65P04 FPGA is designed to be nearly pin-compatible with the iCE65L04 FPGA. The primary difference is that the iCE65P04 requires power and ground inputs for the PLL as shown in Table 44 and Table 45. The tables list the package balls that are different between the iCE65P04 and the iCE65L04 pinouts for the CB196 and CB284 packages.

Table 44: **Pinout Differences between iCE65P04 and iCE65L04 in CB196 Package**

Ball Number	iCE65P04	iCE65L04
M6	PLLGND	PIO2
N6	PLLVCC	PIO2

Table 45: **Pinout Differences between iCE65P04 and iCE65L04 in CB284 Package**

Ball Number	iCE65P04	iCE65L04
Y9	PLLGND	PIO2
Y10	PLLVCC	PIO2

Ball Function	Ball Number	Pin Type	Bank
PIO0	A4	PIO	0
PIO0	A5	PIO	0
PIO0	A6	PIO	0
PIO0	A7	PIO	0
PIO0	A8	PIO	0
PIO0	A10	PIO	0
PIO0	B3	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B8	PIO	0
PIO0	B9	PIO	0
PIO0	C5	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	D5	PIO	0
PIO0	D7	PIO	0
PIO0	E5	PIO	0
PIO0	E6	PIO	0
PIO0	E7	PIO	0
PIO0	F7	PIO	0
VCCIO_0	B7	VCCIO	0
GBIN2/PIO1	F9	GBIN	1
GBIN3/PIO1	F8	GBIN	1
PIO1	A11	PIO	1
PIO1	B11	PIO	1
PIO1	C11	PIO	1
PIO1	D8	PIO	1
PIO1	D9	PIO	1
PIO1	D10	PIO	1
PIO1	D11	PIO	1
PIO1	E8	PIO	1
PIO1	E9	PIO	1
PIO1	E11	PIO	1
PIO1	F10	PIO	1
PIO1	G7	PIO	1
PIO1	G8	PIO	1
PIO1	G9	PIO	1
PIO1	G10	PIO	1
PIO1	H7	PIO	1
PIO1	H8	PIO	1
PIO1	H9	PIO	1
PIO1	H10	PIO	1
VCCIO_1	E10	VCCIO	1
CDONE	J7	CONFIG	2
CRESET_B	K7	CONFIG	2
GBIN4/PIO2	L9	GBIN	2
GBIN5/PIO2	L8	GBIN	2
PIO2	H4	PIO	2
PIO2	H5	PIO	2
PIO2	H11	PIO	2

Ball Function	Ball Number	Pin Type	Bank
PIO2	J4	PIO	2
PIO2	J5	PIO	2
PIO2	J11	PIO	2
PIO2	K3	PIO	2
PIO2	K4	PIO	2
PIO2	K11	PIO	2
PIO2	L2	PIO	2
PIO2	L3	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L10	PIO	2
PIO2	L11	PIO	2
PIO2/CBSEL0	H6	PIO	2
PIO2/CBSEL1	J6	PIO	2
VCCIO_2	K5	VCCIO	2
PIO3/DP00A	C1	DPIO	3
PIO3/DP00B	B1	DPIO	3
PIO3/DP01A	D1	DPIO	3
PIO3/DP01B	E2	DPIO	3
PIO3/DP02A	C2	DPIO	3
PIO3/DP02B	D2	DPIO	3
PIO3/DP03A	C3	DPIO	3
PIO3/DP03B	C4	DPIO	3
PIO3/DP04A	E4	DPIO	3
PIO3/DP04B	D4	DPIO	3
PIO3/DP05A	F3	DPIO	3
PIO3/DP05B	G3	DPIO	3
PIO3/DP06B	G4	DPIO	3
GBIN6/PIO3/DP06A	F4	GBIN	3
GBIN7/PIO3/DP07B	D3	GBIN	3
PIO3/DP07A	E3	DPIO	3
PIO3/DP08A	F2	DPIO	3
PIO3/DP08B	G1	DPIO	3
PIO3/DP09A	H1	DPIO	3
PIO3/DP09B	J1	DPIO	3
PIO3/DP10A	H2	DPIO	3
PIO3/DP10B	H3	DPIO	3
PIO3/DP11A	J3	DPIO	3
PIO3/DP11B	J2	DPIO	3
PIO3/DP12A	K1	DPIO	3
PIO3/DP12B	L1	DPIO	3
VCCIO_3	A1	VCCIO	3
VCCIO_3	G2	VCCIO	3
PIOS/SPI_SO	J8	SPI	SPI
PIOS/SPI_SI	K8	SPI	SPI
PIOS/SPI_SCK	K9	SPI	SPI
PIOS/SPI_SS_B	J9	SPI	SPI
SPI_VCC	J10	SPI	SPI
PLLGND	L6	PLLGND	PLL
PLLVCC	L7	PLLVCC	PLL

Ball Function	Ball Number	Pin Type	Bank
GND	B2	GND	GND
GND	B10	GND	GND
GND	E1	GND	GND
GND	F5	GND	GND
GND	F6	GND	GND
GND	G5	GND	GND
GND	G6	GND	GND
GND	G11	GND	GND
GND	K2	GND	GND
GND	K10	GND	GND
VCC	B6	VCC	VCC
VCC	F1	VCC	VCC
VCC	F11	VCC	VCC
VCC	K6	VCC	VCC
VPP_2V5	C10	VPP	VPP
VPP_FAST	A9	VPP	VPP

CB284 Chip-Scale Ball-Grid Array

The CB284 package, partially-populated 0.5 mm pitch, ball grid array simplifies PCB layout with empty ball rings.

Footprint Diagram

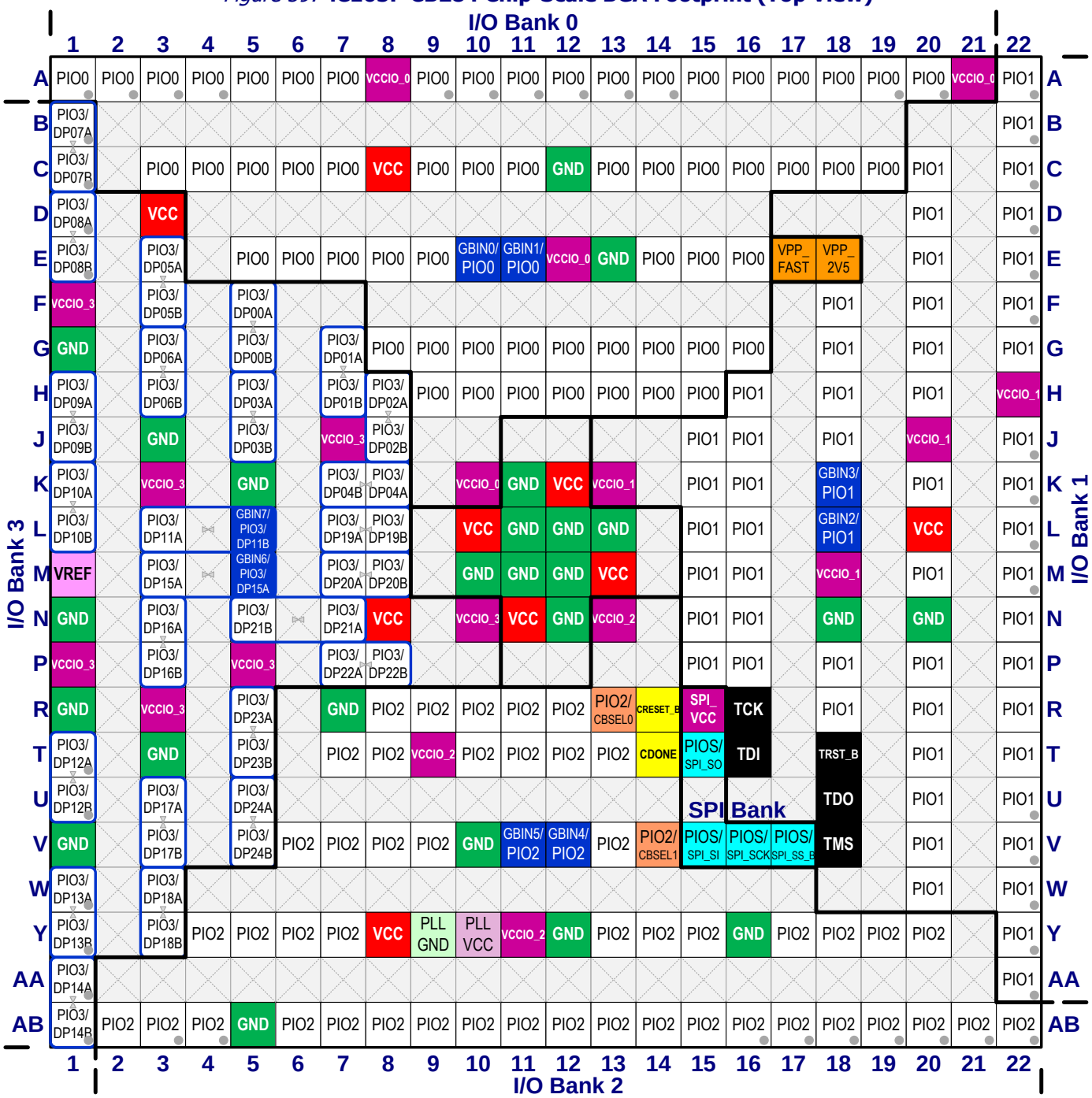
Figure 39 shows the CB284 chip-scale BGA footprint.

Figure 34 shows the conventions used in the diagram.

Also see Table 48 for a complete, detailed pinout for the 284-ball chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 39: **iCE65P CB284 Chip-Scale BGA Footprint (Top View)**

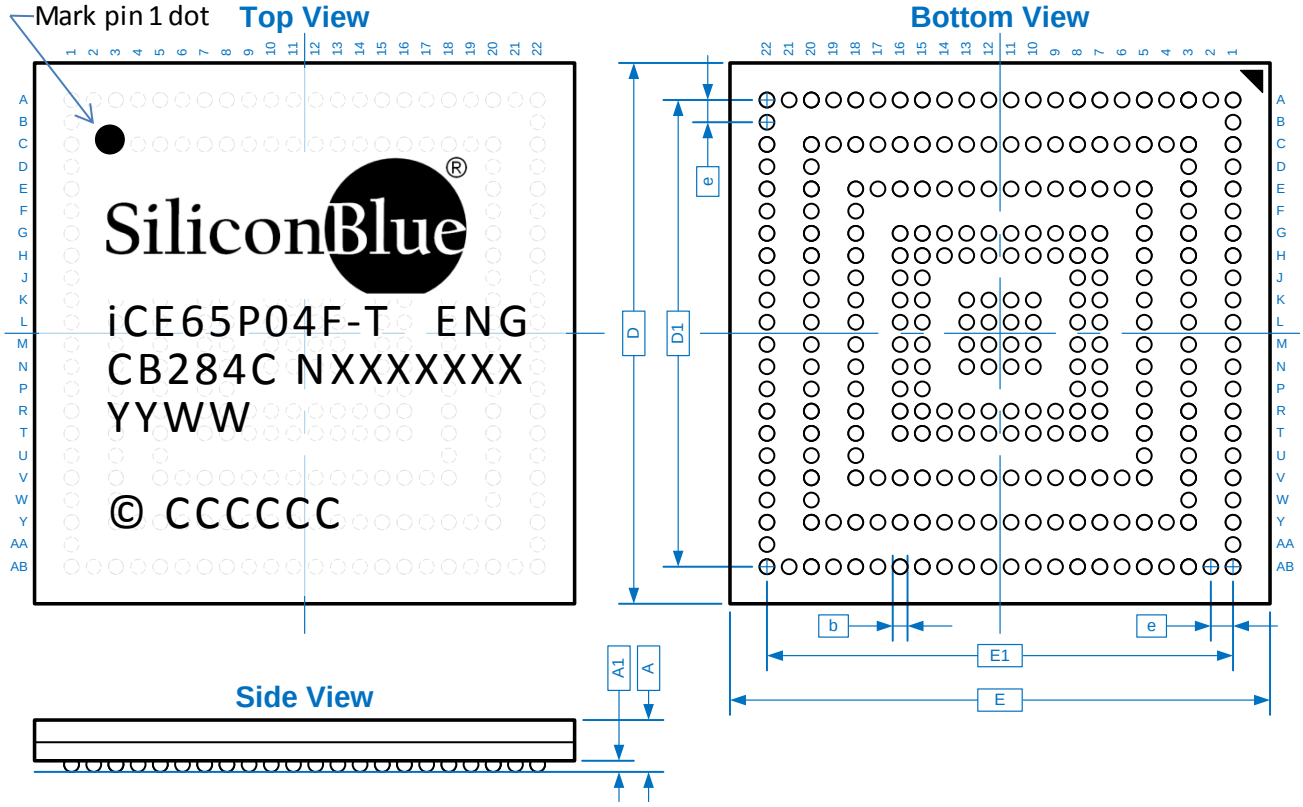


Ball Function	Ball Number	Pin Type by Device		Bank
		iCE65P04	iCE65P08	
PIO3/DP05B	F3	DPIO	DPIO	3
PIO3/DP06A	G3	DPIO	DPIO	3
PIO3/DP06B	H3	DPIO	DPIO	3
PIO3/DP07A (●)	B1	N.C.	DPIO	3
PIO3/DP07B (●)	C1	N.C.	DPIO	3
PIO3/DP08A (●)	D1	N.C.	DPIO	3
PIO3/DP08B (●)	E1	N.C.	DPIO	3
PIO3/DP09A	H1	DPIO	DPIO	3
PIO3/DP09B	J1	DPIO	DPIO	3
PIO3/DP10A	K1	DPIO	DPIO	3
PIO3/DP10B	L1	DPIO	DPIO	3
PIO3/DP11A	L3	DPIO	DPIO	3
GBIN7/PIO3/DP11B	L5	GBIN	GBIN	3
PIO3/DP12A (●)	T1	N.C.	DPIO	3
PIO3/DP12B (●)	U1	N.C.	DPIO	3
PIO3/DP13A (●)	W1	N.C.	DPIO	3
PIO3/DP13B (●)	Y1	N.C.	DPIO	3
PIO3/DP14A (●)	AA1	N.C.	DPIO	3
PIO3/DP14B (●)	AB1	N.C.	DPIO	3
GBIN6/PIO3/DP15A	M5	GBIN	GBIN	3
PIO3/DP15B	M3	DPIO	DPIO	3
PIO3/DP16A	N3	DPIO	DPIO	3
PIO3/DP16B	P3	DPIO	DPIO	3
PIO3/DP17A	U3	DPIO	DPIO	3
PIO3/DP17B	V3	DPIO	DPIO	3
PIO3/DP18A	W3	DPIO	DPIO	3
PIO3/DP18B	Y3	DPIO	DPIO	3
PIO3/DP19A	L7	DPIO	DPIO	3
PIO3/DP19B	L8	DPIO	DPIO	3
PIO3/DP20A	M7	DPIO	DPIO	3
PIO3/DP20B	M8	DPIO	DPIO	3
PIO3/DP21A	N7	DPIO	DPIO	3
PIO3/DP21B	N5	DPIO	DPIO	3
PIO3/DP22A	P7	DPIO	DPIO	3
PIO3/DP22B	P8	DPIO	DPIO	3
PIO3/DP23A	R5	DPIO	DPIO	3
PIO3/DP23B	T5	DPIO	DPIO	3
PIO3/DP24A	U5	DPIO	DPIO	3
PIO3/DP24B	V5	DPIO	DPIO	3
VCCIO_3	F1	VCCIO	VCCIO	3
VCCIO_3	P1	VCCIO	VCCIO	3
VCCIO_3	J7	VCCIO	VCCIO	3
VCCIO_3	K3	VCCIO	VCCIO	3
VCCIO_3	N10	VCCIO	VCCIO	3
VCCIO_3	P5	VCCIO	VCCIO	3
VCCIO_3	R3	VCCIO	VCCIO	3
VREF	M1	VREF	VREF	3

Package Mechanical Drawing

Figure 40: **CB284 Package Mechanical Drawing**

CB284: 12 x 12 mm, 284-ball, 0.5 mm ball-pitch, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			22		Columns
Number of Ball Rows	Y			22		Rows
Number of Signal Balls		n		284		Balls
Body Size	X	E	11.90	12.00	12.10	mm
	Y	D	11.90	12.00	12.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	10.50	—	
	Y	D1	—	10.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65P04F	Part number
	-T	Power/Speed
	ENG	Engineering
3	CB284C NXXXXXXX	Package type and Lot number
4	YYWW	Date Code
5	N/A	Blank
6	© CCCCCC	Country

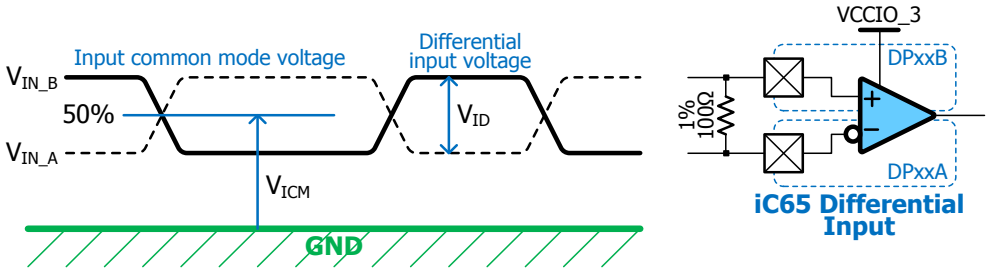
Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
35	28

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIOS_00/SPI_SO	M11	T15	124	2,690.00	37.20
PIOS_01/SPI_SI	P11	V15	125	2,740.00	139.20
GND	P6	Y16	126	2,790.00	37.20
PIOS_02/SPI_SCK	P12	V16	127	2,840.00	139.20
PIOS_03/SPI_SS_B	P13	V17	128	2,890.00	37.20
SPI_VCC	L11	R15	129	2,990.00	37.20
TDI	M12	T16	130	3,610.80	342.00
TMS	P14	V18	131	3,712.80	392.00
TCK	L12	R16	132	3,610.80	442.00
TDO	N14	U18	133	3,712.80	492.00
TRST_B	M14	T18	134	3,610.80	542.00
PIO1_00	K11	R18	135	3,712.80	592.00
PIO1_01	L13	P16	136	3,610.80	642.00
PIO1_02	K12	P15	137	3,712.80	692.00
PIO1_03	M13	P18	138	3,610.80	727.00
GND	J14	N18	139	3,712.80	762.00
GND	J14	N18	140	3,610.80	797.00
PIO1_04	J10	N16	141	3,712.80	832.00
PIO1_05	L14	N15	142	3,610.80	867.00
VCCIO_1	H14	M18	143	3,712.80	902.00
VCCIO_1	—	—	144	3,610.80	937.00
PIO1_06	J11	M16	145	3,712.80	972.00
PIO1_07	K14	M15	146	3,610.80	1,007.00
PIO1_08	H10	W20	147	3,712.80	1,042.00
PIO1_09	J13	V20	148	3,610.80	1,077.00
PIO1_10	J12	U20	149	3,712.80	1,112.00
VCC	N7	M13	150	3,610.80	1,147.00
VCC	—	—	151	3,712.80	1,182.00
PIO1_11	H13	T22	152	3,610.80	1,217.00
PIO1_12	H12	R22	153	3,712.80	1,252.00
PIO1_13	—	P22	154	3,610.80	1,287.00
PIO1_14	—	N22	155	3,712.80	1,322.00
PIO1_15	G13	T20	156	3,610.80	1,357.00
PIO1_16	H11	R20	157	3,712.80	1,392.00
PIO1_17	G14	P20	158	3,610.80	1,427.00
GND	K10	N20	159	3,712.80	1,462.00
GND	—	—	160	3,610.80	1,497.00
PIO1_18	G10	M20	161	3,712.80	1,532.00
GBIN3/PIO1_19	G12	K18	162	3,610.80	1,567.00
GBIN2/PIO1_20	F10	L18	163	3,712.80	1,602.00
PIO1_21	F14	K20	164	3,610.80	1,637.00
VCCIO_1	H14	J20	165	3,712.80	1,672.00
VCCIO_1	—	—	166	3,610.80	1,707.00
PIO1_22	F13	H20	167	3,712.80	1,742.00
PIO1_23	D13	G20	168	3,610.80	1,777.00
PIO1_24	G11	F20	169	3,712.80	1,812.00

Differential Inputs

Figure 41: **Differential Input Specifications**



Input common mode voltage: $$V_{ICM} = \frac{VCCIO\_3}{2} \pm \Delta V_{ICM}$$

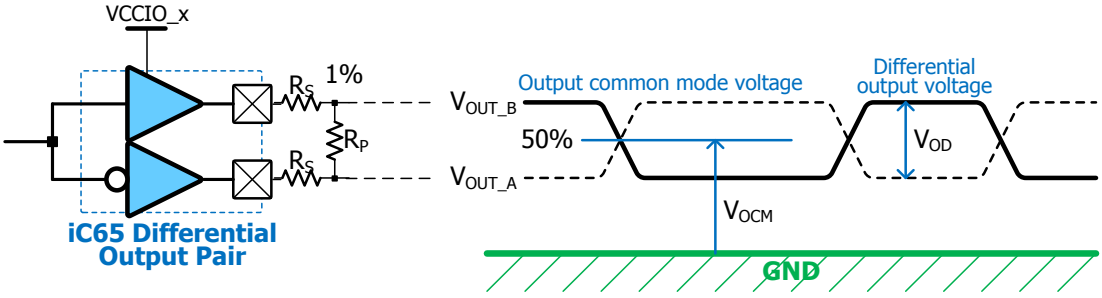
Differential input voltage: $$V_{ID} = |V_{IN\_B} - V_{IN\_A}|$$

Table 55: **Recommended Operating Conditions for Differential Inputs**

I/O Standard	VCCIO_3 (V)			V_{ID} (mV)			V_{ICM} (V)		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	250	350	450	$\frac{VCCIO\_3}{2} - 0.30$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.30$
SubLVDS	1.71	1.80	1.89	100	150	200	$\frac{VCCIO\_3}{2} - 0.25$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.25$

Differential Outputs

Figure 42: **Differential Output Specifications**



Output common mode voltage: $$V_{OCM} = \frac{VCCIO\_x}{2} \pm \Delta V_{OCM}$$

Differential output voltage: $$V_{OD} = |V_{OUT\_B} - V_{OUT\_A}|$$

Table 56: **Recommended Operating Conditions for Differential Outputs**

I/O Standard	VCCIO_x (V)			Ω		V_{OD} (mV)			V_{OCM} (V)		
	Min	**Nom**	**Max**	**R_S**	**R_P**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	150	140	300	350	400	$\frac{VCCIO}{2} - 0.15$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.15$
SubLVDS	1.71	1.80	1.89	270	120	100	150	200	$\frac{VCCIO}{2} - 0.10$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.10$