Lattice Semiconductor Corporation - ICE65P04F-TCB196I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

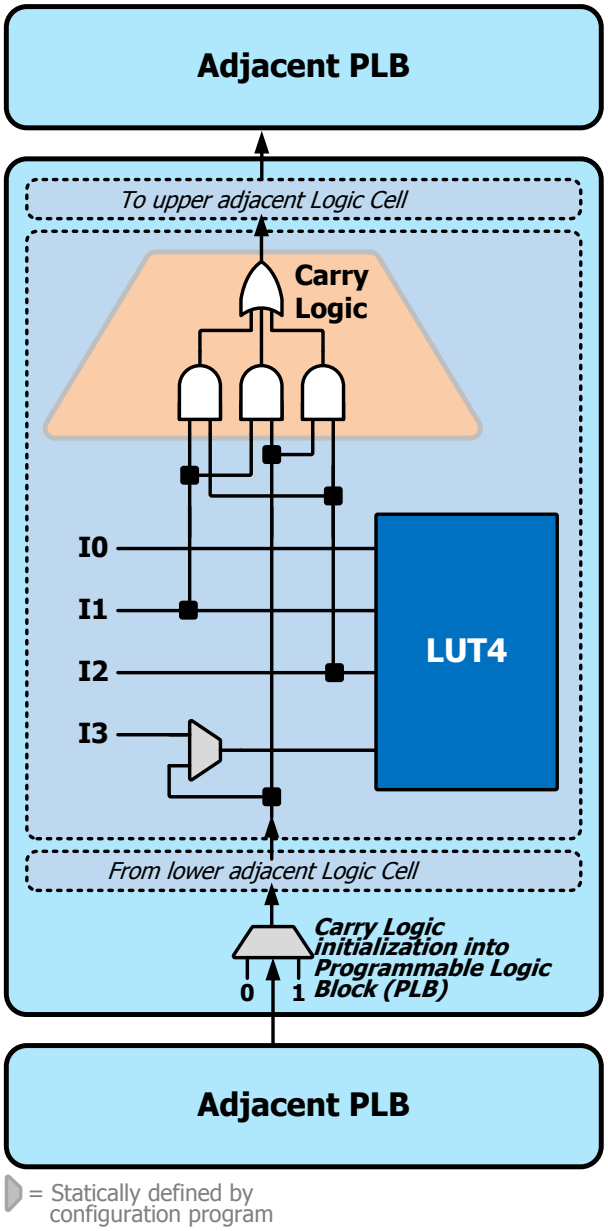
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	148
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	196-VFBGA, CSPBGA
Supplier Device Package	196-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65p04f-tcb196i

Figure 4: **Carry Logic Structure within a Logic Cell and between PLBs**

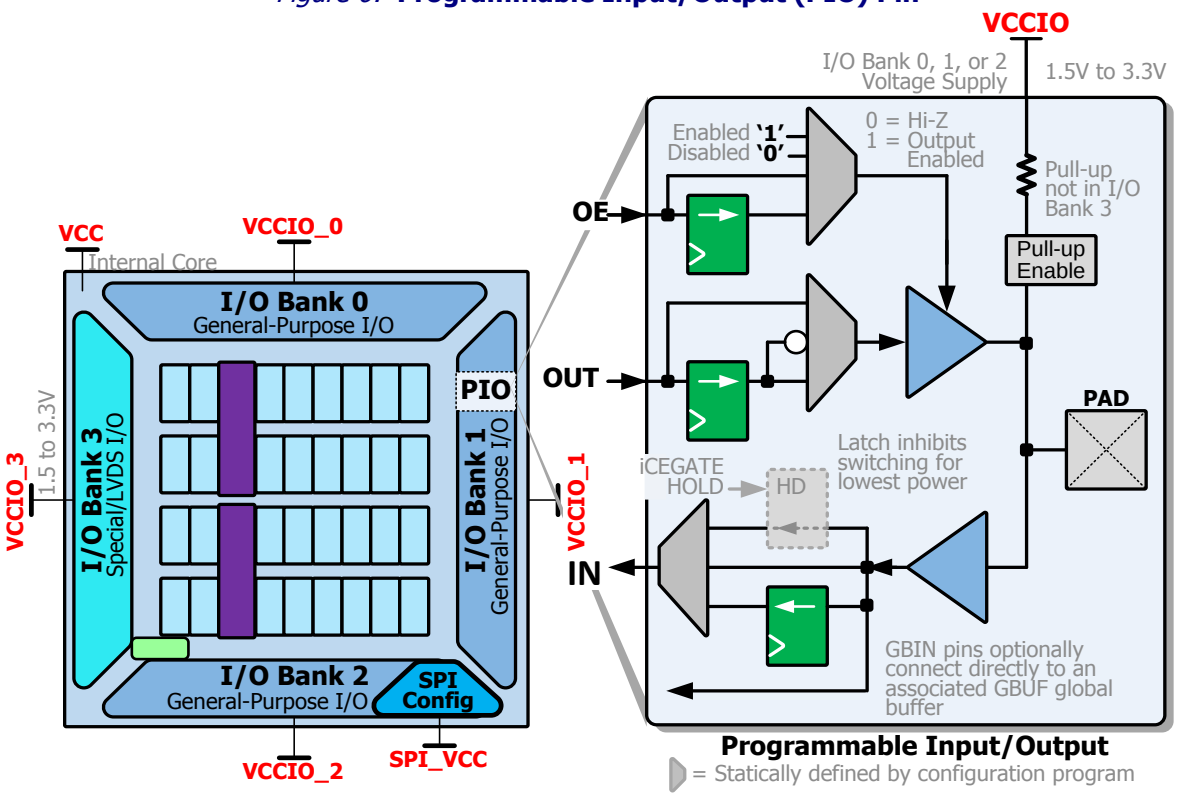


Programmable Input/Output Block (PIO)

Programmable Input/Output (PIO) blocks surround the periphery of the device and connect external components to the Programmable Logic Blocks (PLBs) and RAM4K blocks via programmable interconnect. Individual PIO pins are grouped into one of four I/O banks, as shown in Figure 6. I/O Bank 3 has additional capabilities, including LVDS differential I/O and the ability to interface to Mobile DDR memories.

Figure 6 also shows the logic within a PIO pin. When used in an application, a PIO pin becomes a signal input, an output, or a bidirectional I/O pin with a separate direction control input.

Figure 6: **Programmable Input/Output (PIO) Pin**



I/O Banks

PIO blocks are organized into four separate I/O banks, each with its own voltage supply input, as shown in Table 5. The voltage applied to the VCCIO pin on a bank defines the I/O standard used within the bank. Table 53 and Table 54 describe the I/O drive capabilities and switching thresholds by I/O standard. I/O Bank 3, along the left edge of the die, is different than the others and supports specialized I/O standards.

Because each I/O bank has its own voltage supply, iCE65P components become the ideal bridging device between different interface standards. For example, the iCE65P device allows a 1.8V-only processor to interface cleanly with a 3.3V bus interface. The iCE65P device replaces external voltage translators.

Table 5: **Supported Voltages by I/O Bank**

Bank	Device Edge	Supply Input	3.3V	2.5V	1.8V	1.5V
0	Top	VCCIO_0	Yes	Yes	Yes	Outputs only
1	Right	VCCIO_1	Yes	Yes	Yes	Outputs only
2	Bottom	VCCIO_2	Yes	Yes	Yes	Outputs only
3	Left	VCCIO_3	Yes	Yes	Yes	Yes
SPI	Bottom Right	SPI_VCC	Yes	Yes	Yes	No

If not connected to an external SPI PROM, the four pins associated with the SPI Master Configuration Interface can be used as PIO pins, supplied by the SPI_VCC input, essentially forming a fifth "mini" I/O bank. If using an SPI Flash PROM, then connect SPI_VCC to 3.3V.

Table 8 lists the I/O standards that can co-exist in I/O Bank 3, depending on the VCCIO_3 voltage.

Table 8: **Compatible I/O Standards in I/O Bank 3**

VCCIO_3 Voltage	3.3V	2.5V	1.8V	1.5V
Compatible I/O Standards	SB_LVCMOS33_8	Any SB_LVCMOS25 SB_SSTL2_Class_2 SB_SSTL2_Class_1 SB_LVDS_INPUT	Any SB_LVCMOS18 SB_SSTL18_FULL SB_SSTL18_HALF SB_MDDR10 SB_MDDR8 SB_MDDR4 SB_MDDR2 SB_LVDS_INPUT	Any SB_LVCMOS15

Programmable Output Drive Strength

Each PIO in I/O Bank 3 offers programmable output drive strength, as listed in Table 8. For the LVCMOS and MDDR I/O standards, the output driver has settings for static drive currents ranging from 2 mA to 16 mA output drive current, depending on the I/O standard and supply voltage.

The SSTL18 and SSTL2 I/O standards offer full- and half-strength drive current options

Differential Inputs and Outputs

All PIO pins support "single-ended" I/O standards, such as LVCMOS. However, iCE65P FPGAs also support differential I/O standards where a single data value is represented by two complementary signals transmitted or received using a pair of PIO pins. The PIO pins in I/O Bank 3 support Low-Voltage Differential Swing (LVDS) and SubLVDS inputs as shown in Figure 7. Differential outputs are available in all four I/O banks.

Differential Inputs Only on I/O Bank 3

Differential receivers are required for popular applications such as LVDS and LVPECL clock inputs, camera interfaces, and for various telecommunications standards.

Specific pairs of PIO pins in I/O Bank 3 form a differential input. Each pair consists of a DPxxA and DPxxB pin, where "xx" represents the pair number. The DPxxB receives the true version of the signal while the DPxxA receives the complement of the signal. Typically, the resulting signal pair is routed on the printed circuit board (PCB) with matched 50Ω signal impedance. The differential signaling, the low voltage swing, and the matched signal routing are ideal for communicating very-high frequency signals. Differential signals are generally also more tolerant of system noise and generate little EMI themselves.

The LVDS input circuitry requires 2.5V on the VCCIO_3 voltage supply. Similarly, the SubLVDS input circuitry requires 1.8V on the VCCIO_3 voltage supply. For electrical specifications, see "Differential Inputs" on page 75.

Each differential input pair requires an external 100 Ω termination resistor, as shown in Figure 7.

The PIO pins that make up a differential input pair are indicated with a blue bounding box in the footprint diagrams and in the pinout tables.

Nonvolatile Configuration Memory (NVCM)

All standard iCE65P devices have an internal, nonvolatile configuration memory (NVCM). The NVCM is large enough to program a complete iCE65P device, including initializing all RAM4K block locations (MAXIMUM column in Table 28). The NVCM memory also has very high programming yield due to extensive error checking and correction (ECC) circuitry.

The NVCM is ideal for cost-sensitive, high-volume production applications, saving the cost and board space associated with an external configuration PROM. Furthermore, the NVCM provides exceptional design security, protecting critical intellectual property (IP). The NVCM contents are entirely contained within the iCE65P device and are not readable once protected by the one-time programmable Security bits. Furthermore, there is no observable difference between a programmed or un-programmed memory cell using optical or electron microscopy.

The NVCM memory has a programming interface similar to a 25-series SPI serial Flash PROM. Consequently, it can be programmed using standard device programmers before or after circuit board assembly or programmed in-system from a microprocessor or other intelligent controller.

Configuration Control Signals

The iCE65P configuration process is self-timed and controlled by a few internal signals and device I/O pins, as described in Table 29.

Table 29: **iCE65P Configuration Control Signals**

Signal Name	Direction	Description
POR	Internal control	Internal Power-On Reset (POR) circuit.
OSC	Internal control	Internal configuration oscillator.
CRESET_B	Input	Configuration Reset input. Active-Low. No internal pull-up resistor.
CDONE	Open-drain Output	Configuration Done output. Permanent, weak pull-up resistor to VCCIO_2.

The Power-On Reset circuit, POR, automatically resets the iCE65P component to a known state during power-up (cold boot). The POR circuit monitors the relevant voltage supply inputs, as shown in Figure 25. Once all supplies exceed their minimum thresholds, the configuration controller can start the configuration process.

The configuration controller begins configuring the iCE65P device, clocked by the Internal Oscillator, OSC. The OSC oscillator continues controlling configuration unless the iCE65P device is configured using the SPI Peripheral Configuration Interface.

Figure 24: **iCE65P Configuration Control Pins**

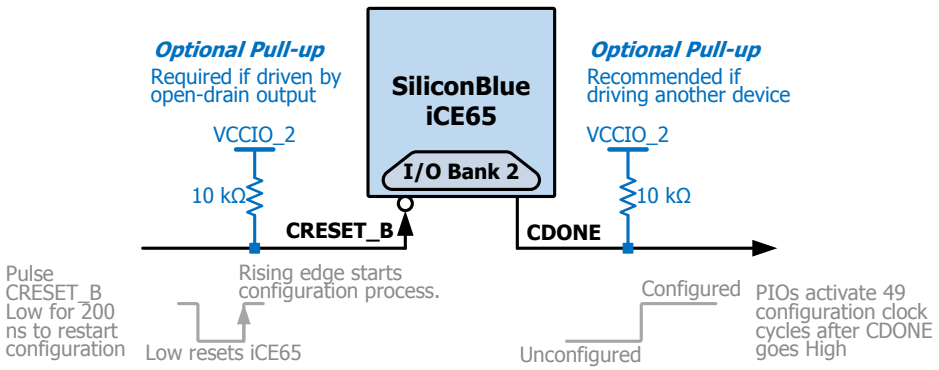


Figure 24 shows the two iCE65P configuration control pins, CRESET_B and CDONE. Table 30 lists the Ball numbers for the configuration control pins by package. When driven Low for at least 200 ns, the dedicated Configuration Reset input, CRESET_B, resets the iCE65P device. When CRESET_B returns High, the iCE65P FPGA restarts the configuration process from its power-on conditions (Cold Boot). The CRESET_B pin is a pure input with no internal pull-up resistor. If driven by open-drain driver or un-driven, then connect the CRESET_B pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Table 33: **SPI Interface Ball Numbers by Package**

SPI Interface	Package Code		
	CB121	**CB196**	**CB284**
SPI_VCC	J10	L11	R15
PIOS/SPI_SO	J8	M11	T15
PIOS/SPI_SI	K8	P11	V15
PIOS/SPI_SS_B	J9	P13	V17
PIOS/SPI_SCK	K9	P12	V16

SPI PROM Requirements

The iCE65P mobileFPGA SPI Flash configuration interface supports a variety of SPI Flash memory vendors and product families. However, SiliconBlue Technologies does not specifically test, qualify, or otherwise endorse any specific SPI Flash vendor or product family. The iCE65P SPI interface supports SPI PROMs that they meet the following requirements.

- The PROM must operate at 3.3V or 2.5V in order to trigger the iCE65P FPGA's power-on reset circuit.
- The PROM must support the 0x0B Fast Read command, using a 24-bit start address and has 8 dummy bits before the PROM provides first data (see Figure 28: SPI Fast Read Command).
- The PROM must have enough bits to program the iCE65P device (see Table 34: Smallest SPI PROM Size (bits), by Device, by Number of Images).
- The PROM must support data operations at the upper frequency range for the selected iCE65P internal oscillator frequency (see Table 61). The oscillator frequency is selectable when creating the FPGA bitstream image.
- For lowest possible power consumption after configuration, the PROM should also support the 0xB9 Deep Power Down command and the 0xAB Release from Deep Power-down Command (see Figure 27 and Figure 29). The low-power mode is optional.
- The PROM must be ready to accept commands 10 µs after meeting its power-on conditions. In the PROM data sheet, this may be specified as t_{VSL} or t_{VCSL}. It is possible to use slower PROMs by holding the CRESET_B input Low until the PROM is ready, then releasing CRESET_B, either under program control or using an external power-on reset circuit.

The SiliconBlue iCEman65 development board and associated programming software uses an ST Micro/Numonyx M25Pxx SPI serial Flash PROM.

SPI PROM Size Requirements

Table 34 lists the minimum SPI PROM size required to configure an iCE65P device. Larger PROM sizes are allowed, but not required unless the end application uses the additional space. SPI serial PROM sizes are specified in bits. For each device size, the table shows the required minimum PROM size for "Logic Only" (no BRAM initialization) and "Logic + RAM4K" (RAM4K blocks pre-initialized). Furthermore, the table shows the PROM size for varying numbers of configuration images. Most applications will use a single image. Applications that use the Cold Boot or Warm Boot features may use more than one image.

Table 34: **Smallest SPI PROM Size (bits), by Device, by Number of Images**

Device	1 Image		2 Images		3 Images		4 Images	
	Logic Only	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**
iCE65P04	512K	1M	1M	2M	2M	2M	2M	4M

Enabling SPI Configuration Interface

The optional 10 kΩ pull-down resistor on the SPI_SS_B signal ensures that the iCE65P FPGA powers up in the SPI peripheral mode. Optionally, the application processor drives the SPI_SS_B pin Low when CRESET_B is released, forcing the iCE65P FPGA into SPI peripheral mode.

SPI Peripheral Configuration Process

Figure 32 illustrates the interface timing for the SPI peripheral mode and Figure 33 outlines the resulting configuration process. The actual timing specifications appear in Table 64. The application processor (AP) begins by driving the iCE65P CRESET_B pin Low, resetting the iCE65P FPGA. Similarly, the AP holds the iCE65's SPI_SS_B pin Low. The AP must hold the CRESET_B pin Low for at least 200 ns. Ultimately, the AP either releases the CRESET_B pin and allows it to float High via the 10 kΩ pull-up resistor to VCCIO_2 or drives CRESET_B High. The iCE65P FPGA enters SPI peripheral mode when the CRESET_B pin returns High while the SPI_SS_B pin is Low,

After driving CRESET_B High or allowing it to float High, the AP must wait a minimum of 300 µs, allowing the iCE65P FPGA to clear its internal configuration memory.

After waiting for the configuration memory to clear, the AP sends the configuration image generated by the iCEcube development system. An SPI peripheral mode configuration image must not use the ColdBoot or WarmBoot options. Send the entire configuration image, without interruption, serially to the iCE65's SPI_SI input on the falling edge of the SPI_SCK clock input. Once the AP sends the `0x7EAA997E` synchronization pattern, the generated SPI_SCK clock frequency must be within the specified 1 MHz to 25 MHz range (40 ns to 1 µs clock period) while sending the configuration image. Send each byte of the configuration image with most-significant bit (msb) first. The AP sends data to the iCE65P FPGA on the falling edge of the SPI_SCK clock. The iCE65P FPGA internally captures each incoming SPI_SI data bit on the rising edge of the SPI_SCK clock. The iCE65's SPI_SO output pin is not used during SPI peripheral mode but must connect to the AP if the AP also programs the iCE65's Nonvolatile Configuration Memory (NVCM).

The iCE65P configuration image must be sent as one contiguous stream without interruption.

The SPI_SCK clock period must be between 40 ns to 1 µs (1 MHz to 25 MHz).

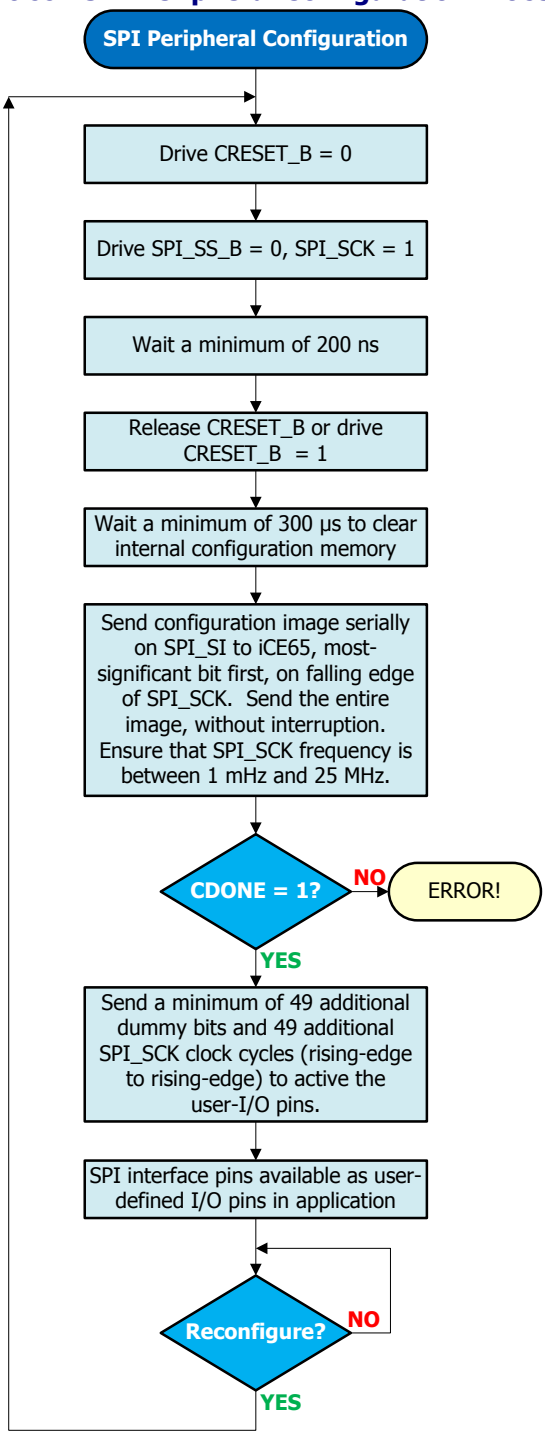
After sending the entire image, the iCE65P FPGA releases the CDONE output allowing it to float High via the 10 kΩ pull-up resistor to AP_VCC. If the CDONE pin remains Low, then an error occurred during configuration and the AP should handle the error accordingly for the application.

After the CDONE output pin goes High, send at least 49 additional dummy bits, effectively 49 additional SPI_SCK clock cycles measured from rising-edge to rising-edge.

After the additional SPI_CLK cycles, the SPI interface pins then become available to the user application loaded in FPGA.

To reconfigure the iCE65P FPGA or to load a different configuration image, merely restart the configuration process by pulsing CRESET_B Low or power-cycling the FPGA.

Figure 33: **SPI Peripheral Configuration Process**



Voltage Compatibility

As shown in Figure 26, there are potentially three different supply voltages involved in the SPI Peripheral interface, described in Table 37.

Table 37: **SPI Peripheral Mode Supply Voltages**

Supply Voltage	Description
AP_VCCIO	I/O supply to the Application Processor (AP)
VCC_SPI	Voltage supply for the iCE65P SPI interface.
VCCIO_2	Supply voltage for the iCE65P I/O Bank 2.

Supported JTAG Commands

The JTAG interface supports the IEEE 1149.1 mandatory instructions, including EXTEST, SAMPLE/PRELOAD, and BYPASS.

Package and Pinout Information

Maximum User I/O Pins by Package and by I/O Bank

Table 41 lists the maximum number of user-programmable I/O pins by package, with additional detail showing user I/O pins by I/O bank. In some cases, a smaller iCE65P device is packaged in a larger package with unconnected (N.C.) pins or balls, resulting in fewer overall I/O pins. See Table 2 and Table 42 for device-specific I/O counts by package.

Table 41: **User I/O by Package, by I/O Bank**

	Package Code		
	CB121	**CB196**	**CB284**
Package Leads	121	196	284
Package Area (mm)	6 x 6	8 x 8	12 x 12
Ball Array (balls)	11 x 11	14 x 14	22 x 22
Ball/Lead Pitch (mm)	0.5	0.5	0.5
Maximum user I/O, all I/O banks	**95**	**148**	**220**
PIO Pins in Bank 0	25	37	60
PIO Pins in Bank 1	21	38	55
PIO Pins in Bank 2	23	33	51
PIO Pins in Bank 3	26	36	50
PIO Pins in SPI Interface	4	4	4

Maximum User I/O by Device and Package

Table 42 lists the maximum available user I/O by device and by and package type. Not all devices are available in all packages. Similarly, smaller iCE65P devices may have unconnected balls in some packages. Devices sharing a common package have similar footprints.

Table 42: **Maximum User I/O by Device and Package**

Package	Device
	iCE65P04
CB121	95
CB196	148
CB284	174

Signal Name	Direction	I/O Bank	Pull-up during Config	Description
PLLVCC	Supply	PLL	N/A	Analog voltage supply for Phase Lock Loop (PLL). If unused, tie to ground.
TDI	Input	1	No	JTAG Test Data Input. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TMS	Input	1	No	JTAG Test Mode Select. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TCK	Input	1	No	JTAG Test Clock. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TDO	Output	1	No	JTAG Test Data Output.
TRST_B	Input	1	No	JTAG Test Reset, active Low. Keep Low during normal operation; High for JTAG operation.
VCC	Supply	All	N/A	Internal core voltage supply. All must be connected.
VCCIO_0	Supply	0	N/A	Voltage supply to I/O Bank 0. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
VCCIO_1	Supply	1	N/A	Voltage supply to I/O Bank 1. All such pins or balls on the package must be connected. Required to guarantee a valid input voltage on TRST_B JTAG pin.
VCCIO_2	Supply	2	N/A	Voltage supply to I/O Bank 2. All such pins or balls on the package must be connected. Required input to the Power-On Reset (POR) circuit.
VCCIO_3	Supply	3	N/A	Voltage supply to I/O Bank 3. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
SPI_VCC	Supply	SPI	N/A	SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM. Required input to the Power-On Reset (POR) circuit.
VPP_FAST	Supply	All	N/A	Direct programming voltage supply. If unused, leave floating or unconnected during normal operation.
VPP_2V5	Supply	All	N/A	Programming supply voltage. When the iCE65P device is active, VPP_2V5 must be in the valid range between 2.3 V to 3.47 V to release the Power-On Reset circuit, even if the application is not using the NVCM.
VREF	Voltage Reference	3	N/A	Input reference voltage in I/O Bank 3 for the SSTL I/O standard. This pin only appears on the CB284 package and for die-based products.

N/A = Not Applicable

CB121 Chip-Scale Ball-Grid Array

The CB121 package is a chip-scale, fully-populated, ball-grid array with 0.5 mm ball pitch.

Footprint Diagram

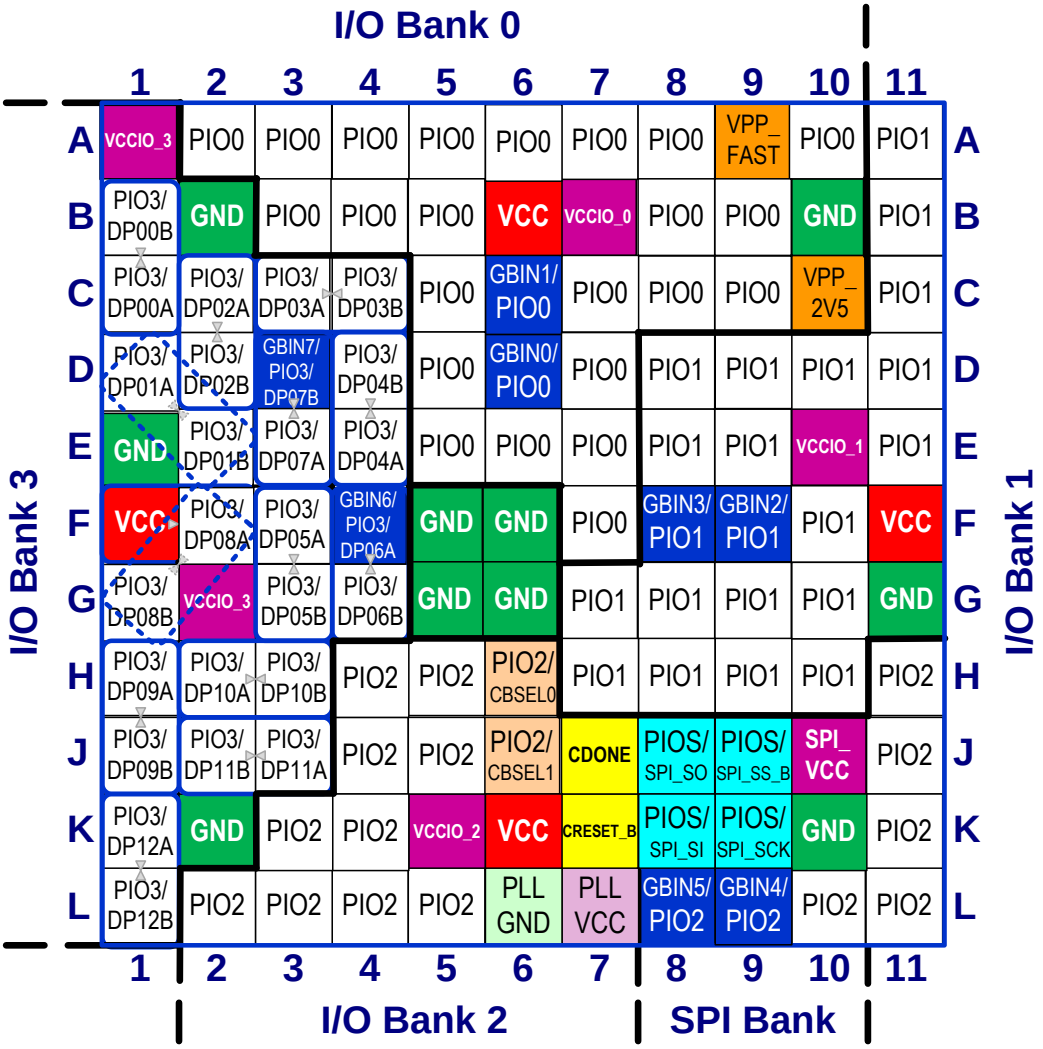
Figure 35 shows the iCE65P04 chip-scale BGA footprint for the 6 x 6 mm CB121 package.

Figure 34 shows the conventions used in the diagram.

Also see Table 46 for a complete, detailed pinout for the 121-ball chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 35: **iCE65P04 CB121 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 46 provides a detailed pinout table for the iCE65P04 in the CB121 chip-scale BGA package. Pins are generally arranged by I/O bank, then by ball function.

Table 46: **iCE65P04 CB121 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	D6	GBIN	0
GBIN1/PIO0	C6	GBIN	0
PIO0	A2	PIO	0
PIO0	A3	PIO	0

Ball Function	Ball Number	Pin Type	Bank
PIO0	A4	PIO	0
PIO0	A5	PIO	0
PIO0	A6	PIO	0
PIO0	A7	PIO	0
PIO0	A8	PIO	0
PIO0	A10	PIO	0
PIO0	B3	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B8	PIO	0
PIO0	B9	PIO	0
PIO0	C5	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	D5	PIO	0
PIO0	D7	PIO	0
PIO0	E5	PIO	0
PIO0	E6	PIO	0
PIO0	E7	PIO	0
PIO0	F7	PIO	0
VCCIO_0	B7	VCCIO	0
GBIN2/PIO1	F9	GBIN	1
GBIN3/PIO1	F8	GBIN	1
PIO1	A11	PIO	1
PIO1	B11	PIO	1
PIO1	C11	PIO	1
PIO1	D8	PIO	1
PIO1	D9	PIO	1
PIO1	D10	PIO	1
PIO1	D11	PIO	1
PIO1	E8	PIO	1
PIO1	E9	PIO	1
PIO1	E11	PIO	1
PIO1	F10	PIO	1
PIO1	G7	PIO	1
PIO1	G8	PIO	1
PIO1	G9	PIO	1
PIO1	G10	PIO	1
PIO1	H7	PIO	1
PIO1	H8	PIO	1
PIO1	H9	PIO	1
PIO1	H10	PIO	1
VCCIO_1	E10	VCCIO	1
CDONE	J7	CONFIG	2
CRESET_B	K7	CONFIG	2
GBIN4/PIO2	L9	GBIN	2
GBIN5/PIO2	L8	GBIN	2
PIO2	H4	PIO	2
PIO2	H5	PIO	2
PIO2	H11	PIO	2

Ball Function	Ball Number	Pin Type	Bank
GND	B2	GND	GND
GND	B10	GND	GND
GND	E1	GND	GND
GND	F5	GND	GND
GND	F6	GND	GND
GND	G5	GND	GND
GND	G6	GND	GND
GND	G11	GND	GND
GND	K2	GND	GND
GND	K10	GND	GND
VCC	B6	VCC	VCC
VCC	F1	VCC	VCC
VCC	F11	VCC	VCC
VCC	K6	VCC	VCC
VPP_2V5	C10	VPP	VPP
VPP_FAST	A9	VPP	VPP

CB284 Chip-Scale Ball-Grid Array

The CB284 package, partially-populated 0.5 mm pitch, ball grid array simplifies PCB layout with empty ball rings.

Footprint Diagram

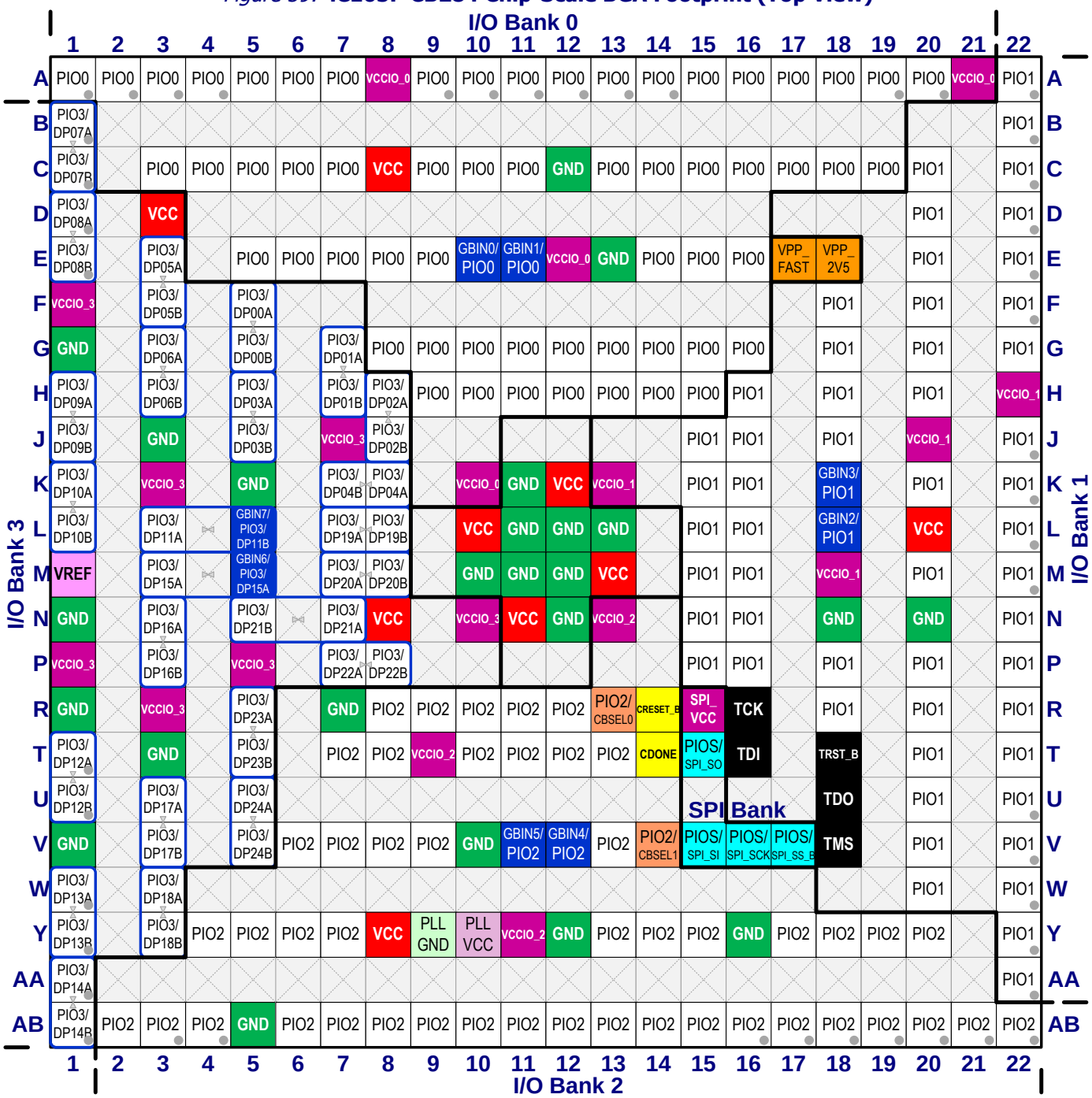
Figure 39 shows the CB284 chip-scale BGA footprint.

Figure 34 shows the conventions used in the diagram.

Also see Table 48 for a complete, detailed pinout for the 284-ball chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 39: **iCE65P CB284 Chip-Scale BGA Footprint (Top View)**



Ball Function	Ball Number	Pin Type by Device		Bank
		iCE65P04	iCE65P08	
PIOS/SPI_SO	T15	SPI	SPI	SPI
PIOS/SPI_SI	V15	SPI	SPI	SPI
PIOS/SPI_SCK	V16	SPI	SPI	SPI
PIOS/SPI_SS_B	V17	SPI	SPI	SPI
SPI_VCC	R15	SPI	SPI	SPI
PLLGND	Y9	PLLGND	PLLGND	PLL
PLLVCC	Y10	PLLVCC	PLLVCC	PLL
GND	C12	GND	GND	GND
GND	E13	GND	GND	GND
GND	J3	GND	GND	GND
GND	K5	GND	GND	GND
GND	K11	GND	GND	GND
GND	L11	GND	GND	GND
GND	L12	GND	GND	GND
GND	L13	GND	GND	GND
GND	M10	GND	GND	GND
GND	M11	GND	GND	GND
GND	M12	GND	GND	GND
GND	N1	GND	GND	GND
GND	N12	GND	GND	GND
GND	N18	GND	GND	GND
GND	N20	GND	GND	GND
GND	R7	GND	GND	GND
GND	T3	GND	GND	GND
GND	V1	GND	GND	GND
GND	V10	GND	GND	GND
GND	Y12	GND	GND	GND
GND	Y16	GND	GND	GND
GND	AB5	GND	GND	GND
GND	G1	GND	GND	GND
GND	R1	GND	GND	GND
VCC	C8	VCC	VCC	VCC
VCC	D3	VCC	VCC	VCC
VCC	K12	VCC	VCC	VCC
VCC	L10	VCC	VCC	VCC
VCC	L20	VCC	VCC	VCC
VCC	M13	VCC	VCC	VCC
VCC	N8	VCC	VCC	VCC
VCC	N11	VCC	VCC	VCC
VCC	Y8	VCC	VCC	VCC
VPP_2V5	E18	VPP	VPP	VPP
VPP_FAST	E17	VPP	VPP	VPP

Die Cross Reference

The tables in this section list all the pads on a specific die type and provide a cross reference on how a specific pad connects to a ball or pin in each of the available package offerings. Similarly, the tables provide the pad coordinates for the die-based version of the product (iCE DiCE). These tables also provide a way to prototype with one package option and then later move to a different package or die.

As described in "Input and Output Register Control per PIO Pair" on page 14, PIO pairs share register control inputs. Similarly, as described in "Differential Inputs and Outputs" on page 11, a PIO pair can form a differential input or output. PIO pairs in I/O Bank 3 are optionally differential inputs or differential outputs. PIO pairs in all other I/O Banks are optionally differential outputs. In the tables, differential pairs are surrounded by a heavy blue box.

iCE65P04

Table 49 lists all the pads on the iCE65P04 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65P04 DiePlus product, please contact your SiliconBlue sales representative..

Table 49: **iCE65P04 Die Cross Reference**

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_00/DP00A	C1	F5	1	129.40	2,687.75
PIO3_01/DP00B	B1	G5	2	231.40	2,642.74
PIO3_02/DP01A	D3	G7	3	129.40	2,597.75
PIO3_03/DP01B	C3	H7	4	231.40	2,552.74
GND	F1	K5	5	129.40	2,507.75
GND	—	—	6	231.40	2,462.74
VCCIO_3	E3	J7	7	129.40	2,417.75
VCCIO_3	—	—	8	231.40	2,372.74
PIO3_04/DP02A	D1	H8	9	129.40	2,327.75
PIO3_05/DP02B	D2	J8	10	231.40	2,292.74
PIO3_06/DP03A	E1	H5	11	129.40	2,257.75
PIO3_07/DP03B	E2	J5	12	231.40	2,222.74
VCC	H9	D3	13	129.40	2,187.75
PIO3_08/DP04A	D4	K8	14	231.40	2,152.74
PIO3_09/DP04B	E4	K7	15	129.40	2,117.75
PIO3_10/DP05A	F3	E3	16	231.40	2,082.74
PIO3_11/DP05B	F4	F3	17	129.40	2,047.75
GND	A9	M10	18	231.40	2,012.74
PIO3_12/DP06A	F5	G3	19	129.40	1,977.75
PIO3_13/DP06B	E5	H3	20	231.40	1,942.74
GND	A9	J3	21	129.40	1,907.75
GND	—	—	22	231.40	1,872.74
PIO3_14/DP07A	—	H1	23	129.40	1,837.75
PIO3_15/DP07B	—	J1	24	231.40	1,802.74
VCCIO_3	K1	K3	25	129.40	1,767.75
VCC	G6	L10	26	231.40	1,732.74
PIO3_16/DP08A	—	K1	27	129.40	1,697.75
PIO3_17/DP08B	—	L1	28	231.40	1,662.74
PIO3_18/DP09A	G2	L3	29	129.40	1,627.75
GBIN7/PIO3_19/DP09B	G1	L5	30	231.40	1,592.74
VCCIO_3	J6	N10	31	129.40	1,557.75

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
VREF	N/A	M1	32	231.40	1,522.74
GND	A9	N1	33	129.40	1,487.75
GBIN6/PIO3_20/DP10A	H1	M5	34	231.40	1,452.74
PIO3_21/DP10B	H2	M3	35	129.40	1,417.75
GND	A9	M11	36	231.40	1,382.74
PIO3_22/DP11A	G3	N3	37	129.40	1,347.75
PIO3_23/DP11B	G4	P3	38	231.40	1,312.74
VCCIO_3	K1	R3	39	129.40	1,277.75
VCCIO_3	—	—	40	231.40	1,242.74
GND	A9	T3	41	129.40	1,207.75
GND	—	—	42	231.40	1,172.74
PIO3_24/DP12A	J1	U3	43	129.40	1,137.75
PIO3_25/DP12B	J2	V3	44	231.40	1,102.74
GND	A9	V1	45	129.40	1,067.75
PIO3_26/DP13A	H4	W3	46	231.40	1,032.74
PIO3_27/DP13B	H3	Y3	47	129.40	997.75
PIO3_28/DP14A	K2	L7	48	231.40	962.74
PIO3_29/DP14B	J3	L8	49	129.40	927.75
PIO3_30/DP15A	H5	M7	50	231.40	892.74
PIO3_31/DP15B	G5	M8	51	129.40	857.75
VCC	F2	N8	52	231.40	822.74
PIO3_32/DP16A	L1	N7	53	129.40	787.75
PIO3_33/DP16B	L2	N5	54	231.40	752.74
VCCIO_3	K1	P5	55	129.40	717.75
VCCIO_3	—	—	56	231.40	682.74
GND	L3	R7	57	129.40	637.75
GND	—	—	58	231.40	592.74
PIO3_34/DP17A	M1	P7	59	129.40	547.75
PIO3_35/DP17B	M2	P8	60	231.40	502.74
PIO3_36/DP18A	K3	R5	61	129.40	457.75
PIO3_37/DP18B	K4	T5	62	231.40	412.74
PIO3_38/DP19A	N1	U5	63	129.40	367.75
PIO3_39/DP19B	N2	V5	64	231.40	322.74
PIO2_00	—	AB2	65	440.00	139.20
PIO2_01	L4	V6	66	490.00	37.20
PIO2_02	M3	T7	67	540.00	139.20
GND	C2	AB5	68	590.00	37.20
PIO2_03	P1	R8	69	640.00	139.20
PIO2_04	N3	V7	70	690.00	37.20
PIO2_05	P2	T8	71	740.00	139.20
PIO2_06	L5	R9	72	790.00	37.20
PIO2_07	M4	V8	73	825.00	139.20
PIO2_08	P3	R10	74	860.00	37.20
VCCIO_2	M5	T9	75	895.00	139.20
PIO2_09	K5	V9	76	930.00	37.20

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO0_17	C9	C18	217	2,087.00	2,962.80
PIO0_18	B9	C17	218	2,052.00	2,860.80
PIO0_19	D8	C16	219	2,017.00	2,962.80
PIO0_20	C8	C15	220	1,982.00	2,860.80
PIO0_21	E8	C14	221	1,947.00	2,962.80
PIO0_22	B8	C13	222	1,912.00	2,860.80
GBIN1/PIO0_23	E7	E11	223	1,877.00	2,962.80
GND	B12	C12	224	1,842.00	2,860.80
GND	—	—	225	1,807.00	2,962.80
GBIN0/PIO0_24	A7	E10	226	1,772.00	2,860.80
PIO0_25	D7	C11	227	1,737.00	2,962.80
PIO0_26	C7	C10	228	1,702.00	2,860.80
PIO0_27	E6	C9	229	1,667.00	2,962.80
VCC	B7	C8	230	1,632.00	2,860.80
VCC	—	—	231	1,597.00	2,962.80
PIO0_28	A6	C7	232	1,562.00	2,860.80
PIO0_29	B6	C6	233	1,527.00	2,962.80
PIO0_30	A5	C5	234	1,492.00	2,860.80
PIO0_31	D6	C4	235	1,457.00	2,962.80
GND	F7	K11	236	1,422.00	2,860.80
GND	—	—	237	1,387.00	2,962.80
PIO0_32	—	C3	238	1,352.00	2,860.80
PIO0_33	—	A7	239	1,317.00	2,962.80
PIO0_34	—	A6	240	1,282.00	2,860.80
PIO0_35	—	A5	241	1,247.00	2,962.80
PIO0_36	C6	G11	242	1,212.00	2,860.80
VCCIO_0	F6	K10	243	1,177.00	2,962.80
VCCIO_0	F6	K10	244	1,142.00	2,860.80
PIO0_37	C5	H11	245	1,107.00	2,962.80
PIO0_38	B5	G10	246	1,072.00	2,860.80
PIO0_39	A4	E9	247	1,037.00	2,962.80
PIO0_40	B4	H10	248	1,002.00	2,860.80
PIO0_41	D5	G9	249	967.00	2,962.80
PIO0_42	A3	E8	250	917.00	2,860.80
GND	G7	L11	251	867.00	2,962.80
PIO0_43	B3	H9	252	817.00	2,860.80
PIO0_44	C4	G8	253	767.00	2,962.80
PIO0_45	A2	E7	254	717.00	2,860.80
PIO0_46	A1	E6	255	667.00	2,962.80
PIO0_47	B2	E5	256	617.00	2,860.80

Electrical Characteristics

All parameter limits are specified under worst-case supply voltage, junction temperature, and processing conditions.

Absolute Maximum Ratings

Stresses beyond those listed under Table 50 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 50: **Absolute Maximum Ratings**

Symbol	Description	Minimum	Maximum	Units
VCC	Core supply Voltage	–0.5	1.42	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply			V
VPP_FAST	Optional fast NVCM programming supply			V
VCCIO_0 **VCCIO_1** **VCCIO_2** **SPI_VCC**	I/O bank supply voltage (I/O Banks 0, 1, and 2 plus SPI interface)	–0.5	4.00	V
VCCIO_3	I/O Bank 3 supply voltage	–0.5	3.60	V
VIN_0 **VIN_1** **VIN_2** **VIN_SPI**	Voltage applied to PIO pin within a specific I/O bank (I/O Banks 0, 1, and 2 plus SPI interface)	–1.0	5.5	V
VIN_3 **VIN_VREF**	Voltage applied to PIO pin within I/O Bank 3	–0.5	3.60	V
VCCPLL	Analog voltage supply to the Phase Locked Loop (PLL)	–0.5	3.60	V
$\mathbf{I_{OUT}}$	DC output current per pin	—	20	mA
$\mathbf{T_J}$	Junction temperature	–55	125	°C
$\mathbf{T_{STG}}$	Storage temperature, no bias	–65	150	°C

Recommended Operating Conditions

Table 51: **Recommended Operating Conditions**

Symbol	Description		Minimum	Nominal	Maximum	Units
VCC	Core supply voltage	High Performance, low-power	1.14	1.20	1.26	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply	Release from Power-on Reset	1.30	—	3.47	V
		Configure from NVCM	2.30	—	3.47	V
		NVCM programming	2.30	—	3.00	V
VPP_FAST	Optional fast NVCM programming supply		Leave unconnected in application			
SPI_VCC	SPI interface supply voltage		1.71	—	3.47	V
VCCIO_0 VCCIO_1 VCCIO_2 VCCIO_3 SPI_VCC	I/O standards, all banks	**LVCMOS33**	2.70	3.30	3.47	V
		LVCMOS25, LVDS	2.38	2.50	2.63	V
		LVCMOS18, SubLVDS	1.71	1.80	1.89	V
		LVCMOS15	1.43	1.50	1.58	V
VCCIO_3	I/O standards only available in I/O Bank 3	**SSTL2**	2.38	2.50	2.63	V
		SSTL18	1.71	1.80	1.89	V
		MDDR	1.71	1.80	1.89	V
VCCPLL	Analog voltage supply to the Phase Locked Loop (PLL)		1.71	2.50	2.63	V
T_A	Ambient temperature	Commercial (C)	0	—	70	°C
		Industrial (I)	–40	—	85	°C
$\mathbf{T_{PROG}}$	NVCM programming temperature		10	25	30	°C

NOTE:

VPP_FAST is only used for fast production programming. Leave floating or unconnected in application. When the iCE65P device is active, VPP_2V5 must be connected to a valid voltage.

RAM4K Block

Table 59 provides timing information for the logic in a RAM4K block, which includes the paths shown in Figure 50.

Figure 50: **RAM4K Timing Circuit**

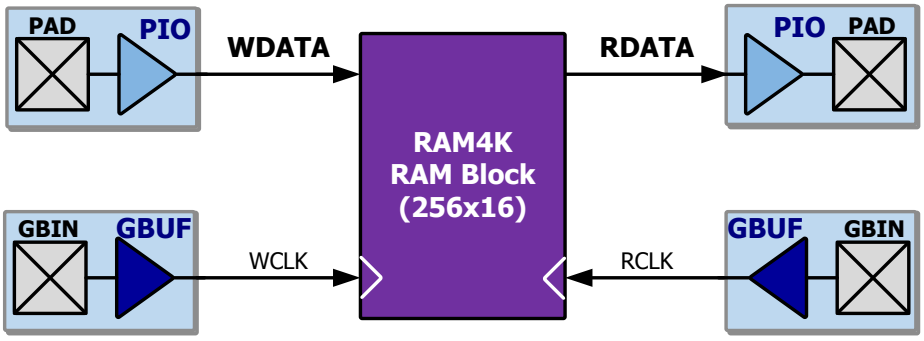


Table 59: **Typical RAM4K Block Timing**

Symbol	From	To	Description	Power/Speed Grade: –T Nominal VCC: 1.2 V Typ.	Units
Write Setup/Hold Time					
t_{SUWD}	PIO input	GBIN input	Minimum write data setup time on PIO inputs before active clock edge on GBIN input, include interconnect delay.	0.8	ns
t_{HDWD}	GBIN input	PIO input	Minimum write data hold time on PIO inputs after active clock edge on GBIN input, including interconnect delay.	0	ns
Read Clock-Output-Time					
t_{CKORD}	RCLK clock input	PIO output	Clock-to-output delay from RCLK input pin, through RAM4K RDATA output flip-flop to PIO output pad, including interconnect delay.	7.3	ns
t_{GBCKRM}	GBIN input	RCLK clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to the RCLK clock input.	2.6	ns
Write and Read Clock Characteristics					
t_{RMWCKH}	WCLK RCLK	WCLK RCLK	Write clock High time	0.54	ns
t_{RMWCKL}			Write clock Low time	0.63	ns
t_{RMWCYC}			Write clock cycle time	1.27	ns
F_{WMAX}			Sustained write clock frequency	256	MHz

Phase-Locked Loop (PLL) Block

Table 59 provides timing information for the Phase-Locked Loop (PLL) block shown in Figure 50.

Figure 51: **Phase-Locked Loop (PLL)**

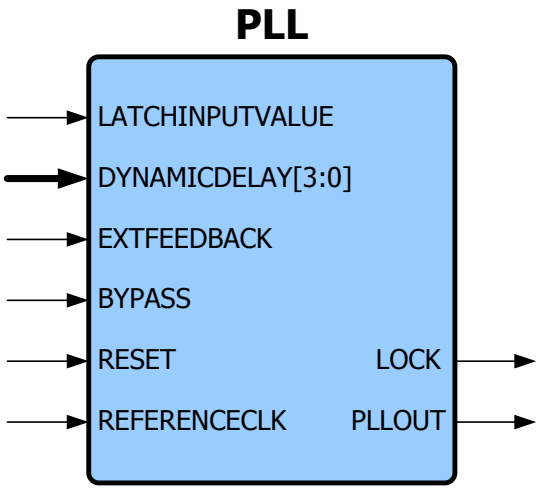


Table 60: **Phase-Locked Loop (PLL) Block Timing**

Symbol	From	To	Description	Power/Speed Grade: –T Nominal VCC: 1.2 V Min.	Typical	Max.	Units
Frequency Range							
F_{REF}			Input clock frequency range	10	—	133	MHz
F_{OUT}			Output clock frequency range (cannot exceed maximum frequency supported by global buffers)	10	—	533	MHz
Duty Cycle							
PLL_{IJ}			Input duty cycle	35	—	65	%
Tw_{HI}			Input clock high time	2.5	—	—	ns
Tw_{LOW}			Input clock low time	2.5	—	—	ns
PLL_{OJD}			Output duty cycle (divided frequency)	45	—	55	%
PLL_{OJM}			Output duty cycle (undivided frequency)	40	—	60	%
Fine Delay							
t_{FDTAP}			Fine delay adjustment, per tap		165		ps
PLL_{TAPS}			Fine delay adjustment settings	0	—	15	taps
PLL_{FDAM}			Maximum delay adjustment		2.5		ns
Jitter							
PLL_{IPJ}			Input clock period jitter	—	—	+/- 300	ps
PLL_{OPJ}			PLLOUT output period jitter	—	1% or ≤ 100	+/- 1.1% output period or ≥ 110	ps
Lock/Reset Time							
t_{LOCK}			PLL lock time after receive stable, monotonic REFERENCECLK input	—	—	50	µs
tw_{RST}			Minimum reset pulse width	20	—	—	ns

Notes:

1. Output jitter performance is affected by input jitter. A clean reference clock < 100ps jitter must be used to ensure best jitter performance.
2. The output jitter specification refers to the intrinsic jitter of the PLL.