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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	174
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	284-VFBGA, CSPBGA
Supplier Device Package	284-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65p04f-tcb284c

Packaging Options

iCE65P components are available in a variety of package options to support specific application requirements. The available options, including the number of available user-programmable I/O pins (PIOs), are listed in Table 2. Fully-tested Known-Good Die (KGD) DiePlus™ are available for die stacking and highly space-conscious applications. All iCE65P devices are provided exclusively in Pb-free, RoHS-compliant packages.

Table 2: **iCE65P Family Packaging Options, Maximum I/O per Package**

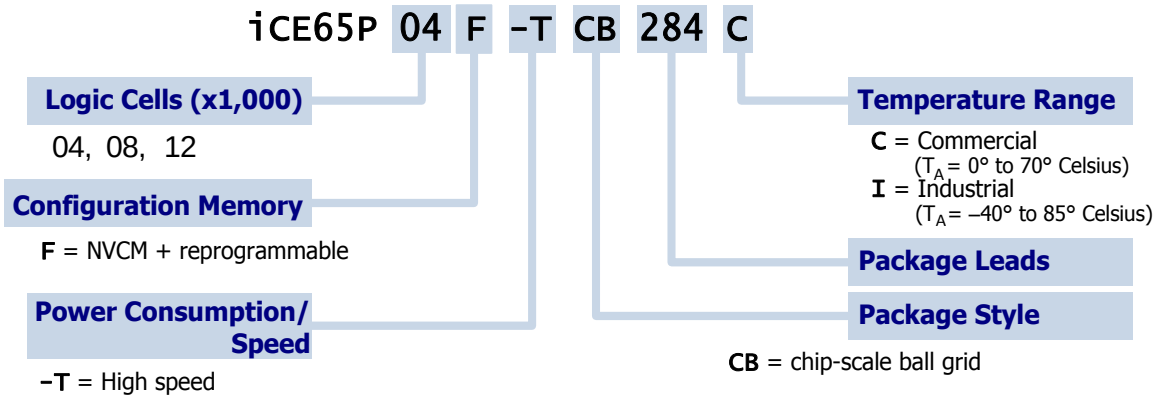
Package	Board Area (mm)	Package Code	Ball/Lead Pitch (mm)	iCE65P04	iCE65P08	iCE65P12
121-ball chip-scale BGA	6 x 6	CB121	0.5	95 *(13)*		
196-ball chip-scale BGA	8 x 8	CB196		148 *(18)*		
284-ball chip-scale BGA	12 x 12	CB284		174 *(20)*		
DiePlus known good die	See die data sheet	DI	—	174 *(20)*		

Feature-rich versions of the end application mount a larger iCE65P device on the circuit board. Low-end versions mount a smaller iCE65P device.

Ordering Information

Figure 2 describes the iCE65P ordering codes for all packaged components. See the separate DiePlus data sheets when ordering die-based products.

Figure 2: **iCE65P Ordering Codes (packaged, non-die components)**



iCE65P devices come standard in the higher speed "**-T**" version.

iCE65P devices are available in two operating temperature ranges, one for typical commercial applications, the other with an extended temperature range for industrial and telecommunications applications. The ordering code also specifies the device package option, as described further in Table 2.

Programmable Logic Block (PLB)

Generally, a logic design for an iCE65P component is created using a high-level hardware description language such as Verilog or VHDL. The SiliconBlue Technologies development software then synthesizes the high-level description into equivalent functions built using the programmable logic resources within each iCE65P device. Both sequential and combinational functions are constructed from an array of Programmable Logic Blocks (PLBs). Each PLB contains eight Logic Cells (LCs), as pictured in Figure 3, and share common control inputs, such as clocks, reset, and enable controls.

PLBs are connected to one another and other logic functions using the rich Programmable Interconnect resources.

Table 12 and Table 13 list the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pair. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

Table 12: **iCE65P04: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	No
GBUF1		Yes	Yes	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	Yes	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	Yes	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	Yes	Yes

Table 13: **iCE64L08: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	Yes
GBUF1		Yes	Yes	No
GBUF2		Yes	Yes	Yes
GBUF3		Yes	Yes	No
GBUF4		Yes	Yes	Yes
GBUF5		Yes	Yes	No
GBUF6		Yes	Yes	Yes
GBUF7		Yes	Yes	No

Global Buffer Inputs

The iCE65P component has eight specialized GBIN/PIO pins that are optionally direct inputs to the global buffers, offering the best overall clock characteristics. As shown in Figure 14, each GBIN/PIO pin is a full-featured I/O pin but also provides a direct connection to its associated global buffer. The direct connection to the global buffer bypasses the iCEgate input-blocking latch and other PIO input logic. These special PIO pins are allocated two to an I/O Bank, a total of eight. These pins are labeled GBIN0 through GBIN7, as shown in Figure 13 and the pin locations for each GBIN input appear in Table 14.

Attributes/Properties

Table 18 lists the attributes or properties associated with the PLL and the allowable settings for each attribute..

Table 18: **PLL Attributes and Settings**

Attribute/Property	Description	Setting	Description
FEEDBACK_PATH	Selects the feedback path to the PLL	SIMPLE	Feedback directly from VCO
		DELAY	Feedback from VCO through fine delay adjustment
		PHASE_AND_DELAY	Feedback from VCO through the fine delay adjustment and phase shifter; feedback is further divided by four
		EXTERNAL	Feedback from EXTFEEDBACK input
DELAY_ADJUSTMENT_MODE	Selects the control input for the fine delay adjustment. Delays the PLLOUT output nominally by (***n***+1) • 150 ps	FIXED	Delay controlled by FIXED_DELAY_ADJUSTMENT setting
		DYNAMIC	Delay controlled by current value of DYNAMIC_DELAY[3:0]
FIXED_DELAY_ADJUSTMENT	Sets the constant value for the fine delay adjustment when DELAY_ADJUSTMENT mode set to FIXED	0, 1, ..., 15	Delays the PLLOUT output by specified setting
PLL_OUT_PHASE	Controls the phase alignment of the PLLOUT output relative to the input reference clock; see Figure 18	NONE	Phase alignment disabled, no duty-cycle correction
		0deg	0° phase shift (no phase shift)
		90deg	90° phase shift (quarter cycle shift)
		180deg	180° phase shift (half-cycle shift)
		270deg	270° phase shift (three-quarter cycle shift)
DIVR	Divider value for the input clock	0, 1, ..., 15	These attributes control the PLL output frequency. See Equation 2 and Equation 3 and the Frequency Synthesis spreadsheet.
DIVF	Divider value for feedback	0, 1, ..., 63	
DIVQ	Divider value for the VCO output, generates PLLOUT	0, 1, ..., 5	
RANGE	Controls the PLL operating range	0, 1, ..., 7	
ENABLE_ICEGATE	Enables iCEgate to disable GBUF transitions	0	GBUF disabled
		1	GBUF enabled

Clock Input Requirements

For proper operation, the PLL requires ...

- A stable monotonic (single frequency) reference clock input.
- The reference clock input must be within the input clock frequency range, F_{REF}, specified in Table 60.
- The reference clock must have a duty cycle that meets the requirement specified in Table 60.
- The jitter on the reference input clock must not exceed the limits specified in Table 60.

PLL Output Requirements

The PLL output clock, PLLOUT requires the following restrictions.

- The PLLOUT output frequency must be within the limits specified in Table 60.
- The PLLOUT output is not valid or stable until the PLL's LOCK output remains High.

The data contents of the RAM4K block are optionally pre-loaded during iCE65P device configuration. If the RAM4K blocks are not pre-loaded during configuration, then the resulting configuration bitstream image is smaller. However, if an uninitialized RAM4K block is used in the application, then the application must initialize the RAM contents to guarantee the data value.

See Table 59 for detailed timing information.

Signals

Table 24 lists the signal names, direction, and function of each connection to the RAM4K block. See also Figure 20.

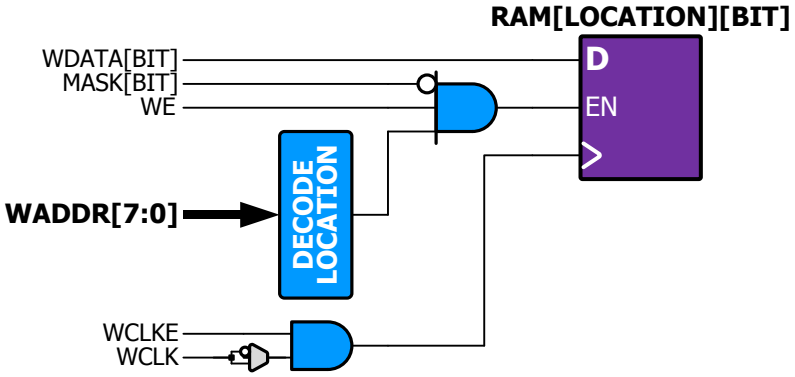
Table 24: **RAM4K Block RAM Signals**

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = Write bit; 1 = Don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

Write Operations

Figure 21 shows the logic involved in writing a data bit to a RAM location. Table 25 describes various write operations for a RAM4K block. By default, all RAM4K write operations are synchronized to the rising edge of WCLK although the clock is invertible as shown in Figure 21.

Figure 21: **RAM4K Bit Write Logic**



When the WCLKE signal is Low, the clock to the RAM4K block is disabled, keeping the RAM in its lowest power mode.

Table 25: **RAM4K Write Operations**

Operation	WDATA[15:0] Data	MASK[15:0] Mask Bit	WADDR[7:0] Address	WE Write Enable	WCLKE Clock Enable	WCLK Clock	RAM Location
Disabled	X	X	X	X	X	0	No change
Disabled					0	X	No change
Disabled	X	X	X	0	X	X	No change
Write Data	WDATA[i]	MASK[i] = 0	WADDR	1	1	↑	RAM[WADDR][i] = WDATA[i]
Masked Write	X	MASK[i] = 1	WADDR	1	1	↑	RAM[WADDR][i] = No change

To write data into the RAM4K block, perform the following operations.

- Supply a valid address on the WADDR[7:0] address input port
- Supply valid data on the WDATA[15:0] data input port
- To write or mask selected data bits, set the associated MASK input port accordingly. For example, write operations on data bit D[i] are controlled by the associated MASK[i] input.
  - MASK[i] = 0: Write operations are enabled for data line WDATA[i]
  - MASK[i] = 1: Mask write operations are disabled for data line WDATA[i]
- Enable the RAM4K write port (WE = 1)
- Enable the RAM4K write clock (WCLKE = 1)
- Apply a rising clock edge on WCLK (assuming that the clock is not inverted)

Read Operations

Figure 22 shows the logic involved in reading a location from RAM. Table 26 describes various read operations for a RAM4K block. By default, all RAM4K read operations are synchronized to the rising edge of RCLK although the clock is invertible as shown in Figure 22.

Figure 22: **RAM4K Read Logic**

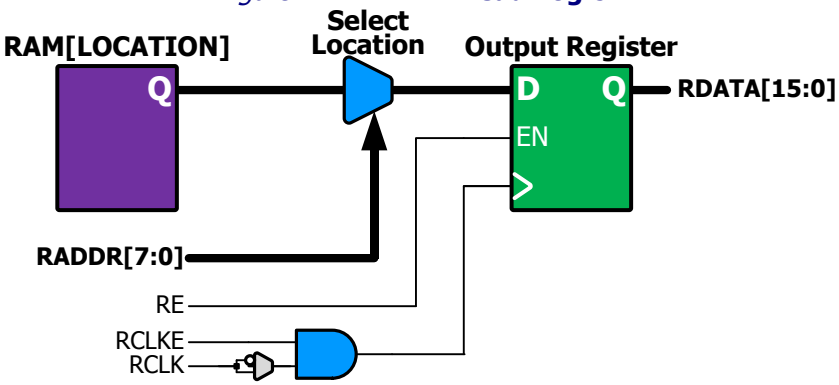
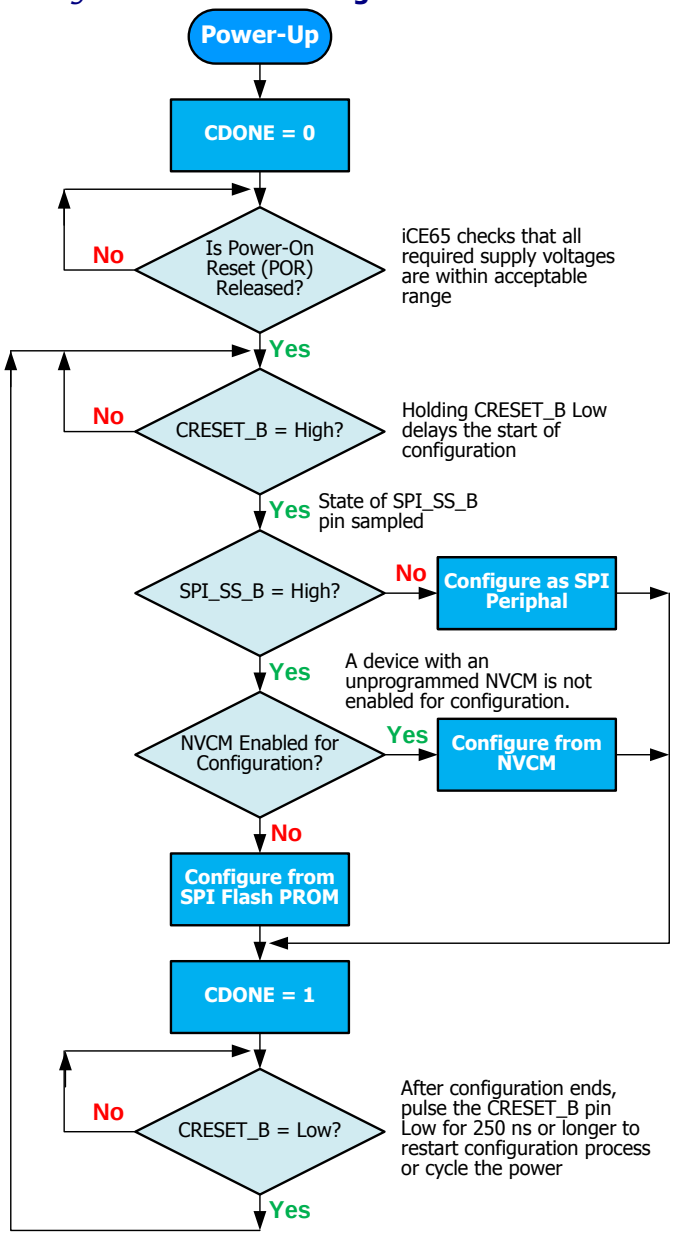


Figure 23: **Device Configuration Control Flow**



Configuration Image Size

Table 28 shows the number of memory bits required to configure an iCE65P device. Two values are provided for each device. The "Logic Only" value indicates the minimum configuration size, the number of bits required to configure only the logic fabric, leaving the RAM4K blocks uninitialized. The "Logic + RAM4K" column indicates the maximum configuration size, the number of bits to configure the logic fabric and to pre-initialize all the RAM4K blocks.

Table 28: **iCE65P Configuration Image Size (Kbits)**

Device	MINIMUM Logic Only (RAM4K not initialized)	MAXIUM Logic + RAM4K (RAM4K pre-initialized)
iCE65P04	453 Kbits	533 Kbits

Power-On Reset (POR)

The Power-on Reset (POR) circuit monitors specific voltage supply inputs and holds the device in reset until all the relevant supplies exceed the internal voltage thresholds. The SPI_VCC supply also has an additional time-out delay to allow an attached SPI serial PROM to power up properly. Table 31 shows the POR supply inputs. The Nonvolatile Configuration Memory (NVCM) requires that the VPP_2V5 supply be connected, even if the application does not use the NVCM.

Table 31: **Power-on Reset (POR) Voltage Resources**

Supply Rail	iCE65P Production Devices
VCC	Yes
SPI_VCC	Yes
VCCIO_1	No
VCCIO_2	Yes
VPP_2V5	Yes

CRESET_B Pin

The CRESET_B pin resets the iCE65P internal logic when Low.

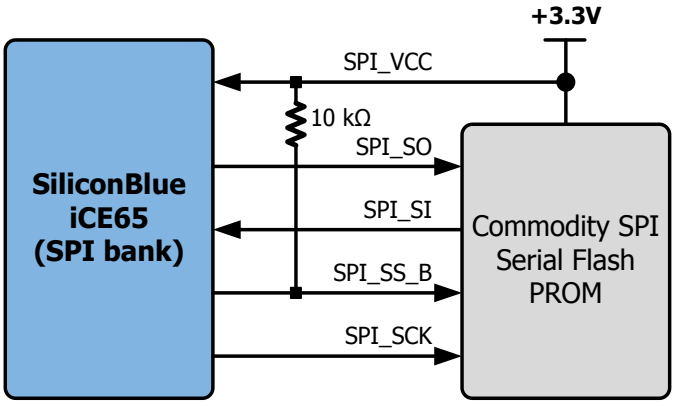
JTAG Interface

Specific command sequences also reset the iCE65P internal logic.

SPI Master Configuration Interface

All iCE65P devices, including those with NVCM, can be configured from an external, commodity SPI serial Flash PROM, as shown in Figure 26. The SPI configuration interface is essentially its own independent I/O bank, powered by the VCC_SPI supply input. Presently, most commercially-available SPI serial Flash PROMs require a 3.3V supply.

Figure 26: **iCE65P SPI Master Configuration Interface**



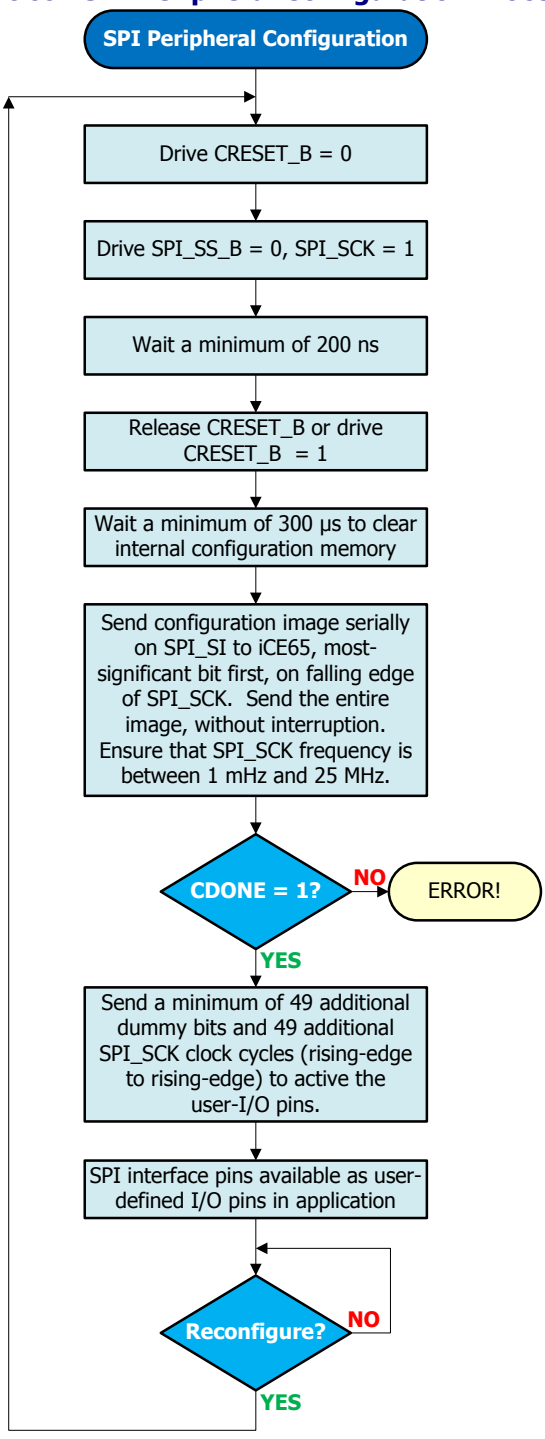
The SPI configuration interface is used primarily during development before mass production, where the configuration is then permanently programmed in the NVCM configuration memory. However, the SPI interface can also be the primary configuration interface allowing easy in-system upgrades and support for multiple configuration images.

The SPI control signals are defined in Table 32. Table 33 lists the SPI interface ball or pins numbers by package.

Table 32: **SPI Master Configuration Interface Pins (SPI_SS_B High before Configuration)**

Signal Name	Direction	Description
SPI_VCC	Supply	SPI Flash PROM voltage supply input.
SPI_SO	Output	SPI Serial Output from the iCE65P device.
SPI_SI	Input	SPI Serial Input to the iCE65P device, driven by the select SPI serial Flash PROM.
SPI_SS_B	Output	SPI Slave Select output from the iCE65P device. Active Low.
SPI_SCK	Output	SPI Slave Clock output from the iCE65P device.

Figure 33: **SPI Peripheral Configuration Process**



Voltage Compatibility

As shown in Figure 26, there are potentially three different supply voltages involved in the SPI Peripheral interface, described in Table 37.

Table 37: **SPI Peripheral Mode Supply Voltages**

Supply Voltage	Description
AP_VCCIO	I/O supply to the Application Processor (AP)
VCC_SPI	Voltage supply for the iCE65P SPI interface.
VCCIO_2	Supply voltage for the iCE65P I/O Bank 2.

Signal Name	Direction	I/O Bank	Pull-up during Config	Description
PLLVCC	Supply	PLL	N/A	Analog voltage supply for Phase Lock Loop (PLL). If unused, tie to ground.
TDI	Input	1	No	JTAG Test Data Input. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TMS	Input	1	No	JTAG Test Mode Select. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TCK	Input	1	No	JTAG Test Clock. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TDO	Output	1	No	JTAG Test Data Output.
TRST_B	Input	1	No	JTAG Test Reset, active Low. Keep Low during normal operation; High for JTAG operation.
VCC	Supply	All	N/A	Internal core voltage supply. All must be connected.
VCCIO_0	Supply	0	N/A	Voltage supply to I/O Bank 0. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
VCCIO_1	Supply	1	N/A	Voltage supply to I/O Bank 1. All such pins or balls on the package must be connected. Required to guarantee a valid input voltage on TRST_B JTAG pin.
VCCIO_2	Supply	2	N/A	Voltage supply to I/O Bank 2. All such pins or balls on the package must be connected. Required input to the Power-On Reset (POR) circuit.
VCCIO_3	Supply	3	N/A	Voltage supply to I/O Bank 3. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
SPI_VCC	Supply	SPI	N/A	SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM. Required input to the Power-On Reset (POR) circuit.
VPP_FAST	Supply	All	N/A	Direct programming voltage supply. If unused, leave floating or unconnected during normal operation.
VPP_2V5	Supply	All	N/A	Programming supply voltage. When the iCE65P device is active, VPP_2V5 must be in the valid range between 2.3 V to 3.47 V to release the Power-On Reset circuit, even if the application is not using the NVCM.
VREF	Voltage Reference	3	N/A	Input reference voltage in I/O Bank 3 for the SSTL I/O standard. This pin only appears on the CB284 package and for die-based products.

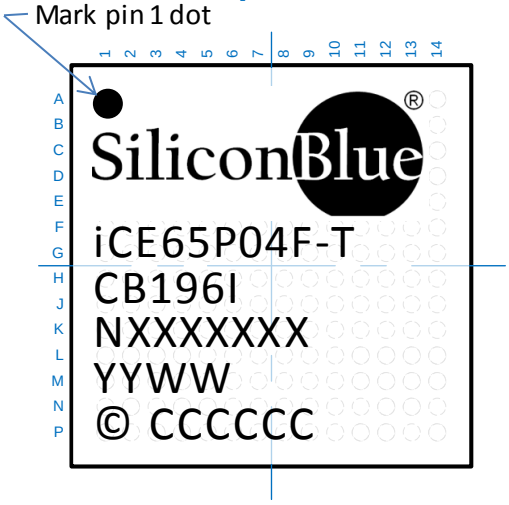
N/A = Not Applicable

Ball Function	Ball Number	Pin Type	Bank
PIO2	J4	PIO	2
PIO2	J5	PIO	2
PIO2	J11	PIO	2
PIO2	K3	PIO	2
PIO2	K4	PIO	2
PIO2	K11	PIO	2
PIO2	L2	PIO	2
PIO2	L3	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L10	PIO	2
PIO2	L11	PIO	2
PIO2/CBSEL0	H6	PIO	2
PIO2/CBSEL1	J6	PIO	2
VCCIO_2	K5	VCCIO	2
PIO3/DP00A	C1	DPIO	3
PIO3/DP00B	B1	DPIO	3
PIO3/DP01A	D1	DPIO	3
PIO3/DP01B	E2	DPIO	3
PIO3/DP02A	C2	DPIO	3
PIO3/DP02B	D2	DPIO	3
PIO3/DP03A	C3	DPIO	3
PIO3/DP03B	C4	DPIO	3
PIO3/DP04A	E4	DPIO	3
PIO3/DP04B	D4	DPIO	3
PIO3/DP05A	F3	DPIO	3
PIO3/DP05B	G3	DPIO	3
PIO3/DP06B	G4	DPIO	3
GBIN6/PIO3/DP06A	F4	GBIN	3
GBIN7/PIO3/DP07B	D3	GBIN	3
PIO3/DP07A	E3	DPIO	3
PIO3/DP08A	F2	DPIO	3
PIO3/DP08B	G1	DPIO	3
PIO3/DP09A	H1	DPIO	3
PIO3/DP09B	J1	DPIO	3
PIO3/DP10A	H2	DPIO	3
PIO3/DP10B	H3	DPIO	3
PIO3/DP11A	J3	DPIO	3
PIO3/DP11B	J2	DPIO	3
PIO3/DP12A	K1	DPIO	3
PIO3/DP12B	L1	DPIO	3
VCCIO_3	A1	VCCIO	3
VCCIO_3	G2	VCCIO	3
PIOS/SPI_SO	J8	SPI	SPI
PIOS/SPI_SI	K8	SPI	SPI
PIOS/SPI_SCK	K9	SPI	SPI
PIOS/SPI_SS_B	J9	SPI	SPI
SPI_VCC	J10	SPI	SPI
PLLGND	L6	PLLGND	PLL
PLLVCC	L7	PLLVCC	PLL

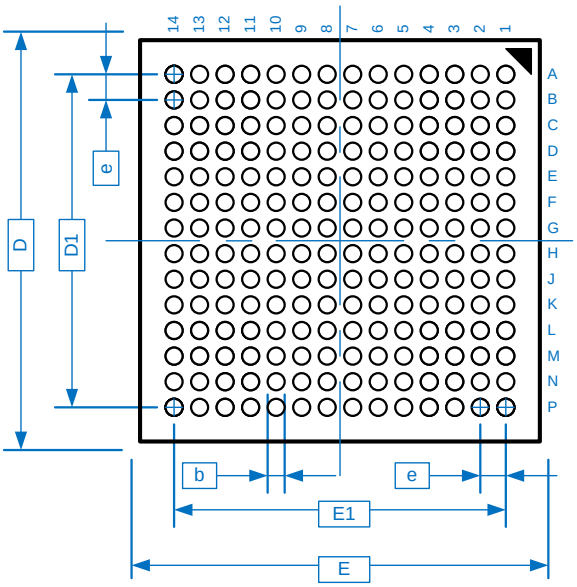
Ball Function	Ball Number	Pin Type	Bank
PIO2	N4	PIO	2
PIO2	N5	PIO	2
PIO2 (◆)	***iCE65P04:*** N8	PIO	2
PIO2	N9	PIO	2
PIO2	N11	PIO	2
PIO2	N12	PIO	2
PIO2	N13	PIO	2
PIO2	P1	PIO	2
PIO2	P2	PIO	2
PIO2	P3	PIO	2
PIO2	P4	PIO	2
PIO2	P7	PIO	2
PIO2	P8	PIO	2
PIO2	P9	PIO	2
PIO2/CBSEL0	L9	PIO	2
PIO2/CBSEL1	P10	PIO	2
VCCIO_2	J9	VCCIO	2
VCCIO_2	M5	VCCIO	2
VCCIO_2	N10	VCCIO	2
PIO3/DP00A	C1	DPIO	3
PIO3/DP00B	B1	DPIO	3
PIO3/DP01A	D3	DPIO	3
PIO3/DP01B	C3	DPIO	3
PIO3/DP02A	D1	DPIO	3
PIO3/DP02B	D2	DPIO	3
PIO3/DP03A (◆)	***iCE65P04:*** E1	DPIO	3
PIO3/DP03B (◆)	***iCE65P04:*** E2	DPIO	3
PIO3/DP04A	D4	DPIO	3
PIO3/DP04B	E4	DPIO	3
PIO3/DP05A (◆)	***iCE65P04:*** F3	DPIO	3
PIO3/DP05B (◆)	***iCE65P04:*** F4	DPIO	3
PIO3/DP06A	F5	DPIO	3
PIO3/DP06B	E5	DPIO	3
PIO3/DP07A (◆)	***iCE65P04:*** G2	DPIO	3
GBIN7/PIO3/DP07B (◆)	***iCE65P04:*** G1	GBIN	3
GBIN6/PIO3/DP08A	H1	GBIN	3
PIO3/DP08B	H2	DPIO	3
PIO3/DP09A	G3	DPIO	3
PIO3/DP09B	G4	DPIO	3
PIO3/DP10A	J1	DPIO	3
PIO3/DP10B	J2	DPIO	3
PIO3/DP11A (◆)	***iCE65P04:*** H4	DPIO	3
PIO3/DP11B (◆)	***iCE65P04:*** H3	DPIO	3
PIO3/DP12A	K2	DPIO	3
PIO3/DP12B	J3	DPIO	3
PIO3/DP13A	H5	DPIO	3
PIO3/DP13B	G5	DPIO	3
PIO3/DP14A	L1	DPIO	3
PIO3/DP14B	L2	DPIO	3
PIO3/DP15A	M1	DPIO	3
PIO3/DP15B	M2	DPIO	3

CB196: 8 x8 mm, 196-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array

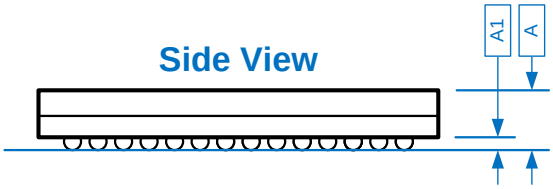
Top View



Bottom View



Side View



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			14		Columns
Number of Ball Rows	Y			14		Rows
Number of Signal Balls		n		196		Balls
Body Size	X	E	7.90	8.00	8.10	mm
	Y	D	7.90	8.00	8.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	6.50	—	
	Y	D1	—	6.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65P04F	Part number
	-T	Power/Speed
3	CB196I	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

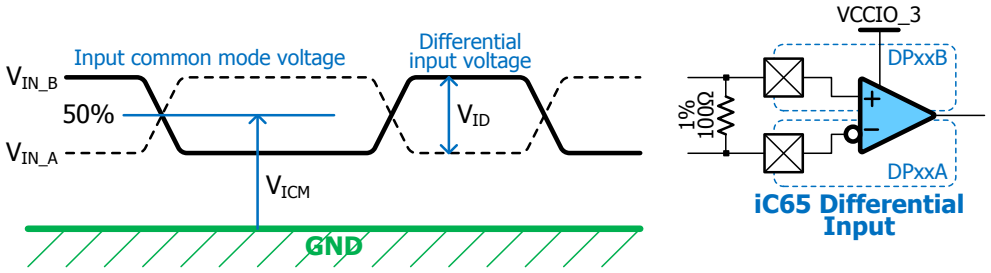
Ball Function	Ball Number	Pin Type by Device		Bank
		iCE65P04	iCE65P08	
PIO1 (●)	L22	N.C.	PIO	1
PIO1	M15	PIO	PIO	1
PIO1	M16	PIO	PIO	1
PIO1	M20	PIO	PIO	1
PIO1 (●)	M22	N.C.	PIO	1
PIO1	N15	PIO	PIO	1
PIO1	N16	PIO	PIO	1
PIO1	N22	PIO	PIO	1
PIO1	P15	PIO	PIO	1
PIO1	P16	PIO	PIO	1
PIO1	P18	PIO	PIO	1
PIO1	P20	PIO	PIO	1
PIO1	P22	PIO	PIO	1
PIO1	R18	PIO	PIO	1
PIO1	R20	PIO	PIO	1
PIO1	R22	PIO	PIO	1
PIO1	T20	PIO	PIO	1
PIO1	T22	PIO	PIO	1
PIO1	U20	PIO	PIO	1
PIO1 (●)	U22	N.C.	PIO	1
PIO1	V20	PIO	PIO	1
PIO1 (●)	V22	N.C.	PIO	1
PIO1	W20	PIO	PIO	1
PIO1 (●)	W22	N.C.	PIO	1
PIO1 (●)	Y22	N.C.	PIO	1
TCK	R16	JTAG	JTAG	1
TDI	T16	JTAG	JTAG	1
TDO	U18	JTAG	JTAG	1
TMS	V18	JTAG	JTAG	1
TRST_B	T18	JTAG	JTAG	1
VCCIO_1	H22	VCCIO	VCCIO	1
VCCIO_1	J20	VCCIO	VCCIO	1
VCCIO_1	K13	VCCIO	VCCIO	1
VCCIO_1	M18	VCCIO	VCCIO	1
CDONE	T14	CONFIG	CONFIG	2
CRESET_B	R14	CONFIG	CONFIG	2
GBIN4/PIO2	V12	GBIN	GBIN	2
GBIN5/PIO2	V11	GBIN	GBIN	2
PIO2	R8	PIO	PIO	2
PIO2	R9	PIO	PIO	2
PIO2	R10	PIO	PIO	2
PIO2	R11	PIO	PIO	2
PIO2	R12	PIO	PIO	2
PIO2	T7	PIO	PIO	2
PIO2	T8	PIO	PIO	2
PIO2	T10	PIO	PIO	2
PIO2	T11	PIO	PIO	2
PIO2	T12	PIO	PIO	2
PIO2	T13	PIO	PIO	2
PIO2	V6	PIO	PIO	2
PIO2	V7	PIO	PIO	2

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO2_10	N4	T10	77	965.00	139.20
GND	H7	V10	78	1,000.00	37.20
PIO2_11	P4	Y4	79	1,035.00	139.20
PIO2_12	L6	Y5	80	1,070.00	37.20
PIO2_13	—	AB6	81	1,105.00	139.20
PIO2_14	—	AB7	82	1,140.00	37.20
PIO2_15	—	AB8	83	1,175.00	139.20
PIO2_16	—	AB9	84	1,210.00	37.20
PIO2_17	—	AB10	85	1,245.00	139.20
PIO2_18	—	AB11	86	1,280.00	37.20
GND	H8	N12	87	1,315.00	139.20
PIO2_19	K6	Y6	88	1,350.00	37.20
PIO2_20	N5	Y7	89	1,385.00	139.20
VCC	J4	Y8	90	1,420.00	37.20
PIO2_21	—	—	91	1,455.00	139.20
PIO2_22	—	—	92	1,490.00	37.20
PLLGND	M6	Y9	93	1,525.00	139.20
PLLVCC	N6	Y10	94	1,595.00	37.20
GBIN5/PIO2_23	P5	V11	95	1,630.00	139.20
GBIN4/PIO2_24	L7	V12	96	1,665.00	37.20
PIO2_25	—	AB12	97	1,700.00	139.20
VCCIO_2	J9	Y11	98	1,735.00	37.20
PIO2_26	—	AB13	99	1,770.00	139.20
PIO2_27	K7	AB14	100	1,805.00	37.20
GND	J5	Y12	101	1,840.00	139.20
PIO2_28	K9	AB15	102	1,875.00	37.20
PIO2_29	M7	Y13	103	1,910.00	139.20
PIO2_30	K8	Y14	104	1,945.00	37.20
PIO2_31	P7	Y15	105	1,980.00	139.20
PIO2_32	L8	Y17	106	2,015.00	37.20
PIO2_33	P8	Y18	107	2,050.00	139.20
PIO2_34	N8	Y19	108	2,085.00	37.20
PIO2_35	M8	Y20	109	2,120.00	139.20
VCC	J7	N11	110	2,155.00	37.20
VCC	—	—	111	2,190.00	139.20
PIO2_36	P9	V13	112	2,225.00	37.20
PIO2_37	N9	T11	113	2,260.00	139.20
VCCIO_2	N10	N13	114	2,295.00	37.20
PIO2_38	M9	R11	115	2,330.00	139.20
GND	J8	M12	116	2,365.00	37.20
PIO2_39	N12	T12	117	2,400.00	139.20
PIO2_40	N11	R12	118	2,435.00	37.20
PIO2_41	N13	T13	119	2,470.00	139.20
PIO2_42/CBSEL0	L9	R13	120	2,505.00	37.20
PIO2_43/CBSEL1	P10	V14	121	2,540.00	139.20
CDONE	M10	T14	122	2,575.00	37.20
CRESET_B	L10	R14	123	2,625.00	139.20

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIOS_00/SPI_SO	M11	T15	124	2,690.00	37.20
PIOS_01/SPI_SI	P11	V15	125	2,740.00	139.20
GND	P6	Y16	126	2,790.00	37.20
PIOS_02/SPI_SCK	P12	V16	127	2,840.00	139.20
PIOS_03/SPI_SS_B	P13	V17	128	2,890.00	37.20
SPI_VCC	L11	R15	129	2,990.00	37.20
TDI	M12	T16	130	3,610.80	342.00
TMS	P14	V18	131	3,712.80	392.00
TCK	L12	R16	132	3,610.80	442.00
TDO	N14	U18	133	3,712.80	492.00
TRST_B	M14	T18	134	3,610.80	542.00
PIO1_00	K11	R18	135	3,712.80	592.00
PIO1_01	L13	P16	136	3,610.80	642.00
PIO1_02	K12	P15	137	3,712.80	692.00
PIO1_03	M13	P18	138	3,610.80	727.00
GND	J14	N18	139	3,712.80	762.00
GND	J14	N18	140	3,610.80	797.00
PIO1_04	J10	N16	141	3,712.80	832.00
PIO1_05	L14	N15	142	3,610.80	867.00
VCCIO_1	H14	M18	143	3,712.80	902.00
VCCIO_1	—	—	144	3,610.80	937.00
PIO1_06	J11	M16	145	3,712.80	972.00
PIO1_07	K14	M15	146	3,610.80	1,007.00
PIO1_08	H10	W20	147	3,712.80	1,042.00
PIO1_09	J13	V20	148	3,610.80	1,077.00
PIO1_10	J12	U20	149	3,712.80	1,112.00
VCC	N7	M13	150	3,610.80	1,147.00
VCC	—	—	151	3,712.80	1,182.00
PIO1_11	H13	T22	152	3,610.80	1,217.00
PIO1_12	H12	R22	153	3,712.80	1,252.00
PIO1_13	—	P22	154	3,610.80	1,287.00
PIO1_14	—	N22	155	3,712.80	1,322.00
PIO1_15	G13	T20	156	3,610.80	1,357.00
PIO1_16	H11	R20	157	3,712.80	1,392.00
PIO1_17	G14	P20	158	3,610.80	1,427.00
GND	K10	N20	159	3,712.80	1,462.00
GND	—	—	160	3,610.80	1,497.00
PIO1_18	G10	M20	161	3,712.80	1,532.00
GBIN3/PIO1_19	G12	K18	162	3,610.80	1,567.00
GBIN2/PIO1_20	F10	L18	163	3,712.80	1,602.00
PIO1_21	F14	K20	164	3,610.80	1,637.00
VCCIO_1	H14	J20	165	3,712.80	1,672.00
VCCIO_1	—	—	166	3,610.80	1,707.00
PIO1_22	F13	H20	167	3,712.80	1,742.00
PIO1_23	D13	G20	168	3,610.80	1,777.00
PIO1_24	G11	F20	169	3,712.80	1,812.00

Differential Inputs

Figure 41: **Differential Input Specifications**



Input common mode voltage: $$V_{ICM} = \frac{VCCIO\_3}{2} \pm \Delta V_{ICM}$$

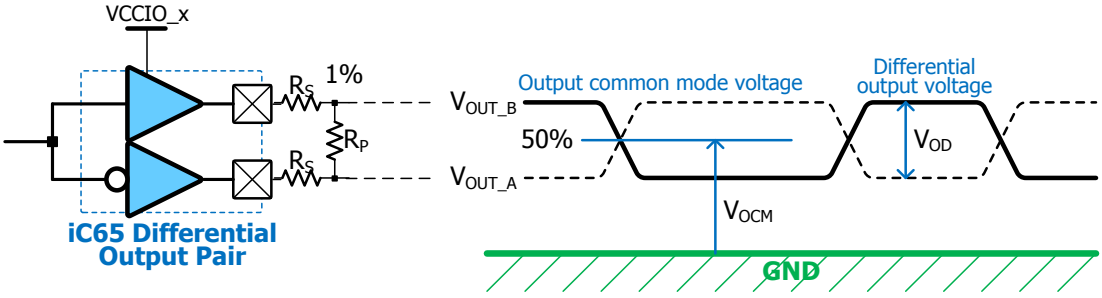
Differential input voltage: $$V_{ID} = |V_{IN\_B} - V_{IN\_A}|$$

Table 55: **Recommended Operating Conditions for Differential Inputs**

I/O Standard	VCCIO_3 (V)			V_{ID} (mV)			V_{ICM} (V)		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	250	350	450	$\frac{VCCIO\_3}{2} - 0.30$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.30$
SubLVDS	1.71	1.80	1.89	100	150	200	$\frac{VCCIO\_3}{2} - 0.25$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.25$

Differential Outputs

Figure 42: **Differential Output Specifications**



Output common mode voltage: $$V_{OCM} = \frac{VCCIO\_x}{2} \pm \Delta V_{OCM}$$

Differential output voltage: $$V_{OD} = |V_{OUT\_B} - V_{OUT\_A}|$$

Table 56: **Recommended Operating Conditions for Differential Outputs**

I/O Standard	VCCIO_x (V)			Ω		V_{OD} (mV)			V_{OCM} (V)		
	Min	**Nom**	**Max**	**R_S**	**R_P**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	150	140	300	350	400	$\frac{VCCIO}{2} - 0.15$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.15$
SubLVDS	1.71	1.80	1.89	270	120	100	150	200	$\frac{VCCIO}{2} - 0.10$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.10$

I/O Banks 0, 1, 2 and SPI Bank Characteristic Curves

Figure 43: **Typical LVCMOS Output Low Characteristics (I/O Banks 0, 1, 2, and SPI)**

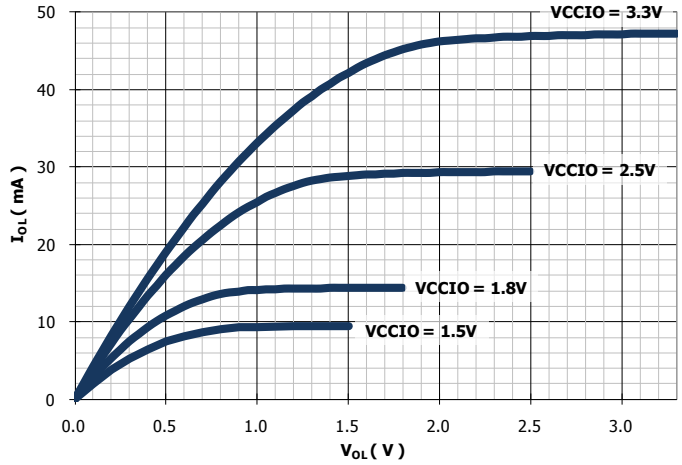


Figure 44: **Typical LVCMOS Output High Characteristics (I/O Banks 0, 1, 2, and SPI)**

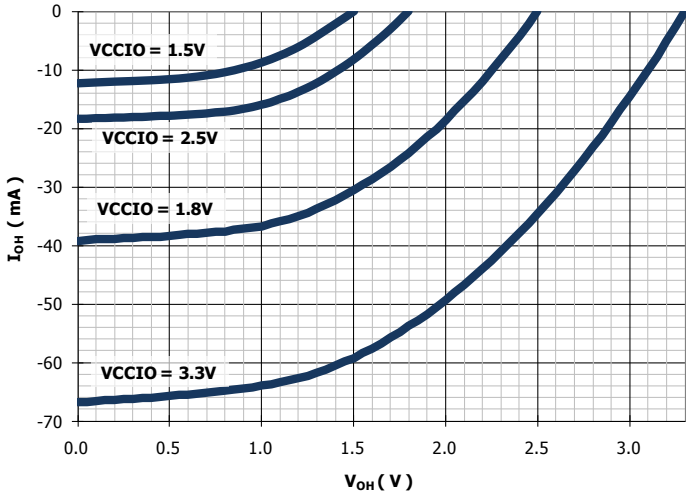
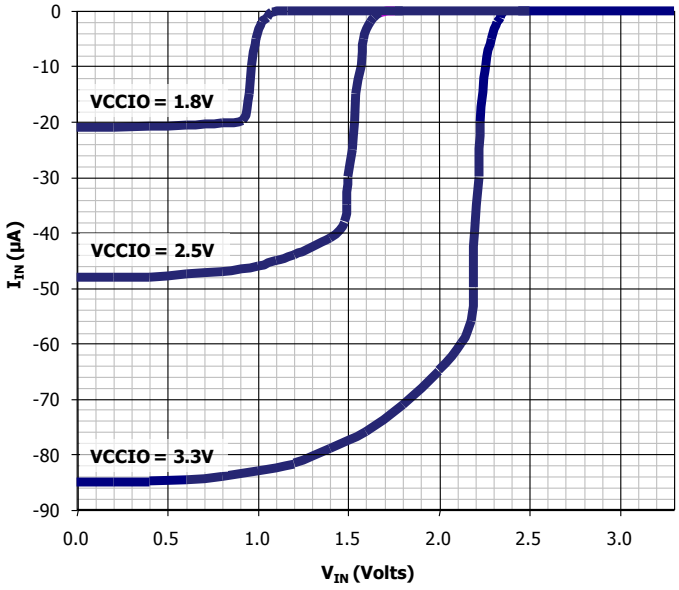


Figure 45: **Input with Internal Pull-Up Resistor Enabled (I/O Banks 0, 1, 2, and SPI)**



RAM4K Block

Table 59 provides timing information for the logic in a RAM4K block, which includes the paths shown in Figure 50.

Figure 50: **RAM4K Timing Circuit**

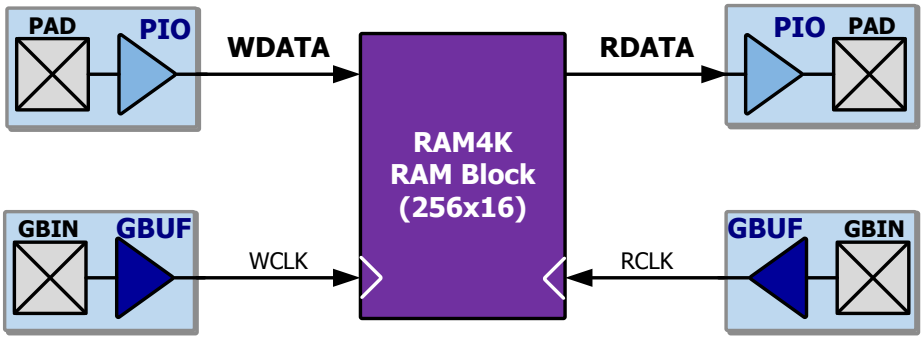


Table 59: **Typical RAM4K Block Timing**

Symbol	From	To	Description	Power/Speed Grade: –T Nominal VCC: 1.2 V Typ.	Units
Write Setup/Hold Time					
t_{SUWD}	PIO input	GBIN input	Minimum write data setup time on PIO inputs before active clock edge on GBIN input, include interconnect delay.	0.8	ns
t_{HDWD}	GBIN input	PIO input	Minimum write data hold time on PIO inputs after active clock edge on GBIN input, including interconnect delay.	0	ns
Read Clock-Output-Time					
t_{CKORD}	RCLK clock input	PIO output	Clock-to-output delay from RCLK input pin, through RAM4K RDATA output flip-flop to PIO output pad, including interconnect delay.	7.3	ns
t_{GBCKRM}	GBIN input	RCLK clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to the RCLK clock input.	2.6	ns
Write and Read Clock Characteristics					
t_{RMWCKH}	WCLK RCLK	WCLK RCLK	Write clock High time	0.54	ns
t_{RMWCKL}			Write clock Low time	0.63	ns
t_{RMWCYC}			Write clock cycle time	1.27	ns
F_{WMAX}			Sustained write clock frequency	256	MHz

Table 64 provides various timing specifications for the SPI peripheral mode interface.

Table 64: **SPI Peripheral Mode Timing**

Symbol	From	To	Description	All Grades		Units
				Min.	Max.	
t_{CR_SCK}	CRESET_B	SPI_SCK	Minimum time from a rising edge on CRESET_B until the first SPI write operation, first SPI_SCK. During this time, the iCE65P FPGA is clearing its internal configuration memory	300	—	µs
$t_{SUSPISI}$	SPI_SI	SPI_SCK	Setup time on SPI_SI before the rising SPI_SCK clock edge	12	—	ns
$t_{HDSPISI}$	SPI_SCK	SPI_SI	Hold time on SPI_SI after the rising SPI_SCK clock edge	12	—	ns
$t_{SPISCKH}$	SPI_SCK	SPI_SCK	SPI_SCK clock High time	20	—	ns
$t_{SPISCKL}$	SPI_SCK	SPI_SCK	SPI_SCK clock Low time	20	—	ns
$t_{SPISCKCYC}$	SPI_SCK	SPI_SCK	SPI_SCK clock period*	40	1,000	ns
F_{SPI_SCK}	SPI_SCK	SPI_SCK	Sustained SPI_SCK clock frequency*	1	25	MHz

* = Applies after sending the synchronization pattern.

Power Consumption Characteristics

Core Power

Table 65 shows the power consumed on the internal VCC supply rail when the device is filled with 16-bit binary counters, measured with a 32.768 kHz and at 32.0 MHz

Table 65: **VCC Power Consumption for Device Filled with 16-Bit Binary Counters**

Symbol	Description	Grade	VCC	iCE65P04		Units
				Typical	Max.	
I_{CC0K}	f =0	–T	1.2V	45		µA
I_{CC32K}	f ≤ 32.768 kHz	–T	1.2V	52		µA
I_{CC32M}	f = 32.0 MHz	–T	1.2V	8		mA

I/O Power

Table 66 provides the static current by I/O bank. The typical current for I/O Banks 0, 1, 2 and the SPI bank is not measurable within the accuracy of the test environment. The PIOs in I/O Bank 3 use different circuitry and dissipate a small amount of static current.

Table 66: I/O Bank Static Current (f = 0 MHz)

Symbol	Description		Typical	Maximum	Units
I_{CCO_0}	I/O Bank 0	Static current consumption per I/O bank. f = 0 MHz. No PIO pull-up resistors enabled. All inputs grounded. All outputs driving Low.	« 1		uA
I_{CCO_1}	I/O Bank 1		« 1		uA
I_{CCO_2}	I/O Bank 2		« 1		uA
I_{CCO_3}	I/O Bank 3		1.2		uA
I_{CCO_SPI}	SPI Bank		« 1		uA

NOTE: The typical static current for I/O Banks 0, 1, 2, and the SPI bank is less than the accuracy of the device tester.

Power Estimator

To estimate the power consumption for a specific application, please download and use the iCE65P Power Estimator Spreadsheet our use the power estimator built into the iCEcube software.

Revision History

Version	Date	Description
1.31	22-APR-2011	Updated Figure 35: iCE65P04 CB121 Chip-Scale BGA Footprint (Top View) A10 to PIO0 and G1 to PIO3/DP08B. Updated Table 46: iCE65P04 CB121 Chip-scale BGA Pinout Table F4 to GBIN6/PIO3/DP06A and G4 to PIO3/DP06B.
1.3	17-DEC-2010	Updated Table 60: Phase-Locked Loop (PLL) Block Timing duty cycle, jitter and lock/reset time parameters
1.2	08-OCT-2010	Changed FSPI_SCK from 0.125 MHz to 1 MHz in SPI Peripheral Configuration Process and Table 64. Updated equation: PLLOUT Frequency for FEEDBACK_PATH = SIMPLE
1.1	06-AUG-2010	Added CB121 package. Removed Programmable Interconnect description
1.0	15-FEB-2010	Initial Release

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