Lattice Semiconductor Corporation - ICE65P04F-TCB284I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	174
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	284-VFBGA, CSPBGA
Supplier Device Package	284-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65p04f-tcb284i

Table 4: **Flip-flop Packing/Sharing within a PLB**

Group	Active Clock Edge	Clock Enable	Set or Reset Control (Sync. or Async)
1	↑	None (always enabled)	None
2	↓		
3	↑		PLB set/reset control
4	↓		
5	↑	Selective (controlled by PLB clock enable)	None
6	↓		
7	↑		PLB set/reset control
8	↓		

For detailed flip-flop internal timing, see Table 57.

Carry Logic

The dedicated Carry Logic within each Logic Cell primarily accelerates and improves the efficiency of arithmetic logic such as adders, accumulators, subtracters, incrementers, decrementers, counters, ALUs, and comparators. The Carry Logic also supports wide combinational logic functions.

$$COUT = I1 \bullet I2 + CIN \bullet I1 + CIN \bullet I2 \qquad \text{[Equation 1]}$$

Equation 1 and Figure 4 describe the Carry Logic structure within a Logic Cell. The Carry Logic shares inputs with the associated Look-Up Table (LUT4). The LUT4's I1 and I2 inputs directly feed the Carry Logic; inputs I0 and I3 do not. A signal cascades between Logic Cells within the Programmable Logic Block. The carry input from the previous adjacent Logic Cell optionally provides an alternate input to the LUT4 function, supplanting the I3 input.

Low-Power Disable

To save power and prevent unnecessary signal switching, the Carry Logic function within a Logic Cell is disabled if not used. The output of a Logic Cell's Carry Logic is forced High.

PLB Carry Input and Carry Output Connections

As shown in Figure 4, each Programmable Logic Block has a carry input signal that can be initialized High, Low, or come from the carry output signal from PLB immediately below.

Similarly, the Carry Logic output from the Programmable Logic Block connects to the PLB immediately above, which allows the Carry Logic to span across multiple PLBs in a column. As shown in Figure 5, the Carry Logic chain can be tapped mid-way through a chain or a PLB by feeding the value through a LUT4 function.

Adder Example

Figure 5 shows an example design that uses the Carry Logic. The example is a 2-bit adder, which can be expanded into an adder of arbitrary size. The LUT4 function within a Logic Cell is programmed to calculate the sum of the two input values and the carry input, `A[i] + B[i] + CARRY_IN[i-1] = SUM[i]`.

The Carry Logic generates the carry value to feed the next bit in the adder. The calculated carry value replaces the I3 input to the next LUT4 in the upper Logic Cell.

If required by the application, the carry output from the final stage of the adder is available by passing it through the final LUT4.

Figure 4: **Carry Logic Structure within a Logic Cell and between PLBs**

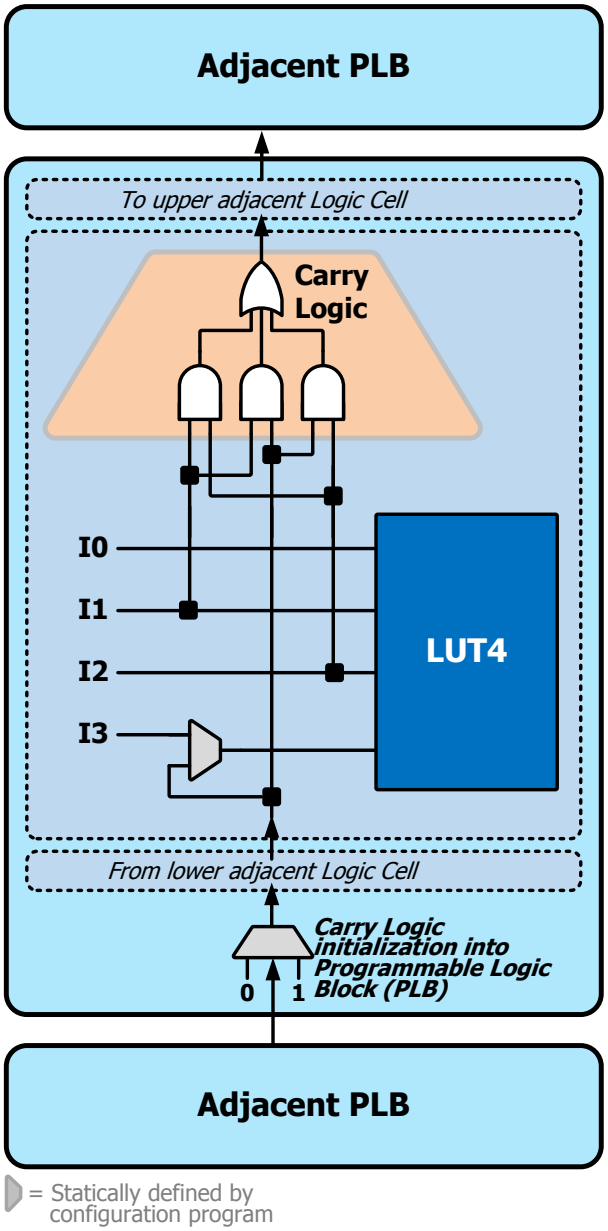
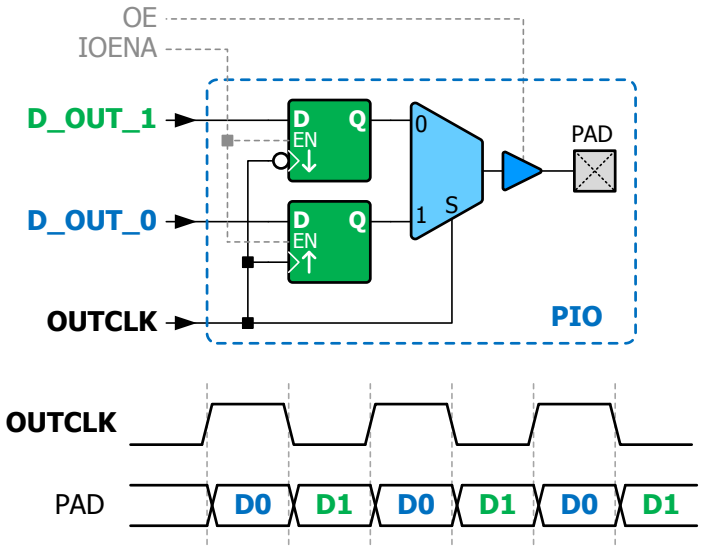
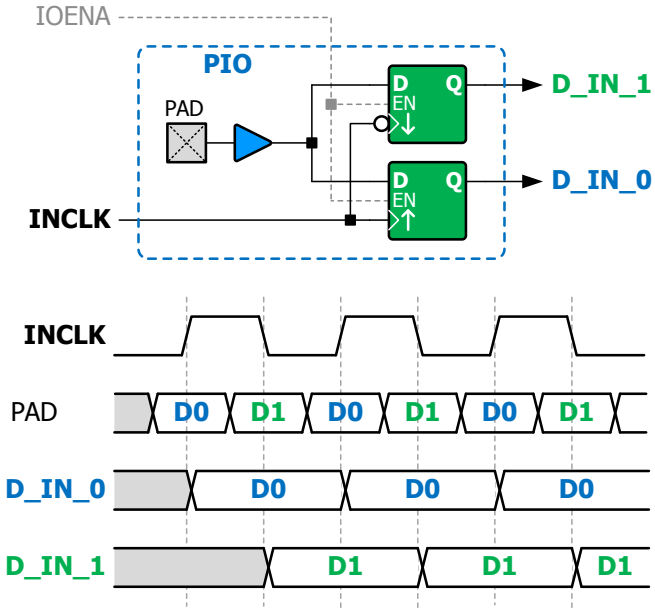


Figure 11: **DDR Output Flip-Flop**



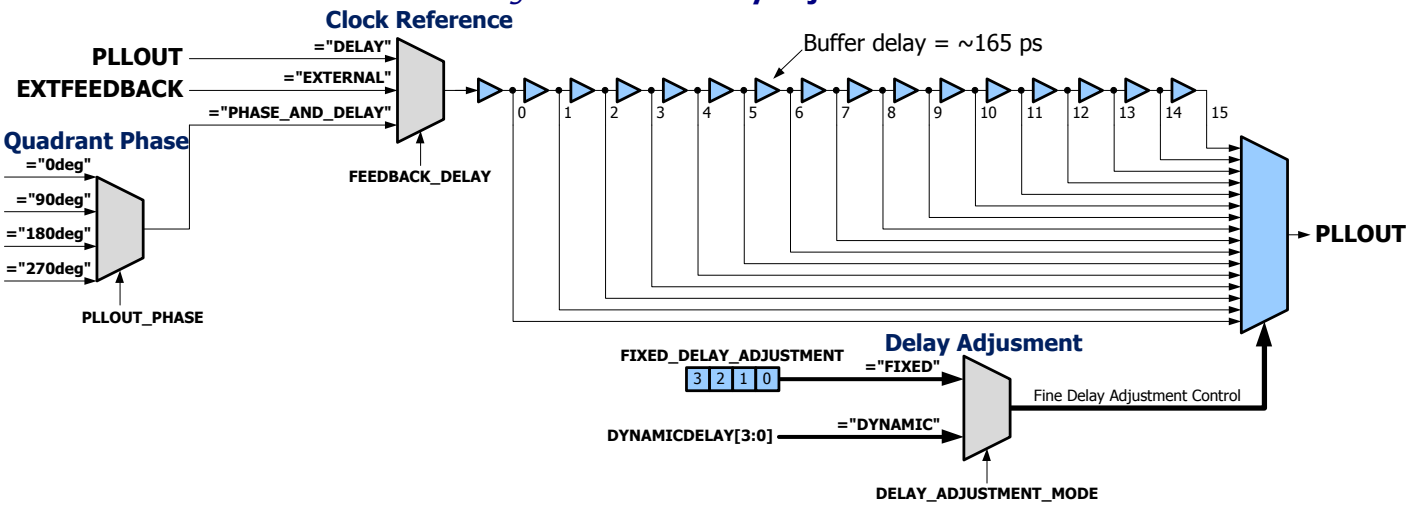
Similarly, Figure 12 demonstrates the DDR input flip-flop functionality. A double data rate (DDR) signal arrives at the pad. Internally, one value is clocked by the rising edge of the INCLK signal and another value is clocked by the falling edge of the INCLK signal. The DDR data stream is effectively de-multiplexed within the PIO pin and presented to the programmable interconnect on D_IN_0 and D_IN_1.

Figure 12: **DDR Input Flip-Flop**



The DDR flip-flops provide several design advantages. Internally within the iCE65P device, the clock frequency is half the effective external data rate. The lower clock frequency eases internal timing, doubling the clock period, and slashes the clock-related power in half.

Figure 19: **Fine Delay Adjust Controls**



Fine Adjustment Control

The number of delay taps is controlled either statically using the FIXED_DELAY_ADJUSTMENT option or dynamically by the application using the PLL's DYNAMIC_DELAY[3:0] inputs, as described in Table 21.

Table 21: **Fine Delay Adjustment Control**

DELAY_ADJUSTMENT_MODE Setting	Adjustment Control
FIXED	FIXED_DELAY_ADJUSTMENT attribute setting
DYNAMIC	DYNAMIC_DELAY[3:0] control inputs

Fine Adjustment Delay

The resulting nominal fine adjustment delay value is shown in Equation 5, where ***n*** is either the value of the FIXED_DELAY_ADJUSTMENT attribute setting or the dynamic binary value presented on the DYNAMIC_DELAY[3:0] inputs. The actual delay varies slightly due to the slight differences in the delay tap buffer delay.

$$\text{Fine Delay Adjustment } \textit{(nominal)} = (n + 1) \bullet 165 \text{ ps} \qquad \text{[Equation 5]}$$

Phase Angle Equivalent

The fine delay adjustment feature always injects an actual delay value, not a fixed phase angle like the Fixed Quadrant Phase Shift feature. Use Equation 6 to convert the fine adjustment delay to a resulting phase angle.

$$\text{Phase\_Shift} = \frac{\text{Fine\_Delay\_Adjustment}}{\text{Clock\_Period}} \bullet 360^{\circ} \qquad \text{[Equation 6]}$$

Low Power Mode

The phase-lock loop (PLL) has low operating power by default. The PLL can be dynamically disabled to further reduce power. The low-power mode must first be enabled by setting the ENABLE_ICEGATE attribute to '1'. Once enabled, use the LATCHINPUTVALUE to control the PLL's operation, as shown in Table 22. The PLL must reacquire the input clock and LOCK when LATCHINPUTVALUE returns from '1' to '0', external feedback is used and path goes out into the fabric.

Table 22: **PLL LATCHINPUTVALUE Control**

ENABLE_ICEGATE Attribute	LATCHINPUTVALUE Input	Function
0	Don't care	PLL is always enabled
1	0	PLL is enabled and operating
	1	PLL is in low-power mode; PLLOUT output holds last clock state

Device Configuration

As described in Table 27, iCE65P components are configured for a specific application by loading a binary configuration bitstream image, generated by the SiliconBlue development system. For high-volume applications, the bitstream image is usually permanently programmed in the on-chip Nonvolatile Configuration Memory (NVCM). However, the bitstream image can also be stored external in a standard, low-cost commodity SPI serial Flash PROM. The iCE65P component can automatically load the image using the SPI Master Configuration Interface. Similarly, the iCE65P configuration data can be downloaded from an external processor, microcontroller, or DSP processor using an SPI-like serial interface or an IEEE 1149 JTAG interface.

Table 27: **iCE65P Device Configuration Modes**

Mode	Analogy	Configuration Data Source
NVCM	ASIC	Internal, lowest-cost, secure, one-time programmable Nonvolatile Configuration Memory (NVCM)
SPI Flash	Microprocessor	External, low-cost, commodity, SPI serial Flash PROM
SPI Peripheral	Processor Peripheral	Configured by external device, such as a processor, microcontroller, or DSP using practically any data source, such as system Flash, a disk image, or over a network connection.
JTAG	JTAG	JTAG configuration requires sending a special command sequence on the SPI interface to enable JTAG configuration. Configuration is controlled by and external device.

Configuration Mode Selection

The iCE65P configuration mode is selected according to the following priority described below and illustrated in Figure 23.

- After exiting the Power-On Reset (POR) state or when CRESET_B returns High after being held Low for 250 ns or more, the iCE65P FPGA samples the logical value on its SPI_SS_B pin. Like other programmable I/O pins, the SPI_SS_B pin has an internal pull-up resistor (see Input Pull-Up Resistors on I/O Banks 0, 1, and 2).
- If the SPI_SS_B pin is sampled as a logic '1' (High), then …
  - Check if the iCE65P is enabled to configure from the Nonvolatile Configuration Memory (NVCM). If the iCE65P device has NVCM memory ('**F**' ordering code) but the NVCM is yet unprogrammed, then the iCE65P device is not enabled to configure from NVCM. Conversely, if the NVCM is programmed, the iCE65P device will configure from NVCM.
    - If enabled to configure from NVCM, the iCE65P device configures itself using the Nonvolatile Configuration Memory (NVCM).
    - If not enabled to configure from NVCM, then the iCE65P FPGA configures using the SPI Master Configuration Interface.
- If the SPI_SS_B pin is sampled as a logic '0' (Low), then the iCE65P device waits to be configured from an external controller or from another iCE65P device in SPI Master Configuration Mode using an SPI-like interface.

Power-On Reset (POR)

The Power-on Reset (POR) circuit monitors specific voltage supply inputs and holds the device in reset until all the relevant supplies exceed the internal voltage thresholds. The SPI_VCC supply also has an additional time-out delay to allow an attached SPI serial PROM to power up properly. Table 31 shows the POR supply inputs. The Nonvolatile Configuration Memory (NVCM) requires that the VPP_2V5 supply be connected, even if the application does not use the NVCM.

Table 31: **Power-on Reset (POR) Voltage Resources**

Supply Rail	iCE65P Production Devices
VCC	Yes
SPI_VCC	Yes
VCCIO_1	No
VCCIO_2	Yes
VPP_2V5	Yes

CRESET_B Pin

The CRESET_B pin resets the iCE65P internal logic when Low.

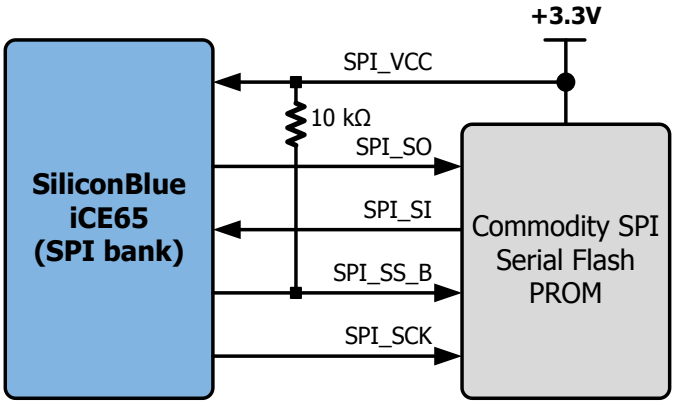
JTAG Interface

Specific command sequences also reset the iCE65P internal logic.

SPI Master Configuration Interface

All iCE65P devices, including those with NVCM, can be configured from an external, commodity SPI serial Flash PROM, as shown in Figure 26. The SPI configuration interface is essentially its own independent I/O bank, powered by the VCC_SPI supply input. Presently, most commercially-available SPI serial Flash PROMs require a 3.3V supply.

Figure 26: **iCE65P SPI Master Configuration Interface**



The SPI configuration interface is used primarily during development before mass production, where the configuration is then permanently programmed in the NVCM configuration memory. However, the SPI interface can also be the primary configuration interface allowing easy in-system upgrades and support for multiple configuration images.

The SPI control signals are defined in Table 32. Table 33 lists the SPI interface ball or pins numbers by package.

Table 32: **SPI Master Configuration Interface Pins (SPI_SS_B High before Configuration)**

Signal Name	Direction	Description
SPI_VCC	Supply	SPI Flash PROM voltage supply input.
SPI_SO	Output	SPI Serial Output from the iCE65P device.
SPI_SI	Input	SPI Serial Input to the iCE65P device, driven by the select SPI serial Flash PROM.
SPI_SS_B	Output	SPI Slave Select output from the iCE65P device. Active Low.
SPI_SCK	Output	SPI Slave Clock output from the iCE65P device.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Table 33: **SPI Interface Ball Numbers by Package**

SPI Interface	Package Code		
	CB121	**CB196**	**CB284**
SPI_VCC	J10	L11	R15
PIOS/SPI_SO	J8	M11	T15
PIOS/SPI_SI	K8	P11	V15
PIOS/SPI_SS_B	J9	P13	V17
PIOS/SPI_SCK	K9	P12	V16

SPI PROM Requirements

The iCE65P mobileFPGA SPI Flash configuration interface supports a variety of SPI Flash memory vendors and product families. However, SiliconBlue Technologies does not specifically test, qualify, or otherwise endorse any specific SPI Flash vendor or product family. The iCE65P SPI interface supports SPI PROMs that they meet the following requirements.

- The PROM must operate at 3.3V or 2.5V in order to trigger the iCE65P FPGA's power-on reset circuit.
- The PROM must support the 0x0B Fast Read command, using a 24-bit start address and has 8 dummy bits before the PROM provides first data (see Figure 28: SPI Fast Read Command).
- The PROM must have enough bits to program the iCE65P device (see Table 34: Smallest SPI PROM Size (bits), by Device, by Number of Images).
- The PROM must support data operations at the upper frequency range for the selected iCE65P internal oscillator frequency (see Table 61). The oscillator frequency is selectable when creating the FPGA bitstream image.
- For lowest possible power consumption after configuration, the PROM should also support the 0xB9 Deep Power Down command and the 0xAB Release from Deep Power-down Command (see Figure 27 and Figure 29). The low-power mode is optional.
- The PROM must be ready to accept commands 10 µs after meeting its power-on conditions. In the PROM data sheet, this may be specified as t_{VSL} or t_{VCSL}. It is possible to use slower PROMs by holding the CRESET_B input Low until the PROM is ready, then releasing CRESET_B, either under program control or using an external power-on reset circuit.

The SiliconBlue iCEman65 development board and associated programming software uses an ST Micro/Numonyx M25Pxx SPI serial Flash PROM.

SPI PROM Size Requirements

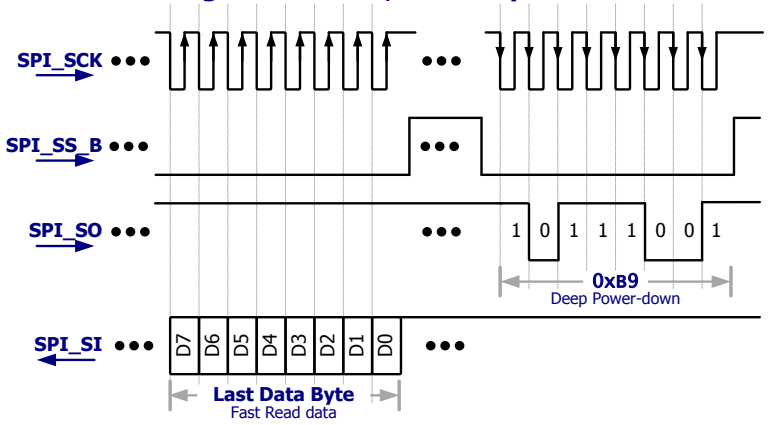
Table 34 lists the minimum SPI PROM size required to configure an iCE65P device. Larger PROM sizes are allowed, but not required unless the end application uses the additional space. SPI serial PROM sizes are specified in bits. For each device size, the table shows the required minimum PROM size for "Logic Only" (no BRAM initialization) and "Logic + RAM4K" (RAM4K blocks pre-initialized). Furthermore, the table shows the PROM size for varying numbers of configuration images. Most applications will use a single image. Applications that use the Cold Boot or Warm Boot features may use more than one image.

Table 34: **Smallest SPI PROM Size (bits), by Device, by Number of Images**

Device	1 Image		2 Images		3 Images		4 Images	
	Logic Only	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**
iCE65P04	512K	1M	1M	2M	2M	2M	2M	4M

After transferring the required number configuration data bits, the iCE65P device ends the Fast Read command by de-asserting its SPI_SS_B PROM select output, as shown in Figure 29. To conserve power, the iCE65P device then optionally issues a final Deep Power-down command, hexadecimal command code 0xB9. After de-asserting the SPI_SS_B output, the SPI PROM enters its Deep Power-down mode. The final power-down step is optional; the application may wish to use the SPI PROM and can skip this step, controlled by a configuration option.

Figure 29: **Final Configuration Data, SPI Deep Power-down Command**



Cold Boot Configuration Option

By default, the iCE65P FPGA is programmed with a single configuration image, either from internal NVCM memory, from an external SPI Flash PROM, or externally from a processor or microcontroller.

Figure 30: **ColdBoot and WarmBoot Configuration**

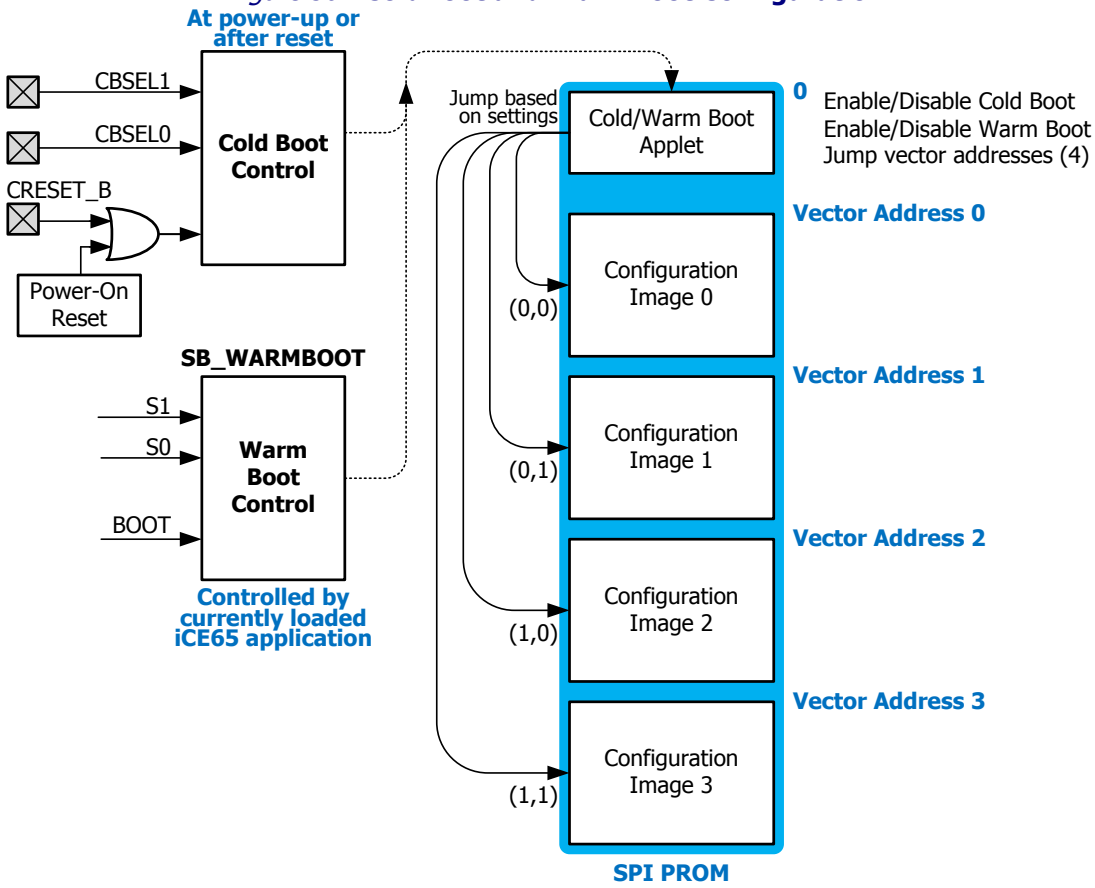
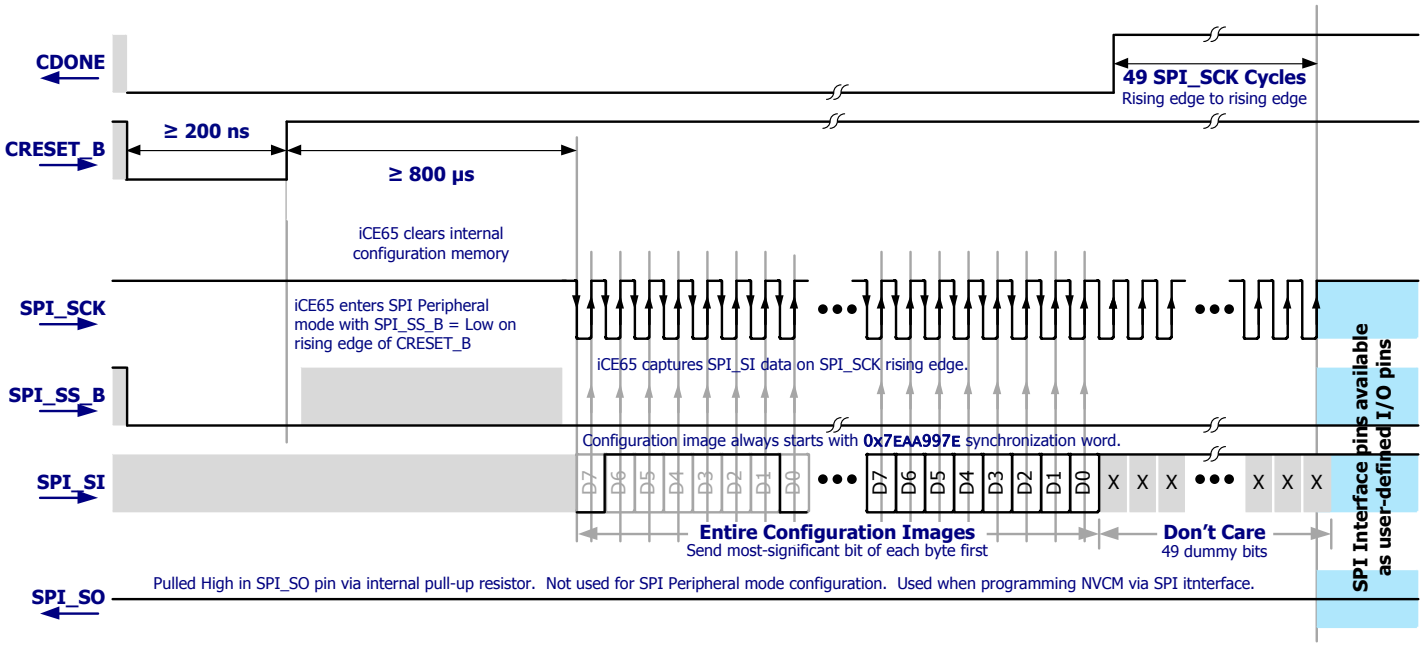


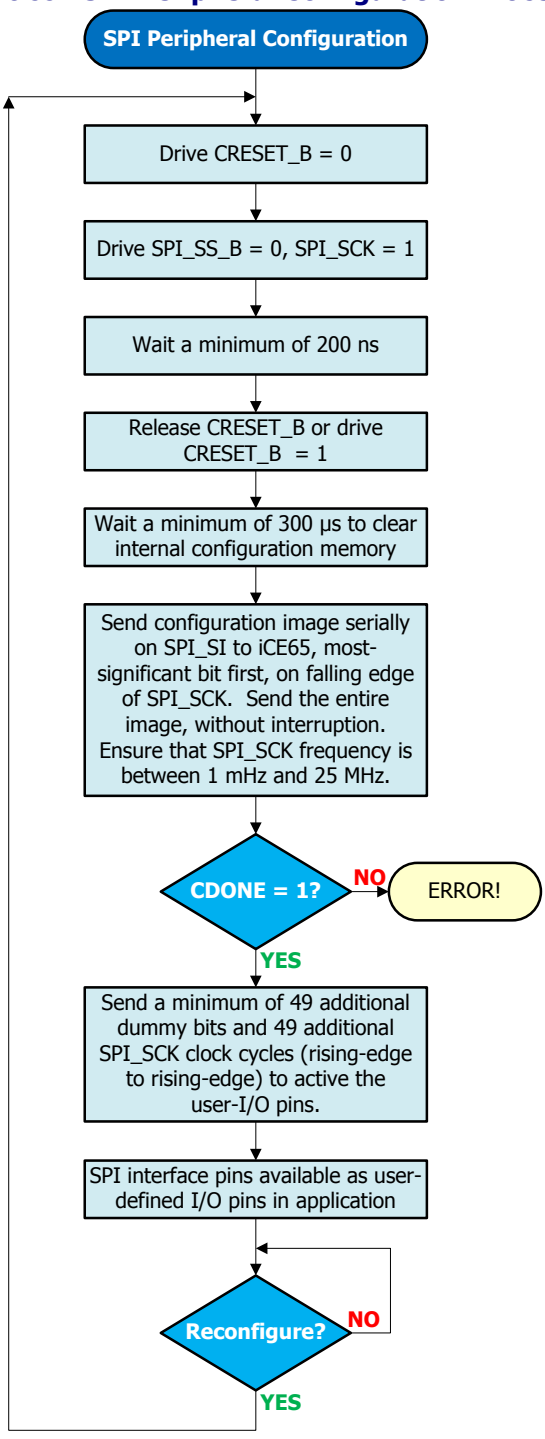
Figure 32: **Application Processor Waveforms for SPI Peripheral Mode Configuration Process**



The iCE65 configuration image must be sent as one contiguous stream without interruption.

The SPI_SCK clock period must be between 40 ns to 1 µs (1 MHz to 25 MHz).

Figure 33: **SPI Peripheral Configuration Process**



Voltage Compatibility

As shown in Figure 26, there are potentially three different supply voltages involved in the SPI Peripheral interface, described in Table 37.

Table 37: **SPI Peripheral Mode Supply Voltages**

Supply Voltage	Description
AP_VCCIO	I/O supply to the Application Processor (AP)
VCC_SPI	Voltage supply for the iCE65P SPI interface.
VCCIO_2	Supply voltage for the iCE65P I/O Bank 2.

Signal Name	Direction	I/O Bank	Pull-up during Config	Description
PLLVCC	Supply	PLL	N/A	Analog voltage supply for Phase Lock Loop (PLL). If unused, tie to ground.
TDI	Input	1	No	JTAG Test Data Input. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TMS	Input	1	No	JTAG Test Mode Select. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TCK	Input	1	No	JTAG Test Clock. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1.
TDO	Output	1	No	JTAG Test Data Output.
TRST_B	Input	1	No	JTAG Test Reset, active Low. Keep Low during normal operation; High for JTAG operation.
VCC	Supply	All	N/A	Internal core voltage supply. All must be connected.
VCCIO_0	Supply	0	N/A	Voltage supply to I/O Bank 0. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
VCCIO_1	Supply	1	N/A	Voltage supply to I/O Bank 1. All such pins or balls on the package must be connected. Required to guarantee a valid input voltage on TRST_B JTAG pin.
VCCIO_2	Supply	2	N/A	Voltage supply to I/O Bank 2. All such pins or balls on the package must be connected. Required input to the Power-On Reset (POR) circuit.
VCCIO_3	Supply	3	N/A	Voltage supply to I/O Bank 3. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
SPI_VCC	Supply	SPI	N/A	SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM. Required input to the Power-On Reset (POR) circuit.
VPP_FAST	Supply	All	N/A	Direct programming voltage supply. If unused, leave floating or unconnected during normal operation.
VPP_2V5	Supply	All	N/A	Programming supply voltage. When the iCE65P device is active, VPP_2V5 must be in the valid range between 2.3 V to 3.47 V to release the Power-On Reset circuit, even if the application is not using the NVCM.
VREF	Voltage Reference	3	N/A	Input reference voltage in I/O Bank 3 for the SSTL I/O standard. This pin only appears on the CB284 package and for die-based products.

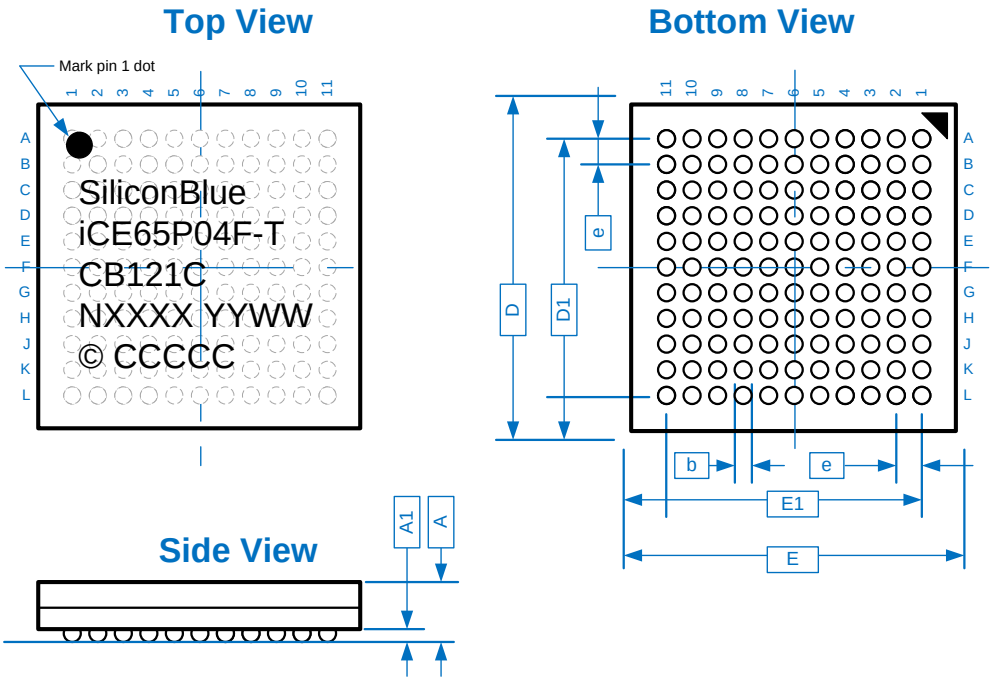
N/A = Not Applicable

Ball Function	Ball Number	Pin Type	Bank
PIO2	J4	PIO	2
PIO2	J5	PIO	2
PIO2	J11	PIO	2
PIO2	K3	PIO	2
PIO2	K4	PIO	2
PIO2	K11	PIO	2
PIO2	L2	PIO	2
PIO2	L3	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L10	PIO	2
PIO2	L11	PIO	2
PIO2/CBSEL0	H6	PIO	2
PIO2/CBSEL1	J6	PIO	2
VCCIO_2	K5	VCCIO	2
PIO3/DP00A	C1	DPIO	3
PIO3/DP00B	B1	DPIO	3
PIO3/DP01A	D1	DPIO	3
PIO3/DP01B	E2	DPIO	3
PIO3/DP02A	C2	DPIO	3
PIO3/DP02B	D2	DPIO	3
PIO3/DP03A	C3	DPIO	3
PIO3/DP03B	C4	DPIO	3
PIO3/DP04A	E4	DPIO	3
PIO3/DP04B	D4	DPIO	3
PIO3/DP05A	F3	DPIO	3
PIO3/DP05B	G3	DPIO	3
PIO3/DP06B	G4	DPIO	3
GBIN6/PIO3/DP06A	F4	GBIN	3
GBIN7/PIO3/DP07B	D3	GBIN	3
PIO3/DP07A	E3	DPIO	3
PIO3/DP08A	F2	DPIO	3
PIO3/DP08B	G1	DPIO	3
PIO3/DP09A	H1	DPIO	3
PIO3/DP09B	J1	DPIO	3
PIO3/DP10A	H2	DPIO	3
PIO3/DP10B	H3	DPIO	3
PIO3/DP11A	J3	DPIO	3
PIO3/DP11B	J2	DPIO	3
PIO3/DP12A	K1	DPIO	3
PIO3/DP12B	L1	DPIO	3
VCCIO_3	A1	VCCIO	3
VCCIO_3	G2	VCCIO	3
PIOS/SPI_SO	J8	SPI	SPI
PIOS/SPI_SI	K8	SPI	SPI
PIOS/SPI_SCK	K9	SPI	SPI
PIOS/SPI_SS_B	J9	SPI	SPI
SPI_VCC	J10	SPI	SPI
PLLGND	L6	PLLGND	PLL
PLLVCC	L7	PLLVCC	PLL

Package Mechanical Drawing

Figure 36: **CB121 Package Mechanical Drawing**

CB121: 6 x 6 mm, 121-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			11		Columns
Number of Ball Rows	Y			11		Rows
Number of Signal Balls		n		121		Balls
Body Size	X	E	5.90	6.00	6.10	mm
	Y	D	5.90	6.00	6.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.2	—	0.3	
Edge Ball Center to Center	X	E1	—	5.00	—	
	Y	D1	—	5.00	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.12	—	0.20	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65P04F	Part number
	-T	Power/Speed
3	CB121C	Package type
	ENG	Engineering
4	NXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
54	45

Die Cross Reference

The tables in this section list all the pads on a specific die type and provide a cross reference on how a specific pad connects to a ball or pin in each of the available package offerings. Similarly, the tables provide the pad coordinates for the die-based version of the product (iCE DiCE). These tables also provide a way to prototype with one package option and then later move to a different package or die.

As described in "Input and Output Register Control per PIO Pair" on page 14, PIO pairs share register control inputs. Similarly, as described in "Differential Inputs and Outputs" on page 11, a PIO pair can form a differential input or output. PIO pairs in I/O Bank 3 are optionally differential inputs or differential outputs. PIO pairs in all other I/O Banks are optionally differential outputs. In the tables, differential pairs are surrounded by a heavy blue box.

iCE65P04

Table 49 lists all the pads on the iCE65P04 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65P04 DiePlus product, please contact your SiliconBlue sales representative..

Table 49: **iCE65P04 Die Cross Reference**

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_00/DP00A	C1	F5	1	129.40	2,687.75
PIO3_01/DP00B	B1	G5	2	231.40	2,642.74
PIO3_02/DP01A	D3	G7	3	129.40	2,597.75
PIO3_03/DP01B	C3	H7	4	231.40	2,552.74
GND	F1	K5	5	129.40	2,507.75
GND	—	—	6	231.40	2,462.74
VCCIO_3	E3	J7	7	129.40	2,417.75
VCCIO_3	—	—	8	231.40	2,372.74
PIO3_04/DP02A	D1	H8	9	129.40	2,327.75
PIO3_05/DP02B	D2	J8	10	231.40	2,292.74
PIO3_06/DP03A	E1	H5	11	129.40	2,257.75
PIO3_07/DP03B	E2	J5	12	231.40	2,222.74
VCC	H9	D3	13	129.40	2,187.75
PIO3_08/DP04A	D4	K8	14	231.40	2,152.74
PIO3_09/DP04B	E4	K7	15	129.40	2,117.75
PIO3_10/DP05A	F3	E3	16	231.40	2,082.74
PIO3_11/DP05B	F4	F3	17	129.40	2,047.75
GND	A9	M10	18	231.40	2,012.74
PIO3_12/DP06A	F5	G3	19	129.40	1,977.75
PIO3_13/DP06B	E5	H3	20	231.40	1,942.74
GND	A9	J3	21	129.40	1,907.75
GND	—	—	22	231.40	1,872.74
PIO3_14/DP07A	—	H1	23	129.40	1,837.75
PIO3_15/DP07B	—	J1	24	231.40	1,802.74
VCCIO_3	K1	K3	25	129.40	1,767.75
VCC	G6	L10	26	231.40	1,732.74
PIO3_16/DP08A	—	K1	27	129.40	1,697.75
PIO3_17/DP08B	—	L1	28	231.40	1,662.74
PIO3_18/DP09A	G2	L3	29	129.40	1,627.75
GBIN7/PIO3_19/DP09B	G1	L5	30	231.40	1,592.74
VCCIO_3	J6	N10	31	129.40	1,557.75

iCE65P04 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIOS_00/SPI_SO	M11	T15	124	2,690.00	37.20
PIOS_01/SPI_SI	P11	V15	125	2,740.00	139.20
GND	P6	Y16	126	2,790.00	37.20
PIOS_02/SPI_SCK	P12	V16	127	2,840.00	139.20
PIOS_03/SPI_SS_B	P13	V17	128	2,890.00	37.20
SPI_VCC	L11	R15	129	2,990.00	37.20
TDI	M12	T16	130	3,610.80	342.00
TMS	P14	V18	131	3,712.80	392.00
TCK	L12	R16	132	3,610.80	442.00
TDO	N14	U18	133	3,712.80	492.00
TRST_B	M14	T18	134	3,610.80	542.00
PIO1_00	K11	R18	135	3,712.80	592.00
PIO1_01	L13	P16	136	3,610.80	642.00
PIO1_02	K12	P15	137	3,712.80	692.00
PIO1_03	M13	P18	138	3,610.80	727.00
GND	J14	N18	139	3,712.80	762.00
GND	J14	N18	140	3,610.80	797.00
PIO1_04	J10	N16	141	3,712.80	832.00
PIO1_05	L14	N15	142	3,610.80	867.00
VCCIO_1	H14	M18	143	3,712.80	902.00
VCCIO_1	—	—	144	3,610.80	937.00
PIO1_06	J11	M16	145	3,712.80	972.00
PIO1_07	K14	M15	146	3,610.80	1,007.00
PIO1_08	H10	W20	147	3,712.80	1,042.00
PIO1_09	J13	V20	148	3,610.80	1,077.00
PIO1_10	J12	U20	149	3,712.80	1,112.00
VCC	N7	M13	150	3,610.80	1,147.00
VCC	—	—	151	3,712.80	1,182.00
PIO1_11	H13	T22	152	3,610.80	1,217.00
PIO1_12	H12	R22	153	3,712.80	1,252.00
PIO1_13	—	P22	154	3,610.80	1,287.00
PIO1_14	—	N22	155	3,712.80	1,322.00
PIO1_15	G13	T20	156	3,610.80	1,357.00
PIO1_16	H11	R20	157	3,712.80	1,392.00
PIO1_17	G14	P20	158	3,610.80	1,427.00
GND	K10	N20	159	3,712.80	1,462.00
GND	—	—	160	3,610.80	1,497.00
PIO1_18	G10	M20	161	3,712.80	1,532.00
GBIN3/PIO1_19	G12	K18	162	3,610.80	1,567.00
GBIN2/PIO1_20	F10	L18	163	3,712.80	1,602.00
PIO1_21	F14	K20	164	3,610.80	1,637.00
VCCIO_1	H14	J20	165	3,712.80	1,672.00
VCCIO_1	—	—	166	3,610.80	1,707.00
PIO1_22	F13	H20	167	3,712.80	1,742.00
PIO1_23	D13	G20	168	3,610.80	1,777.00
PIO1_24	G11	F20	169	3,712.80	1,812.00

I/O Characteristics

Table 52: **PIO Pin Electrical Characteristics**

Symbol	Description	Conditions	Minimum	Nominal	Maximum	Units
I_I	Input pin leakage current	V_{IN} = $VCCIO_{max}$ to 0 V			±10	µA
I_{OZ}	Three-state I/O pin (Hi-Z) leakage current	V_O = $VCCIO_{max}$ to 0 V			±10	µA
C_{PIO}	PIO pin input capacitance			6		pF
C_{GBIN}	GBIN global buffer pin input capacitance			6		pF
R_{PULLUP}	Internal PIO pull-up resistance during configuration	VCCIO = 3.3V		40		kΩ
		VCCIO = 2.5V		50		kΩ
		VCCIO = 1.8V		90		kΩ
		VCCIO = 1.5V				kΩ
		VCCIO = 1.2V				kΩ
V_{HYST}	Input hysteresis	VCCIO = 1.5V to 3.3V		50		mV

NOTE: All characteristics are characterized and may or may not be tested on each pin on each device.

Single-ended I/O Characteristics

Table 53: **I/O Characteristics (I/O Banks 0, 1, 2 and SPI only)**

I/O Standard	Nominal I/O Bank Supply Voltage	Input Voltage (V)		Output Voltage (V)		Output Current at Voltage (mA)	
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{OL}	I_{OH}
LVCMOS33	3.3V	0.80	2.00	0.4	2.40	8	8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	6	6
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	1.40	4	4
LVCMOS15	1.5V	Not supported: Use I/O Bank 3 and SPI Bank		0.4	1.20	2	2

Table 54: **I/O Characteristics (I/O Bank 3 only)**

I/O Standard	Supply Voltage	Input Voltage (V)		Output Voltage (V)		I/O Attribute Name	mA at Voltage
		Max. V_{IL}	Min. V_{IH}	Max. V_{OL}	Min. V_{OH}		I_{OL}, I_{OH}
LVCMOS33	3.3V	0.80	2.20	0.4	2.40	SL_LVCMOS33_8	±8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	SB_LVCMOS25_16	±16
						SB_LVCMOS25_12	±12
						SB_LVCMOS25_8 *	±8
						SB_LVCMOS25_4	±4
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_LVCMOS18_10	±10
						SB_LVCMOS18_8	±8
						SB_LVCMOS18_4 *	±4
						SB_LVCMOS18_2	±2
LVCMOS15	1.5V	35% VCCIO	65% VCCIO	25% VCCIO	75% VCCIO	SB_LVCMOS15_4	±4
						SB_LVCMOS15_2 *	±2
MDDR	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_MDDR10	±10
						SB_MDDR8	±8
						SB_MDDR4 *	±4
						SB_MDDR2	±2
SSTL2 (Class 2)	2.5V	VREF–0.180	VREF+0.180	0.35	VTT+0.430	SB_SSTL2_CLASS_2	±16.2
SSTL2 (Class 1)				0.54		SB_SSTL2_CLASS_1	±8.1
SSTL18 (Full)	1.8V	VREF–0.125	VREF+0.125	0.28	VTT+0.280	SB_SSTL18_FULL	±13.4
SSTL18 (Half)				VTT–0.475	VTT+0.475	SB_SSTL18_HALF	±6.7

NOTES:
SSTL2 and SSTL18 I/O standards require the VREF input pin, which is only available on the CB284 package and for die-based products.

AC Timing Guidelines

The following examples provide some guidelines of device performance. The actual performance depends on the specific application and how it is physically implemented in the iCE65P FPGA using the SiliconBlue iCEcube software. The following guidelines assume typical conditions (VCC = 1.0 V or 1.2 V as specified, temperature = 25 °C). Apply derating factors using the iCEcube timing analyzer to adjust to other operating regimes.

Programmable Logic Block (PLB) Timing

Table 57 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 46 and Figure 47.

Figure 46 **PLB Sequential Timing Circuit**

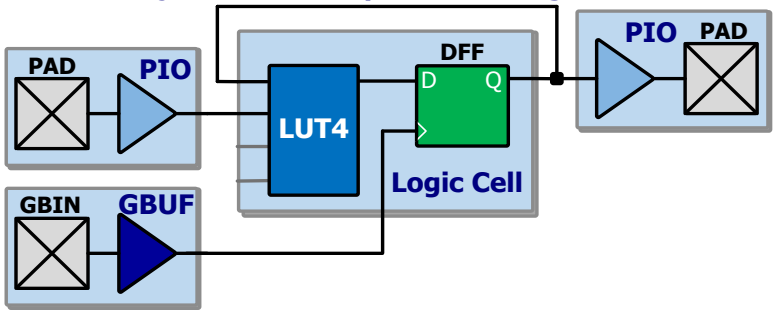


Figure 47 **PLB Combinational Timing Circuit**

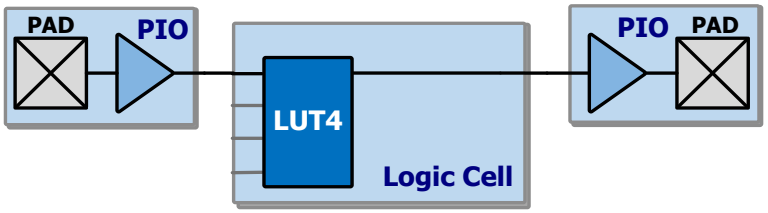


Table 57: **Typical Programmable Logic Block (PLB) Timing**

Symbol	From	To	Description	Power/Speed Grade: –T Nominal VCC: 1.2 V Typ.	Units
Sequential Logic Paths					
F_{TOGGLE}	GBIN input	GBIN input	Flip-flop toggle frequency. DFF flip-flop output fed back to LUT4 input with 4-input XOR, clocked on same clock edge	256	MHz
t_{CKO}	DFF clock input	PIO output	Logic cell flip-flop (DFF) clock-to-output time, measured from the DFF CLK input to PIO output, including interconnect delay.	7.1	ns
t_{GBCKLC}	GBIN input	DFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the logic cell DFF flip-flop.	2.7	ns
t_{SULI}	PIO input	GBIN input	Minimum setup time on PIO input, through LUT4, to DFF flip-flop D-input before active clock edge on the GBIN input, including interconnect delay.	1.2	ns
t_{HDLI}	GBIN input	PIO input	Minimum hold time on PIO input, through LUT4, to DFF flip-flop D-input after active clock edge on the GBIN input, including interconnect delay.	0	ns
Combinational Logic Paths					
t_{LUT4IN}	PIO input	LUT4 input	Asynchronous delay from PIO input pad to adjacent PLB interconnect.	3.3	ns
t_{ILO}	LUT4 input	LUT4 output	Logic cell LUT4 combinational logic propagation delay, regardless of logic complexity from input to output.	0.62	ns
t_{LUT4IN}	LUT4 output	PIO output	Asynchronous delay from adjacent PLB interconnect to PIO output pad.	6.6	ns

Programmable Input/Output (PIO) Block

Table 58 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 48 and Figure 49. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

Figure 48: **Programmable I/O (PIO) Pad-to-Pad Timing Circuit**

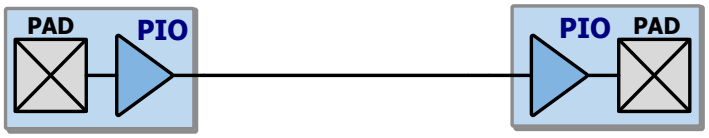


Figure 49: **Programmable I/O (PIO) Sequential Timing Circuit**

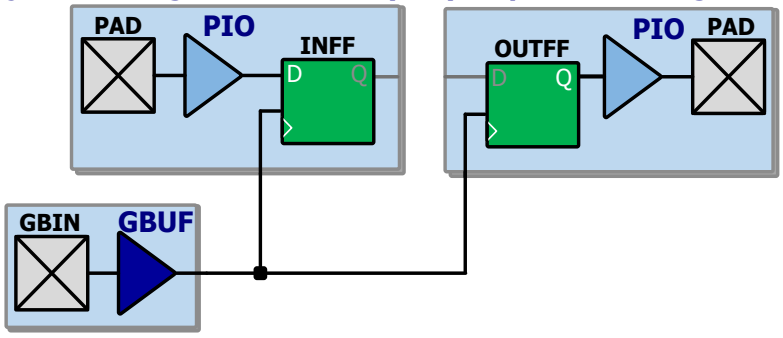


Table 58: **Typical Programmable Input/Output (PIO) Timing (LVCMOS25)**

Symbol	From	To	*Power/Speed Grad* / *Nominal VCC* / Description	–T / 1.2 V / Typ.	Units
Synchronous Output Paths					
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.6	ns
Synchronous Input Paths					
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.8	ns
Pad to Pad					
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	3.2	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	6.2	ns

RAM4K Block

Table 59 provides timing information for the logic in a RAM4K block, which includes the paths shown in Figure 50.

Figure 50: **RAM4K Timing Circuit**

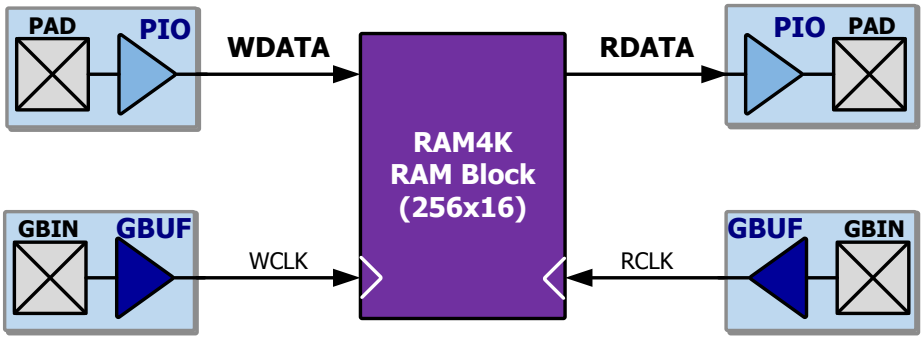


Table 59: **Typical RAM4K Block Timing**

Symbol	From	To	Description	Power/Speed Grade: –T Nominal VCC: 1.2 V Typ.	Units
Write Setup/Hold Time					
t_{SUWD}	PIO input	GBIN input	Minimum write data setup time on PIO inputs before active clock edge on GBIN input, include interconnect delay.	0.8	ns
t_{HDWD}	GBIN input	PIO input	Minimum write data hold time on PIO inputs after active clock edge on GBIN input, including interconnect delay.	0	ns
Read Clock-Output-Time					
t_{CKORD}	RCLK clock input	PIO output	Clock-to-output delay from RCLK input pin, through RAM4K RDATA output flip-flop to PIO output pad, including interconnect delay.	7.3	ns
t_{GBCKRM}	GBIN input	RCLK clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to the RCLK clock input.	2.6	ns
Write and Read Clock Characteristics					
t_{RMWCKH}	WCLK RCLK	WCLK RCLK	Write clock High time	0.54	ns
t_{RMWCKL}			Write clock Low time	0.63	ns
t_{RMWCYC}			Write clock cycle time	1.27	ns
F_{WMAX}			Sustained write clock frequency	256	MHz

Phase-Locked Loop (PLL) Block

Table 59 provides timing information for the Phase-Locked Loop (PLL) block shown in Figure 50.

Figure 51: **Phase-Locked Loop (PLL)**

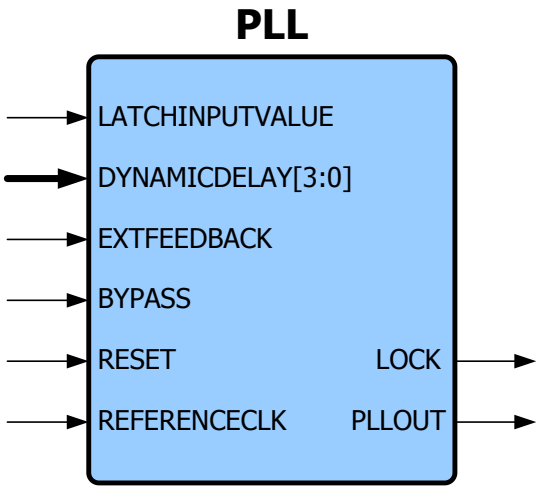


Table 60: **Phase-Locked Loop (PLL) Block Timing**

Symbol	From	To	Description	Power/Speed Grade: –T Nominal VCC: 1.2 V Min.	Typical	Max.	Units
Frequency Range							
F_{REF}			Input clock frequency range	10	—	133	MHz
F_{OUT}			Output clock frequency range (cannot exceed maximum frequency supported by global buffers)	10	—	533	MHz
Duty Cycle							
PLL_{IJ}			Input duty cycle	35	—	65	%
Tw_{HI}			Input clock high time	2.5	—	—	ns
Tw_{LOW}			Input clock low time	2.5	—	—	ns
PLL_{OJD}			Output duty cycle (divided frequency)	45	—	55	%
PLL_{OJM}			Output duty cycle (undivided frequency)	40	—	60	%
Fine Delay							
t_{FDTAP}			Fine delay adjustment, per tap		165		ps
PLL_{TAPS}			Fine delay adjustment settings	0	—	15	taps
PLL_{FDAM}			Maximum delay adjustment		2.5		ns
Jitter							
PLL_{IPJ}			Input clock period jitter	—	—	+/- 300	ps
PLL_{OPJ}			PLLOUT output period jitter	—	1% or ≤ 100	+/- 1.1% output period or ≥ 110	ps
Lock/Reset Time							
t_{LOCK}			PLL lock time after receive stable, monotonic REFERENCECLK input	—	—	50	µs
tw_{RST}			Minimum reset pulse width	20	—	—	ns

Notes:

1. Output jitter performance is affected by input jitter. A clean reference clock < 100ps jitter must be used to ensure best jitter performance.
2. The output jitter specification refers to the intrinsic jitter of the PLL.