Toshiba Semiconductor and Storage - TMPM061FWFG(C,OHZ) Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LCD, LVD, WDT
Number of I/O	64
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/toshiba-semiconductor-and-storage/tmpm061fwfg-c-ohz

Table 1-1 Pin Names and Functions Sorted by Pin (2/6)

Type	Pin No.	Pin Name	Input/ Out-put	Function
Function	18	PI0 TXD2 IROUT2	I/O O O	I/O port Sending serial data Sending serial data with carrier pulse (note) While $\overline{\text{RESET}}$ pin is "Low", keep PI0 pin from being set to "Low".
Function	19	PI1 RXD2	I/O I	I/O port Receiving serial data
Function	20	PI2 SCLK2 $\overline{\text{CTS2}}$ T16A2OUT	I/O I/O I O	I/O port Serial clock input/ output Handshake input pin Timer 16A output
Function	21	PI3 TB0IN	I/O I	I/O port Inputting the timer B capture trigger
PS	22	COUT	−	Regulator output pin Connect a 1μF capacitor to between COUT and RVSS.
PS	23	RVSS	−	GND pin
PS	24	RVDD3	−	Power supply pin (note 3)
Function	25	PI4 TXD30	I/O O	I/O port Sending serial data
Function	26	PI5 RXD30	I/O I	I/O port (5V tolerant input) (note 7) Receiving serial data
Function	27	PI6 SCLK30 $\overline{\text{CTS30}}$ T16A5OUT	I/O I/O I O	I/O port (5V tolerant input) (note 7) Serial clock input/ output Handshake input pin Timer 16A output
Function	28	PJ0 SDA0 SO0 $\overline{\text{BOOT}}$	I/O I/O I/O I	I/O port I2C mode: data pin SIO mode: data pin Setting a single boot mode: (note) TMPM061FWFG goes into single boot mode by sampling "Low" at the rise of a $\overline{\text{RESET}}$ signal.
Function	29	PJ1 SCL0 SI0	I/O I/O I/O	I/O port I2C mode: clock pin SIO mode: data pin
Function	30	PJ2 SCK0 INT1	I/O I/O I	I/O port (5V tolerant input) (note 7) Inputting and outputting a clock if the serial bus interface operates in the SIO mode. External interrupt pin
Function	31	PJ3 RTCOUT	I/O O	I/O port RTC output
Function	32	PJ4 T16A3OUT SCOUT	I/O O O	I/O port Timer 16A output System clock output
Function	33	PJ5 TB1IN XTCLKIN	I I I	Input port Inputting the timer B capture trigger Low-speed clock input pin

Table 1-1 Pin Names and Functions Sorted by Pin (6/6)

Type	Pin No.	Pin Name	Input/ Out-put	Function
PS	97	SRVDD	−	Supplying the voltage reference circuit with a power supply. (note 6)
Function	98	PF0 AIN0	I/O I	I/O port 10bit AD converter analog input
Function	99	PF1 AIN1 INT0	I/O I I	I/O port 10bit AD converter analog input External interrupt pin
PS	100	AVSS	−	10bit AD converter: GND pin (note 2)

Note 1: AVDD3 and VREH must be connected to power supply even if 10bit AD converter is not used.

Note 2: AVSS must be connected to GND even if the 10bit AD converter is not used.

Note 3: The same voltage must be supplied to DVDD3, AVDD3, RVDD3, DSRVDD3, SRVDD, VLC.

Note 4: When 24bit ΔΣAD converter is used, provide pin treatments as follows:

- Do not connect VREFINx to a reference voltage.
- Connect AGNDREFx to DVSS level.
- Connect a 1μF capacitor to between VREFINx and AGNDREFx.

Note 5: When 24bit ΔΣAD converter is not used, below settings are required.

- Connect AGNDREFx to DVSS level.

Note 6: When a temperature sensor is also not used, a reference voltage circuit requires below settings.

- Connect DSRVDD3 and SRVDD to DVDD3.
- Connect DSRVSS to DVSS.

Note 7: Only when input is enabled, these pins tolerate 5V inputs.
Note that these pins cannot be pulled up over the power supply voltage when using as open-drain output.

1.5 Pin Numbers and Power Supply Pins

Table 1-2 Pin Numbers and Power Supplies

Power supply	Voltage range	Pin No.	Pin name
AVDD3	1.8 to 3.6V	2	1 to 2 pin, 98 to 100 pin
DVDD3		8, 74	3 to 82 pin
SRVDD		97	95 to 97 pin
VREFIN0	-	86	83 to 86 pin
VREFIN1		90	87 to 90 pin
VREFIN2		94	91 to 94 pin

4.3 Address lists of peripheral functions

Base addresses of the peripheral functions are shown below. Be careful of which area of SFR0 or SFR1 the peripheral function is allocated.

Do not access to addresses in the SFR area except control registers. For details of control registers, refer to Chapter of each peripheral functions.

Peripheral Function		Base Address	Area
Clock/Mode control (CG)		0x400F_3000	SFR0
Input/Output Ports	PORTA	0x400C_0000	SFR0
	PORTB	0x400C_0100	SFR0
	PORTC	0x400C_0200	SFR0
	PORTD	0x400C_0300	SFR0
	PORTE	0x400C_0400	SFR0
	PORTF	0x400C_0500	SFR0
	PORTG	0x440C_0600	SFR1
	PORTH	0x400C_0700	SFR0
	PORTI	0x400C_0800	SFR0
	PORTJ	0x400C_0900	SFR0
	PORTK	0x400C_0A00	SFR0
16-bit Timer/Event Counters (TMRB)	ch0	0x400C_4000	SFR0
	ch1	0x440C_4100	SFR1
16-bit Timer A (TMR16A)	ch0	0x4008_D000	SFR0
	ch1	0x4008_E000	SFR0
	ch2	0x4008_F000	SFR0
	ch3	0x4009_0000	SFR0
	ch4	0x4009_1000	SFR0
	ch5	0x4409_2000	SFR1
	ch6	0x4409_3000	SFR1
Serial Channel (SIO/SIO)	ch0	0x400E_1000	SFR0
	ch1	0x400E_1100	SFR0
	ch2	0x400E_1200	SFR0
	ch3	0x400E_1300	SFR0
Serial Bus Interface (I2C/SIO)		0x400E_0000	SFR0
Analog/Digital Converter (ADC)		0x400F_C000	SFR0
ΔΣAnalg/Digital Converter (DSADC)	unit0	0x4406_7000	SFR1
	unit1	0x4406_8000	SFR1
	unit2	0x4406_9000	SFR1
Temperature sensor (TEMP)		0x4005_D000	SFR0
Real Time Clock (RTC)		0x400C_C000	SFR0
LCD Driver (LCD)		0x4006_E000	SFR0
Voltage Detector (LVD)		0x400F_4000	SFR0
Watch Dog Timer (WDT)		0x400F_2000	SFR0
Flash / Debug (FC)		0x41FF_F000	SFR0

Bit	Bit Symbol	Type	Function
17	OSCSEL	R/W	High-speed oscillator 0: internal (f_{IHOSC}) 1: external (f_{EHOSC}) The high-speed oscillator is changed between internal and external. Stopping the internal oscillator after switching to the external oscillator can reduce the power consumption.
16	XEN2	R/W	Internal high-speed oscillator operation (Note 3) 0: Stop 1: Oscillation
15-14	WUPTL[1:0]	R/W	Warm-up counter setup value (Note 1) If high-speed oscillator is selected, <WUODR[1:0]> is set "00".
13-12	−	R/W	Write "0".
11	EHCLKEN	R/W	External high-speed clock input enable 0: Disable 1: Enable
10	LOSCSEL	R/W	Low-speed clock 0: Low-speed oscillator (f_{ELOSC}) 1: Low-speed clock ($f_{ELCLKIN}$)
9	XTEN	R/W	External low-speed oscillator mode 0: Stop 1: Oscillation
8	XEN1	R/W	External high-speed oscillator mode 0: Stop 1: Oscillation
7-4	−	R/W	Write "0011"
3	WUPSEL1	R/W	Warm-up clock 0: High-speed clock 1: Low-speed clock Select source clock for warm-up timer. High-speed clock is followed by <WUPSEL2>. Low-speed clock is selected by CGOSCCR<LOSCSEL>.
2	−	R/W	Write "0".
1	WUEF	R	Operation of warm-up timer (WUP) for oscillator 0: WUP finish 1: WUP active Enables to monitor the status of the warm-up timer.
0	WUEON	W	Operation of warm-up timer (WUP) for oscillator 0: don't care 1: WUP start Enables to start the warm-up timer. Read as 0.

Note 1: Refer to Section "6.3.4 Warm-up function" about the Warm-up setup.

Note 2: the external high-speed clock input ($f_{EHCLKIN}$) cannot be used as warm-up clock.

Note 3: When using internal high-speed oscillator (IHOSC), do not use it as system clock which high accuracy assurance is required.

7.6.2.10 Application Interrupt and Reset Control Register

	31	30	29	28	27	26	25	24
bit symbol	VECTKEY/VECTKEYSTAT							
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	VECTKEY/VECTKEYSTAT							
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	ENDIANESS	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	-	-	-	-	-	SYSRESET REQ	VECTCLR ACTIVE	-
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-16	VECTKEY (Write)/ VECTKEY-STAT(Read)	R/W	Register key [Write] Writing to this register requires 0x5FA in the <VECTKEY> field. [Read] Read as 0xFA05.
15	ENDIANESS	R/W	Endianness bit:(Note1) 1: big endian 0: little endian
14-3	−	R	Read as 0.
2	SYSRESET REQ	R/W	System Reset Request. 1=CPU outputs a SYSRESETREQ signal. (note2)
1	VECTCLR ACTIVE	R/W	Clear active vector bit 1: clear all state information for active NMI, fault, and interrupts 0: do not clear. This bit self-clears. It is the responsibility of the application to reinitialize the stack.
0	−	R	Read as 0.

Note 1: This product can be used as the little-endian memory format only.

Note 2: When SYSRESETREQ is output, reset is performed on this product. <SYSRESETREQ> is cleared by reset.

7.6.2.11 System Handler Priority Register

The following shows the addresses of the System Handler Priority Registers corresponding to each exception.

	31 24	23 16	15 8	7 0
0xE000_ED1C	PRI_11 (SVCall)	PRI_10	PRI_9	PRI_8
0xE000_ED20	PRI_15 (SysTick)	PRI_14 (PendSV)	PRI_13	PRI_12

Cortex-M0 core uses two bits for assigning a priority.

The following shows the fields of the System Handler Priority Registers for Memory Management, Bus Fault and Usage Fault. Unused bits return "0" when read, and writing to unused bits has no effect.

8.6.4.5 Port E Setting

Pin name	Port Type	Function	Pin name	PE CR	PE FRn	PE OD	PE PUP	PE PDN	PE IE
PE0	FT10	SEG32 (Output)		0	PE0 FR1	0	0	0	0
PE1	FT10	SEG33 (Output)		0	PE1 FR1	0	0	0	0
PE2	FT10	SEG34 (Output)		0	PE2 FR1	0	0	0	0
	FT1	T16A6OUT (Output)		1	PE2 FR2	x	x	x	0
PE3	FT10	SEG35 (Output)		0	PE3 FR1	0	0	0	0
	FT1	SCLK31 (Input)		0	PE3 FR2	x	x	x	1
		SCLK31 (Output)		1	PE3 FR2	x	x	x	0
	FT1	$\overline{\text{CTS31}}$ (Output)		1	PE3 FR3	x	x	x	0
PE4	FT10	SEG36 (Output)		0	PE4 FR1	0	0	0	0
	FT1	RXD31 (Input)		0	PE4 FR2	x	x	x	1
PE5	FT10	SEG37 (Output)		0	PE5 FR1	0	0	0	0
	FT1	TXD31 (Input)		1	PE5 FR2	x	x	x	0
PE6	FT10	SEG38 (Output)		0	PE6 FR1	0	0	0	0
	FT2	SWCLK (Input)	o	0	PE6 FR2	0	0	1	1
PE7	FT10	SEG39 (Output)		0	PE7 FR1	0	0	0	0
	FT2	SWDIO (I/O)	o	1	PE7 FR2	0	1	0	1

9.3.12 TBxCP0 (Capture register 0)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	TBCP0							
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
	7	6	5	4	3	2	1	0
bit symbol	TBCP0							
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit	Bit Symbol	Type	Function
31-16	−	R	Read as "0".
15-0	TBCP0[15:0]	R	A value captured from the up-counter is read.

9.3.13 TBxCP1 (Capture register 1)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	TBCP1							
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
	7	6	5	4	3	2	1	0
bit symbol	TBCP1							
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit	Bit Symbol	Type	Function
31-16	−	R	Read as "0".
15-0	TBCP1[15:0]	R	A value captured from the up-counter is read.

11.3.5 SCxMOD0 (Mode Control Register 0)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	TB8	CTSE	RXE	WU	SM		SC	
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-8	−	R	Read as "0".
7	TB8	R/W	Transmit data bit 8 (For UART) Writes the 9th bit of transmit data in the 9-bit UART mode.
6	CTSE	R/W	Handshake function control (For UART) 0: CTS disabled 1: CTS enabled Controls handshake function. Setting "1" enables handshake function using $\overline{CTS}$ pin.
5	RXE	R/W	Receive control (Note1)(Note2) 0: Disabled 1: Enabled
4	WU	R/W	Wake-up function (For UART) 0: Disabled 1: Enabled This function is available only at 9-bit UART mode. In other mode, this function has no meaning. In it is Enabled, Interrupt only when RB9 = "1" at 9-bit UART mode.
3-2	SM[1:0]	R/W	Specifies transfer mode. 00: I/O interface mode 01: 7-bit length UART mode 10: 8-bit length UART mode 11: 9-bit length UART mode
1-0	SC[1:0]	R/W	Serial transfer clock (For UART) 00: Timer output 01: Baud rate generator 10: Internal clock fsys 11: External clock (SCLK input) (As for the I/O interface mode, the serial transfer clock can be set in the control register (SCxCR).

Note 1: Set <RXE> to "1" after setting each mode register (SCxMOD0, SCxMOD1 and SCxMOD2).

Note 2: Do not stop the receive operation (by setting SCxMOD0<RXE> to "0") when data is being received.

SCxBRADD

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	-	-	-	-	BRK			
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-4	−	R	Read as "0".
3-0	BRK[3:0]	R/W	Specify K for the "N + (16 − K)/16" division (For UART) 0000: Prohibited 0001: K = 1 0010: K = 2 ... 1111: K = 15

Table 11-1 lists the settings of baud rate generator division ratio.

Table 11-1 Setting division ratio

	<BRADDE> = "0"	<BRADDE> = "1" (Note1) (Only UART mode)
<BRS>	Specify "N" (Note2) (Note3)	
<BRK>	No setting required	Specify "K" (Note4)
Division ratio	Divide by N	$N + \frac{(16 - K)}{16}$ division.

Note 1: To use the "N + (16 - K)/16" division function, be sure to set <BRADDE> to "1" after setting the K value to <BRK>. The "N + (16 - K)/16" division function can only be used in the UART mode.

Note 2: As a division ratio, 1 ("0001") or 16 ("0000") can not be applied to N when using the "N + (16 - K)/16" division function in the UART mode.

Note 3: The division ratio "1" of the baud rate generator can be specified only when the double buffering is used in the I/O interface mode.

Note 4: Specifying "K = 0" is prohibited.

12.4 Registers

12.4.1 Register List

The table below shows control registers and their addresses.

For detail of the base address, refer to "Address lists of peripheral functions" of "Memory Map" chapter.

Register name		Address (Base+)
Control register 0	SBIxCR0	0x0000
Control register 1	SBIxCR1	0x0004
Data buffer register	SBIxDBR	0x0008
I2C bus address register	SBIxI2CAR	0x000C
Control register 2	SBIxCR2 (writing)	0x0010
Status register	SBIxSR (reading)	
Baud rate register 0	SBIxBR0	0x0014

12.5 Control Registers in the I2C Bus Mode

The following registers control the serial bus interface in the I2C bus mode and provide its status information for monitoring.

12.5.1 SBIxCR0(Control register 0)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	SBIEN	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-8	-	R	Read as "0".
7	SBIEN	R/W	Serial bus interface operation 0:Disable 1:Enable To use the serial bus interface, enable this bit first. For the first time in case of setting to enable, the relevant SBI registers can be read or written. Since all clocks except SBIxCR0 stop if this bit is disabled, power consumption can be reduced by disabling this bit. If this bit is disabled after it's been enabled once, the settings of each register are retained.
6-0	-	R	Read as "0".

12.5.2 SBIxCR1(Control register 1)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	BC			ACK	-	SCK2	SCK1	SCK0 / SWRMON
After reset	0	0	0	0	1	0	0	1(Note3)

Bit	Bit Symbol	Type	Function
31-8	-	R	Read as 0.

13.3.8 ADMOD5 (Mode Control Register 5)

	31	30	29	28	27	26	25	24
Bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
Bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
Bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
Bit symbol	-	-	ADOBIC1	ADREGS1				ADOBSV1
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-6	−	R	Read as 0.
5	ADOBIC1	R/W	Set the AD monitor function interrupt 1. 0: If the value of the conversion result is smaller than the comparison register 1, an interrupt is generated. 1: If the value of the conversion result is bigger than the comparison register 1, an interrupt is generated.
4-1	ADREGS1[3:0]	R/W	Select a target conversion result register when using the AD monitor function 1 (See the below table).
0	ADOBSV1	R/W	AD monitor function 1 0: Disable 1: Enable

<ADREGS1[3:0]>	Conversion result register to be compared	<ADREGS1[3:0]>	Conversion result register to be compared
0000	ADREG08	0100	ADREG4C
0001	ADREG19	0101	ADREG5D
0010	ADREG2A	0110	ADREG6E
0011	ADREG3B	0111	ADREG7F
−	−	1xxx	ADREGSP

16. Real Time Clock (RTC)

16.1 Function

1. Clock (hour, minute and second)
2. Calendar (month, week, date and leap year)
3. Selectable 12 (am/ pm) and 24 hour display
4. Time adjustment + or − 30 seconds (by software)
5. Alarm function (available only in the products that have $\overline{\text{ALARM}}$ pin.)
6. Alarm interrupt
7. Clock correction function
8. 1 Hz clock output

16.2 Block Diagram

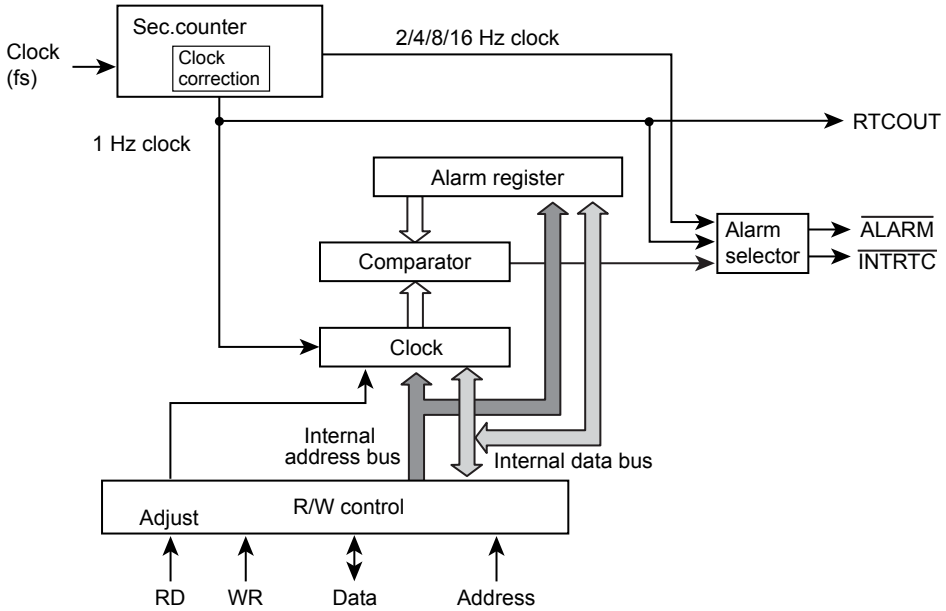


Figure 16-1 Block Diagram

Note 1: Western calendar year column:This product uses only the final two digits of the year. The year following 99 is 00 years. Please take into account the first two digits when handling years in the western calendar.

Note 2: Leap year:A leap year is divisible by 4 excluding a year divisible by 100; the year divisible by 100 is not considered to be a leap year. Any year divisible by 400 is a leap year. This product is considered the year divisible by 4 to be a leap year and does not take into account the above exceptions. It needs adjustments for the exceptions.

16.3.3.3 RTCHOURR (Hour column register(PAGE0/1))

(1) 24-hour clock mode (RTCMONTHR<MO0>= "1")

	7	6	5	4	3	2	1	0
Bit symbol	-	-	HO					
After reset	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit	Bit Symbol	Type	Functon
7-6	−	R	Read as 0.
5-0	HO	R/W	Setting digit register of Hour. 00_0000 : 0 o'clock 01_0000 : 10 o'clock 10_0000 : 20 o'clock 00_0001 : 1 o'clock 01_0001 : 11 o'clock 10_0001 : 21 o'clock 00_0010 : 2 o'clock 01_0010 : 12 o'clock 10_0010 : 22 o'clock 00_0011 : 3 o'clock 01_0011 : 13 o'clock 10_0011 : 23 o'clock 00_0100 : 4 o'clock 01_0100 : 14 o'clock 00_0101 : 5 o'clock 01_0101 : 15 o'clock 00_0110 : 6 o'clock 01_0110 : 16 o'clock 00_0111 : 7 o'clock 01_0111 : 17 o'clock 00_1000 : 8 o'clock 01_1000 : 18 o'clock 00_1001 : 9 o'clock 01_1001 : 19 o'clock 11_1111 : Don't compare Hour at alarm function.

Note: The setting other than listed above is prohibited.

(2) 12-hour clock mode (RTCMONTHR<MO0> = "0")

	7	6	5	4	3	2	1	0
Bit symbol	-	-	HO					
After reset	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit	Bit Symbol	Type	Functon
7-6	−	R	Read as 0.
5-0	HO	R/W	Setting digit register of Hour. (AM) (PM) 00_0000 : 0 o'clock 10_0000 : 0 o'clock 00_0001 : 1 o'clock 10_0001 : 1 o'clock 00_0010 : 2 o'clock 10_0010 : 2 o'clock 00_0011 : 3 o'clock 10_0011 : 3 o'clock 00_0100 : 4 o'clock 10_0100 : 4 o'clock 00_0101 : 5 o'clock 10_0101 : 5 o'clock 00_0110 : 6 o'clock 10_0110 : 6 o'clock 00_0111 : 7 o'clock 10_0111 : 7 o'clock 00_1000 : 8 o'clock 10_1000 : 8 o'clock 00_1001 : 9 o'clock 10_1001 : 9 o'clock 01_0000 : 10 o'clock 11_0000 : 10 o'clock 01_0001 : 11 o'clock 11_0001 : 11 o'clock 11_1111 : Don't compare hour at alarm function.

Note: The setting other than listed above is prohibited.

16.4.3 Entering the Low Power Consumption Mode

To enter SLEEP mode, in which the system clock stops, after changing clock data, adjusting seconds or re-setting the clock, be sure to observe one of the following procedures

1. After changing the clock setting registers, setting the RTCPAGER<ADJUST> bit or setting the RTCRESTR<RSTTMR> bit, wait for one second for an interrupt to be generated.

2. After changing the clock setting registers, setting the RTCPAGER<ADJUST> bit or setting the RTCRESTR<RSTTMR> bit, read the corresponding clock register values, <ADJUST> or <RSTTMR> to make sure that the setting you have made is reflected.

17.2.2.8 LCDBUF04 (Buffer register 04)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	SEG9				SEG8			
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-8	−	R	Read as "0".
7-4	SEG9	R/W	Data of SEG9 Specifies the COM3,COM2,COM1 and COM0 data of SEG9.
3-0	SEG8	R/W	Data of SEG8 Specifies the COM3,COM2,COM1 and COM0 data of SEG8.

17.2.2.9 LCDBUF05 (Buffer register 05)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	SEG11				SEG10			
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-8	−	R	Read as "0".
7-4	SEG11	R/W	Data of SEG11 Specifies the COM3,COM2,COM1 and COM0 data of SEG11.
3-0	SEG10	R/W	Data of SEG10 Specifies the COM3,COM2,COM1 and COM0 data of SEG10.

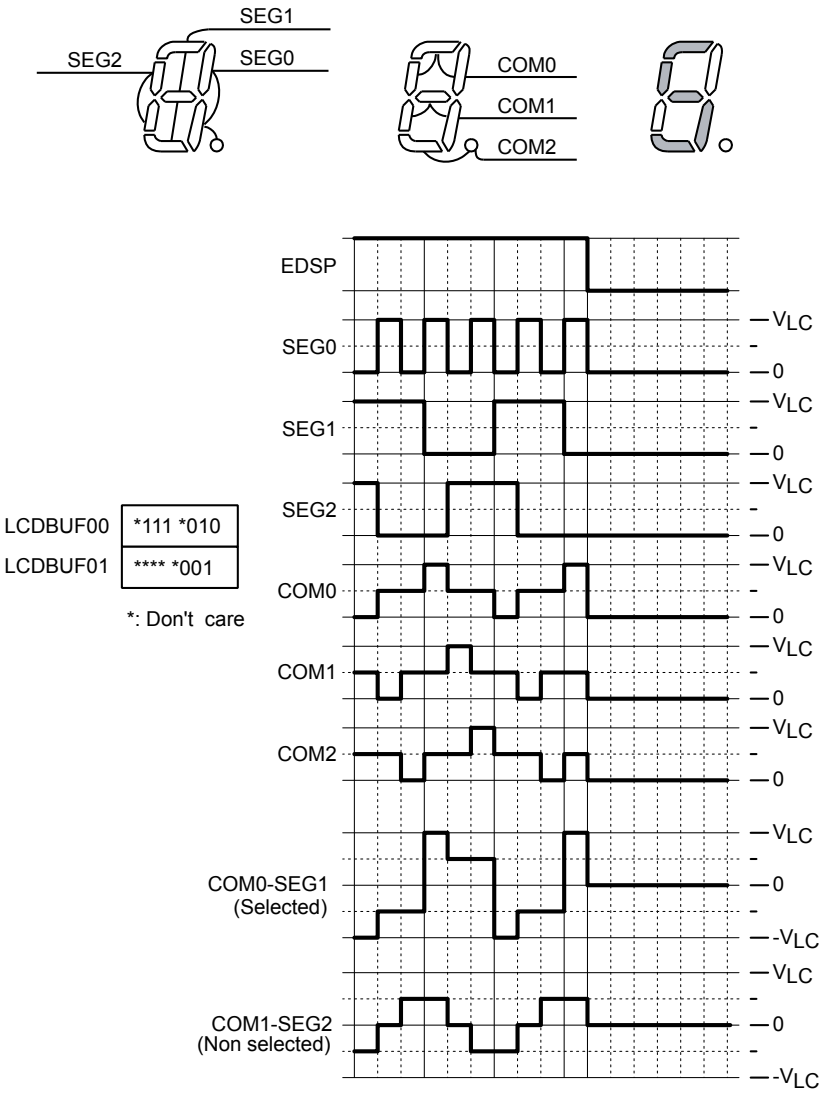


Figure 17-10 1/3 Duty (1/2 Bias) Drive

19.2 Register

19.2.1 Register List

The table below shows control registers and their addresses.

For detail of the base address, refer to "Address lists of peripheral functions" of "Memory Map" chapter.

Register name		Address (Base+)
Watchdog Timer Mode Register	WDMOD	0x0000
Watchdog Timer Control Register	WDCR	0x0004

19.2.2 WDMOD (Watchdog Timer Mode Register)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	WDTE	WDTP			-	I2WDT	RESCR	-
After reset	1	0	0	0	0	0	1	0

Bit	Bit Symbol	Type	Function
31-8	−	R	Read as "0".
7	WDTE	R/W	Enable / Disable control 0:Disable 1: Enable To disable the watchdog timer to protect from the error writing by the malfunction, first <WDTE> is set to "0", and then the disable code (0xB1) must be written to WDCR. To change the status of the watchdog timer from "disable" to "enable", set <WDTE> to "1".
6-4	WDTP[2:0]	R/W	Selects WDT detection time 000: $2^{15}/f_{SYS}$ 100: $2^{23}/f_{SYS}$ 001: $2^{17}/f_{SYS}$ 101: $2^{25}/f_{SYS}$ 010: $2^{19}/f_{SYS}$ 110: Reserved 011: $2^{21}/f_{SYS}$ 111: Reserved
3	−	R	Read as "0"
2	I2WDT	R/W	Operation in IDLE mode 0: Stop 1: Operate
1	RESCR	R/W	Operation after detecting malfunction 0: INTWDT interrupt request is generated. Note) 1: Reset
0	−	R/W	Write "0".

Note: INTWDT interrupt is a factor of the non-mask interrupt.

20.4 Programming in the User Boot Mode

A user Boot mode is to use flash memory programming routine defined by users. It is used when the data transfer buses for flash memory program code on the user application is different from the serial I/O. It operates in the single chip mode; therefore, a switch from normal mode in which user application is activated in the use boot mode to the user boot mode for programming flash is required. Specifically, add a mode judgment routine to the reset service routine in the user application program.

The condition to switch the modes needs to be set according to the user's system setup condition. Also, a flash memory programming routine that the user uniquely makes up needs to be set in the new application. This routine is used for programming after being switched to the user boot mode. The data in built-in Flash memory cannot be read out during erase/reprogramming mode. Thus, reprogramming routine must be take place while it is stored in the area outside of Flash memory area. Once re-programming is complete, it is recommended to protect relevant flash blocks from accidental reprogramming. Be sure not to generate interrupt/fault to avoid abnormal termination during the user boot mode.

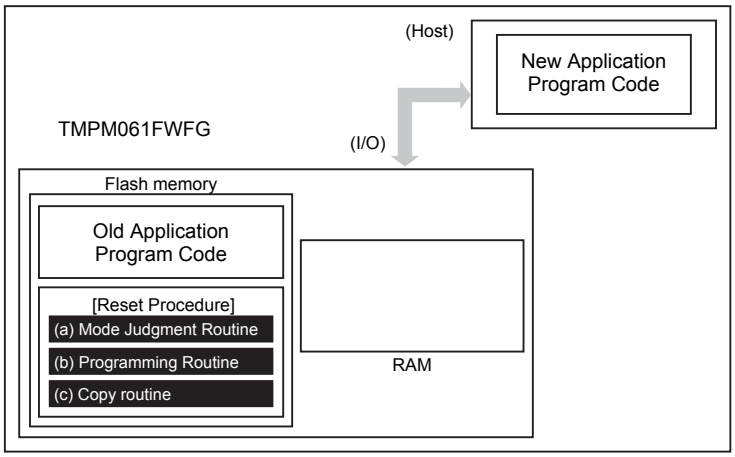
Taking examples from two cases such as the method that reprogramming routine stored in Flash memory (1-A) and transferred from the external device (1-B), the following section explains the procedure. For a detail of the program/erase to Flash memory, refer to "20.2 Detail of Flash Memory".

20.4.1 (1-A) Procedure that a Programming Routine Stored in Flash memory

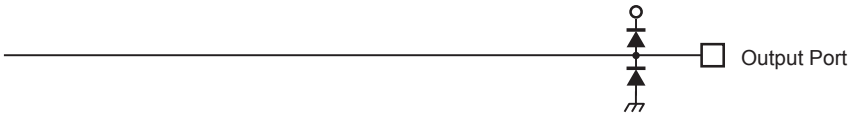
20.4.1.1 Step-1

A user determines the conditions (e.g., pin status) to enter the user boot mode and the I/O bus to be used to transfer data. Then suitable circuit design and program are created. Before installing the device on a printed circuit board, write the following three program routines into an arbitrary flash block using programming equipment such as a flash writer.

(a) Mode determination routine:	A program to determine to switch to user boot mode or not
(b) Flash programming routine:	A program to download new program from the host controller and re-program Flash memory
(c) Copy routine:	A program to copy the data described in (a) to the built-in RAM or external memory device



23.2 Analog pin

COM0, COM1, COM2, COM3	
DAIN0+, DAIN0-, DAIN1+, DAIN1-, DAIN2+, DAIN2-,	

23.3 Control pin

MODE	 Mode pin must be connected to GND.
$\overline{\text{RESET}}$