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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | M8C |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 16 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 5.25V |
| Data Converters | A/D 28x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 20-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21334-24pvxi |

### PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted in Table 1.

**Table 1. PSoC Device Characteristics**

| PSoC Part Number | Digital I/O | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size |
|---|---|---|---|---|---|---|---|---|---|
| CY8C29x66 | up to 64 | 4 | 16 | up to 12 | 4 | 4 | 12 | 2 K | 32 K |
| CY8C28xxx | up to 44 | up to 3 | up to 12 | up to 44 | up to 4 | up to 6 | up to 12 + 4[6] | 1 K | 16 K |
| CY8C27x43 | up to 44 | 2 | 8 | up to 12 | 4 | 4 | 12 | 256 | 16 K |
| CY8C24x94 | up to 56 | 1 | 4 | up to 48 | 2 | 2 | 6 | 1 K | 16 K |
| CY8C24x23A | up to 24 | 1 | 4 | up to 12 | 2 | 2 | 6 | 256 | 4 K |
| CY8C23x33 | up to 26 | 1 | 4 | up to 12 | 2 | 2 | 4 | 256 | 8 K |
| CY8C22x45 | up to 38 | 2 | 8 | up to 38 | 0 | 4 | 6[6] | 1 K | 16 K |
| CY8C21x45 | up to 24 | 1 | 4 | up to 24 | 0 | 4 | 6[6] | 512 | 8 K |
| CY8C21x34 | up to 28 | 1 | 4 | up to 28 | 0 | 2 | 4[6] | 512 | 8 K |
| CY8C21x23 | up to 16 | 1 | 4 | up to 8 | 0 | 2 | 4[6] | 256 | 4 K |
| CY8C20x34 | up to 28 | 0 | 0 | up to 28 | 0 | 0 | 3[6,7] | 512 | 8 K |
| CY8C20xx6 | up to 36 | 0 | 0 | up to 36 | 0 | 0 | 3[6,7] | up to 2 K | up to 32 K |

## Getting Started

For in-depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

### Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

### Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

### Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

### CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

### Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

### Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

**Notes**
6. Limited analog functionality.
7. Two analog blocks and one CapSense®.

## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

### Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

### Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

## 32-pin Part Pinout

**Figure 7. CY8C21434 32-pin PSoC Device**

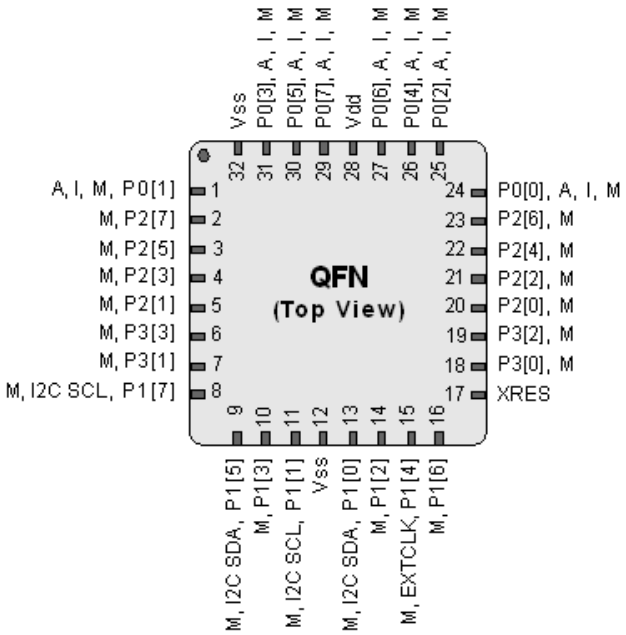



**Figure 7. CY8C21634 32-pin PSoC Device**

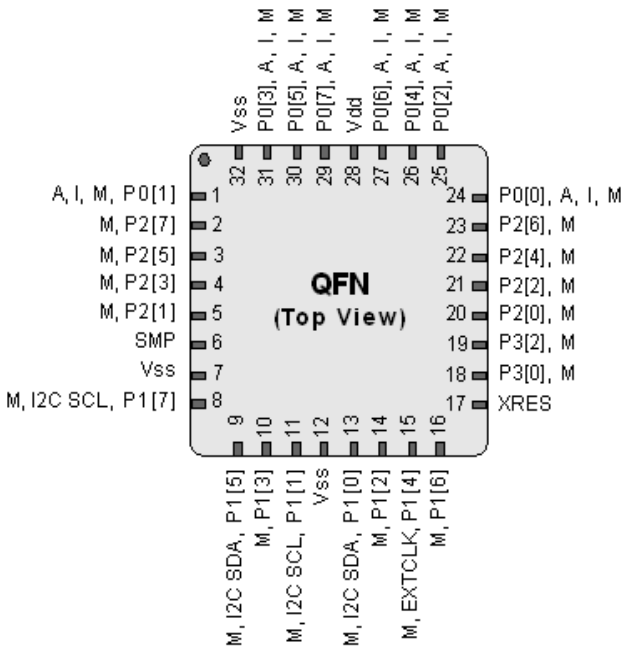



**Figure 8. CY8C21434 32-pin Sawn PSoC Device Sawn**

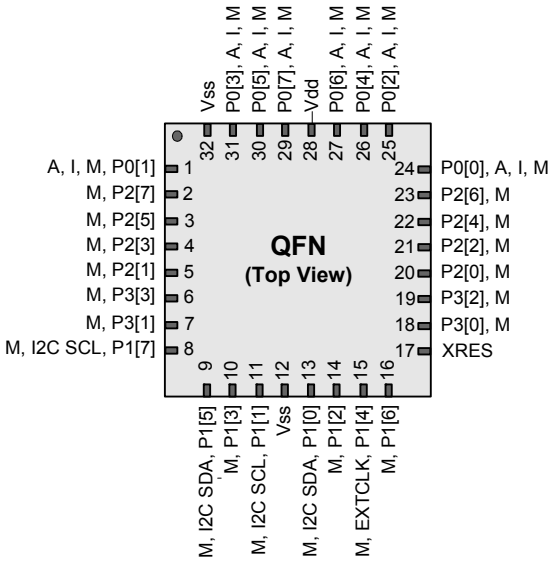
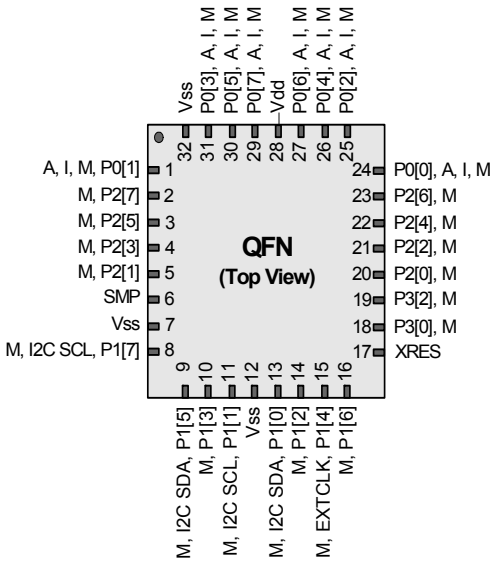



**Figure 9. CY8C21634 32-pin Sawn PSoC Device Sawn**



### CY8C21001 56-pin SSOP Pin Definitions (continued)

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 20 | I/O | | P3[1] | |
| 21 | | | NC | No connection. Pin must be left floating |
| 22 | | | NC | No connection. Pin must be left floating |
| 23 | I/O | | P1[7] | $I^2C$ SCL |
| 24 | I/O | | P1[5] | $I^2C$ SDA |
| 25 | | | NC | No connection. Pin must be left floating |
| 26 | I/O | | P1[3] | $I_{FMTEST}$ |
| 27 | I/O | | P1[1] | $I^2C$ SCL, ISSP-SCLK[19] |
| 28 | Power | | $V_{SS}$ | Ground connection [18] |
| 29 | | | NC | No connection. Pin must be left floating |
| 30 | | | NC | No connection. Pin must be left floating |
| 31 | I/O | | P1[0] | $I^2C$ SDA, ISSP-SDATA[19] |
| 32 | I/O | | P1[2] | $V_{FMTEST}$ |
| 33 | I/O | | P1[4] | Optional external clock input (EXTCLK) |
| 34 | I/O | | P1[6] | |
| 35 | | | NC | No connection. Pin must be left floating |
| 36 | | | NC | No connection. Pin must be left floating |
| 37 | | | NC | No connection. Pin must be left floating |
| 38 | | | NC | No connection. Pin must be left floating |
| 39 | | | NC | No connection. Pin must be left floating |
| 40 | | | NC | No connection. Pin must be left floating |
| 41 | Input | | XRES | Active high external reset with internal pull-down |
| 42 | OCD | | HCLK | OCD high-speed clock output |
| 43 | OCD | | CCLK | OCD CPU clock output |
| 44 | I/O | | P3[0] | |
| 45 | I/O | | P3[2] | |
| 46 | | | NC | No connection. Pin must be left floating |
| 47 | | | NC | No connection. Pin must be left floating |
| 48 | I/O | I | P2[0] | |
| 49 | I/O | I | P2[2] | |
| 50 | I/O | | P2[4] | |
| 51 | I/O | | P2[6] | |
| 52 | I/O | I | P0[0] | Analog column mux input |
| 53 | I/O | I | P0[2] | Analog column mux input and column output |
| 54 | I/O | I | P0[4] | Analog column mux input and column output |
| 55 | I/O | I | P0[6] | Analog column mux input |
| 56 | Power | | $V_{DD}$ | Supply voltage |

**LEGEND**: A = Analog, I = Input, O = Output, and OCD = On-Chip Debug.

**Notes**
18. All $V_{SS}$ pins should be brought out to one common GND plane.
19. These are the ISSP pins, which are not High Z at POR. See the *PSoC Technical Reference Manual* for details.

# Register Reference

This chapter lists the registers of the CY8C21x34 PSoC device. For detailed register information, see the *PSoC Technical Reference Manual*.

## Register Conventions

The register conventions specific to this section are listed in Table 2.

**Table 2. Register Conventions**

| Convention | Description |
|---|---|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

## Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set to 1, the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are reserved and must not be accessed.

**Table 3. Register Map 0 Table: User Space**

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DR | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0GS | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1GS | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | | 87 | | | C7 | |
| PRT2DR | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2IE | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2GS | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2DM2 | 0B | RW | | 4B | | | 8B | | | CB | |
| PRT3DR | 0C | RW | | 4C | | | 8C | | | CC | |
| PRT3IE | 0D | RW | | 4D | | | 8D | | | CD | |
| PRT3GS | 0E | RW | | 4E | | | 8E | | | CE | |
| PRT3DM2 | 0F | RW | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | CUR_PP | D0 | RW |
| | 11 | | | 51 | | | 91 | | STK_PP | D1 | RW |
| | 12 | | | 52 | | | 92 | | | D2 | |
| | 13 | | | 53 | | | 93 | | IDX_PP | D3 | RW |
| | 14 | | | 54 | | | 94 | | MVR_PP | D4 | RW |
| | 15 | | | 55 | | | 95 | | MVW_PP | D5 | RW |
| | 16 | | | 56 | | | 96 | | I2C_CFG | D6 | RW |
| | 17 | | | 57 | | | 97 | | I2C_SCR | D7 | # |
| | 18 | | | 58 | | | 98 | | I2C_DR | D8 | RW |
| | 19 | | | 59 | | | 99 | | I2C_MSCR | D9 | # |
| | 1A | | | 5A | | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | | 5B | | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | | 5E | | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | | 5F | | | 9F | | | DF | |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | AMUXCFG | 61 | RW | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | PWM_CR | 62 | RW | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | | 63 | | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | | E4 | |
| DBB01DR1 | 25 | W | | 65 | | | A5 | | | E5 | |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | ADC0_CR | 68 | # | | A8 | | | E8 | |
| DCB02DR1 | 29 | W | ADC1_CR | 69 | # | | A9 | | | E9 | |
| DCB02DR2 | 2A | RW | | 6A | | | AA | | | EA | |
| DCB02CR0 | 2B | # | | 6B | | | AB | | | EB | |
| DCB03DR0 | 2C | # | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03DR1 | 2D | W | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03DR2 | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| DCB03CR0 | 2F | # | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACE01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | DAC_D | FD | RW |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are reserved and must not be accessed. # Access is bit specific.

*DC General-Purpose I/O Specifications*

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

**Table 6. 5-V and 3.3-V DC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | 4 | 5.6 | 8 | kΩ | |
| $R_{PD}$ | Pull-down resistor | 4 | 5.6 | 8 | kΩ | |
| $V_{OH}$ | High output level | $V_{DD}$ – 1.0 | – | – | V | $I_{OH}$ = 10 mA, $V_{DD}$ = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]) |
| $V_{OL}$ | Low output level | – | – | 0.75 | V | $I_{OL}$ = 25 mA, $V_{DD}$ = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])) |
| $I_{OH}$ | High level source current | 10 | – | – | mA | $V_{OH}$ = $V_{DD}$ – 1.0 V, see the limitations of the total current in the note for $V_{OH}$ |
| $I_{OL}$ | Low level sink current | 25 | – | – | mA | $V_{OL}$ = 0.75 V, see the limitations of the total current in the note for $V_{OL}$ |
| $V_{IL}$ | Input low level | – | – | 0.8 | V | $V_{DD}$ = 3.0 to 5.25 |
| $V_{IH}$ | Input high level | 2.1 | – | | V | $V_{DD}$ = 3.0 to 5.25 |
| $V_H$ | Input hysteresis | – | 60 | – | mV | |
| $I_{IL}$ | Input leakage (absolute value) | – | 1 | – | nA | Gross tested to 1 µA |
| $C_{IN}$ | Capacitive load on pins as input | – | 3.5 | 10 | pF | Package and pin dependent Temp = 25 °C |
| $C_{OUT}$ | Capacitive load on pins as output | – | 3.5 | 10 | pF | Package and pin dependent Temp = 25 °C |

**Table 7. 2.7-V DC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up resistor | 4 | 5.6 | 8 | kΩ | |
| $R_{PD}$ | Pull-down resistor | 4 | 5.6 | 8 | kΩ | |
| $V_{OH}$ | High output level | $V_{DD}$ – 0.4 | – | – | V | $I_{OH}$ = 2.5 mA (6.25 Typ), $V_{DD}$ = 2.4 to 3.0 V (16 mA maximum, 50 mA Typ combined $I_{OH}$ budget) |
| $V_{OL}$ | Low output level | – | – | 0.75 | V | $I_{OL}$ = 10 mA, $V_{DD}$ = 2.4 to 3.0 V (90 mA maximum combined $I_{OL}$ budget) |
| $I_{OH}$ | High level source current | 2.5 | – | – | mA | $V_{OH}$ = $V_{DD}$ – 0.4 V, see the limitations of the total current in the note for $V_{OH}$ |
| $I_{OL}$ | Low level sink current | 10 | – | – | mA | $V_{OL}$ = 0.75 V, see the limitations of the total current in the note for $V_{OL}$ |
| $V_{IL}$ | Input low level | – | – | 0.75 | V | $V_{DD}$ = 2.4 to 3.0 |
| $V_{IH}$ | Input high level | 2.0 | – | – | V | $V_{DD}$ = 2.4 to 3.0 |
| $V_H$ | Input hysteresis | – | 90 | – | mV | |
| $I_{IL}$ | Input leakage (absolute value) | – | 1 | – | nA | Gross tested to 1 µA |
| $C_{IN}$ | Capacitive load on pins as input | – | 3.5 | 10 | pF | Package and pin dependent Temp = 25 °C |
| $C_{OUT}$ | Capacitive load on pins as output | – | 3.5 | 10 | pF | Package and pin dependent Temp = 25 °C |

## AC Electrical Characteristics

*AC Chip-Level Specifications*

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 16. 5-V and 3.3-V AC Chip-Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{IMO24}$ [28] | IMO frequency for 24 MHz | 23.4 | 24 | 24.6[29,30] | MHz | Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 14 on page 20. SLIMO mode = 0 |
| $F_{IMO6}$ [28] | IMO frequency for 6 MHz | 5.52 | 6 | 6.48 [29,30] | MHz | Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 14 on page 20. SLIMO mode = 1 |
| $F_{CPU1}$ | CPU frequency (5 V nominal) | 0.091 | 24 | 24.6[29] | MHz | 24 MHz only for SLIMO mode = 0 |
| $F_{CPU2}$ | CPU frequency (3.3 V nominal) | 0.091 | 12 | 12.3[30] | MHz | SLIMO mode = 0 |
| $F_{BLK5}$ | Digital PSoC block frequency (5 V nominal) | 0 | 48 | 49.2[29,31] | MHz | Refer to AC Digital Block Specifications on page 29 |
| $F_{BLK33}$ | Digital PSoC block frequency (3.3 V nominal) | 0 | 24 | 24.6[31] | MHz | |
| $F_{32K1}$ | ILO frequency | 15 | 32 | 64 | kHz | |
| $F_{32K\_U}$ | ILO untrimmed frequency | 5 | – | 100 | kHz | After a reset and before the M8C starts to run, the ILO is not trimmed. See the system resets section of the *PSoC Technical Reference Manual* for details on this timing |
| $t_{XRST}$ | External reset pulse width | 10 | – | – | µs | |
| DC24M | 24 MHz duty cycle | 40 | 50 | 60 | % | |
| $DC_{ILO}$ | ILO duty cycle | 20 | 50 | 80 | % | |
| Step24M | 24 MHz trim step size | – | 50 | – | kHz | |
| Fout48M | 48 MHz output frequency | 46.8 | 48.0 | 49.2[29,30] | MHz | Trimmed. Using factory trim values |
| $F_{MAX}$ | Maximum frequency of signal on row input or row output. | – | – | 12.3 | MHz | |
| $SR_{POWER\_UP}$ | Power supply slew rate | – | – | 250 | V/ms | $V_{DD}$ slew rate during power-up |
| $t_{POWERUP}$ | Time from end of POR to CPU executing code | – | 16 | 100 | ms | Power-up from 0 V. See the System Resets section of the *PSoC Technical Reference Manual* |
| $t_{jit\_IMO}$ | 24-MHz IMO cycle-to-cycle jitter (RMS)[32] | – | 200 | 700 | ps | |
| | 24-MHz IMO long term N cycle-to-cycle jitter (RMS)[32] | – | 300 | 900 | ps | N = 32 |
| | 24-MHz IMO period jitter (RMS)[32] | – | 100 | 400 | ps | |

**Notes**
28. Errata: The worst case IMO frequency deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
29. 4.75 V < $V_{DD}$ < 5.25 V.
30. 3.0 V < $V_{DD}$ < 3.6 V. See application note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3 V.
31. See the individual user module datasheets for information on maximum frequencies for user modules.
32. Refer to Cypress Jitter Specifications Application Note AN5054 “Understanding Datasheet Jitter Specifications for Cypress Timing Products” at www.cypress.com under Application Notes for more information.

**Table 17. 2.7-V AC Chip-Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{IMO12}$ [33] | IMO frequency for 12 MHz | 11.04 | 12 | 12.96 [34, 35] | MHz | Trimmed for 2.7 V operation using factory trim values. See Figure 14 on page 20. SLIMO mode = 1 |
| $F_{IMO6}$ [33] | IMO frequency for 6 MHz | 5.52 | 6 | 6.48 [34, 35] | MHz | Trimmed for 2.7 V operation using factory trim values. See Figure 14 on page 20. SLIMO mode = 1 |
| $F_{CPU1}$ | CPU frequency (2.7 V nominal) | 0.093 | 3 | 3.15[34] | MHz | 12 MHz only for SLIMO mode = 0 |
| $F_{BLK27}$ | Digital PSoC block frequency (2.7 V nominal) | 0 | 12 | 12.5[34,35] | MHz | Refer to AC Digital Block Specifications on page 29 |
| $F_{32K1}$ | ILO frequency | 8 | 32 | 96 | kHz | |
| $F_{32K\_U}$ | ILO untrimmed frequency | 5 | – | 100 | kHz | After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the *PSoC Technical Reference Manual* for details on this timing |
| $t_{XRST}$ | External reset pulse width | 10 | – | – | µs | |
| $DC_{ILO}$ | IILO duty cycle | 20 | 50 | 80 | % | |
| $F_{MAX}$ | Maximum frequency of signal on row input or row output. | – | – | 12.3 | MHz | |
| $SR_{POWER\_UP}$ | Power supply slew rate | – | – | 250 | V/ms | $V_{DD}$ slew rate during power-up |
| $t_{POWERUP}$ | Time from end of POR to CPU executing code | – | 16 | 100 | ms | Power-up from 0 V. See the System Resets section of the *PSoC Technical Reference Manual*. |
| $t_{jit\_IMO}$ | 12 MHz IMO cycle-to-cycle jitter (RMS)[36] | – | 400 | 1000 | ps | |
| | 12 MHz IMO long term N cycle-to-cycle jitter (RMS)[36] | – | 600 | 1300 | ps | N = 32 |
| | 12 MHz IMO period jitter (RMS)[36] | – | 100 | 500 | ps | |

**Notes**
33. Errata: The worst case IMO frequency deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
34. 2.4 V < $V_{DD}$ < 3.0 V.
35. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” available at http://www.cypress.com for information on maximum frequency for user modules.
36. Refer to Cypress Jitter Specifications Application Note AN5054 “Understanding Datasheet Jitter Specifications for Cypress Timing Products” at www.cypress.com under Application Notes for more information.

*AC General Purpose I/O Specifications*

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

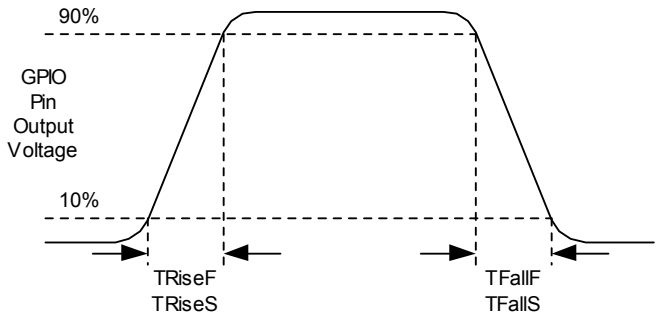
**Table 18. 5-V and 3.3-V AC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO operating frequency | 0 | – | 12 | MHz | Normal strong mode |
| TRiseF | Rise time, normal strong mode, Cload = 50 pF | 3 | – | 18 | ns | $V_{DD}$ = 4.5 to 5.25 V, 10% to 90% |
| TFallF | Fall time, normal strong mode, Cload = 50 pF | 2 | – | 18 | ns | $V_{DD}$ = 4.5 to 5.25 V, 10% to 90% |
| TRiseS | Rise time, slow strong mode, Cload = 50 pF | 7 | 27 | – | ns | $V_{DD}$ = 3 to 5.25 V, 10% to 90% |
| TFallS | Fall time, slow strong mode, Cload = 50 pF | 7 | 22 | – | ns | $V_{DD}$ = 3 to 5.25 V, 10% to 90% |

**Table 19. 2.7 V AC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO operating frequency | 0 | – | 3 | MHz | Normal strong mode |
| TRiseF | Rise time, normal strong mode, Cload = 50 pF | 6 | – | 50 | ns | $V_{DD}$ = 2.4 to 3.0 V, 10% to 90% |
| TFallF | Fall time, normal strong mode, Cload = 50 pF | 6 | – | 50 | ns | $V_{DD}$ = 2.4 to 3.0 V, 10% to 90% |
| TRiseS | Rise time, slow strong mode, Cload = 50 pF | 18 | 40 | 120 | ns | $V_{DD}$ = 2.4 to 3.0 V, 10% to 90% |
| TFallS | Fall time, slow strong mode, Cload = 50 pF | 18 | 40 | 120 | ns | $V_{DD}$ = 2.4 to 3.0 V, 10% to 90% |

**Figure 13. GPIO Timing Diagram**




*AC Operational Amplifier Specifications*

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ $T_A$ ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ $T_A$ ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

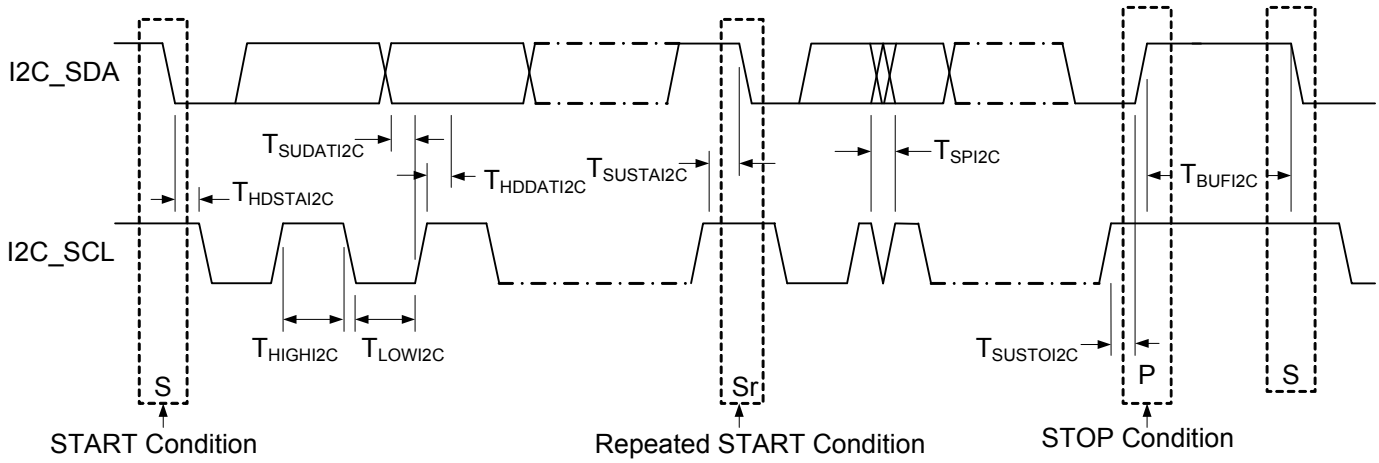
**Table 20. AC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{COMP}$ | Comparator mode response time, 50 mV overdrive | – | – | 100<br>200 | ns<br>ns | $V_{DD}$ ≥ 3.0 V<br>2.4 V < $V_{DD}$ < 3.0 V |

**Table 28. 2.7-V AC Characteristics of the I²C SDA and SCL Pins (Fast Mode not Supported)**

| Symbol | Description | Standard Mode | | Fast Mode | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $F_{SCLI2C}$ | SCL clock frequency | 0 | 100 | – | – | kHz |
| $T_{HDSTAI2C}$ | Hold time (repeated) start condition. After this period, the first clock pulse is generated. | 4.0 | – | – | – | µs |
| $T_{LOWI2C}$ | Low period of the SCL clock | 4.7 | – | – | – | µs |
| $T_{HIGHI2C}$ | High period of the SCL clock | 4.0 | – | – | – | µs |
| $T_{SUSTAI2C}$ | Setup time for a repeated start condition | 4.7 | – | – | – | µs |
| $T_{HDDATI2C}$ | Data hold time | 0 | – | – | – | µs |
| $T_{SUDATI2C}$ | Data setup time | 250 | – | – | – | ns |
| $T_{SUSTOI2C}$ | Setup time for stop condition | 4.0 | – | – | – | µs |
| $T_{BUFI2C}$ | Bus free time between a stop and start condition | 4.7 | – | – | – | µs |
| $T_{SPI2C}$ | Pulse width of spikes are suppressed by the input filter. | – | – | – | – | ns |

**Figure 14. Definition for Timing for Fast/Standard Mode on the I²C Bus**

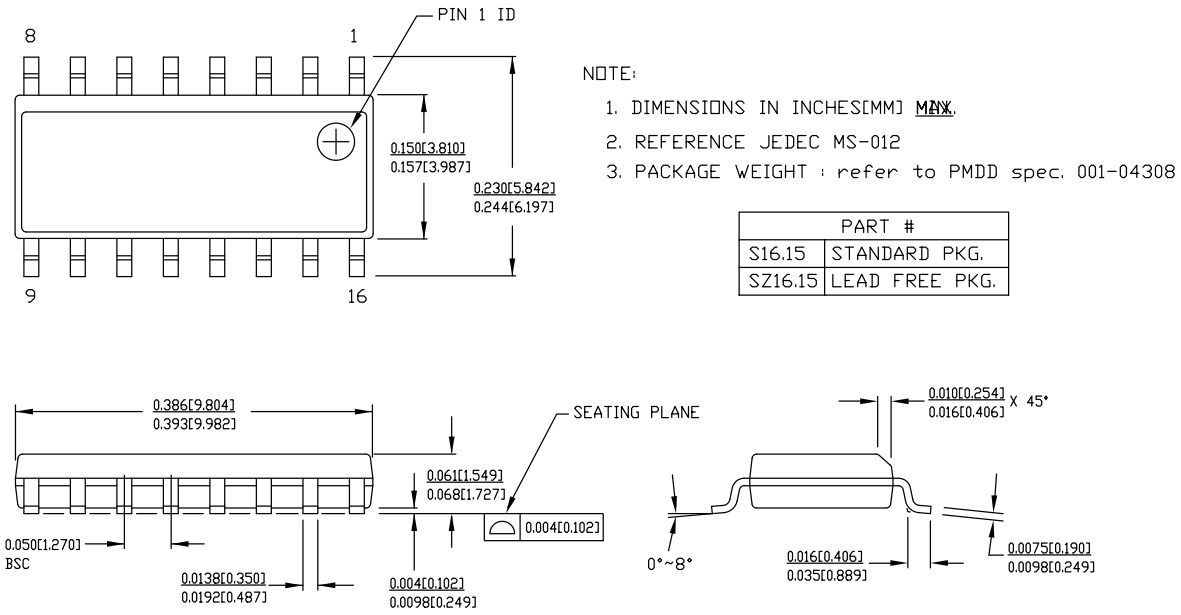


## Packaging Information

This section shows the packaging specifications for the CY8C21x34 PSoC device with the thermal impedances for each package.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

**Figure 15. 16-pin SOIC (150 Mils) Package Outline, 51-85068**




51-85068 *E

## Device Programmers

All device programmers can be purchased from the Cypress Online Store.

*CY3216 Modular Programmer*

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular programmer base
- Three programming module cards
- MiniProg programming unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

*CY3207ISSP In-System Serial Programmer (ISSP)*

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

**Note** CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240 V power supply, Euro-Plug adapter
- USB 2.0 cable

## Accessories (Emulation and Programming)

**Table 31. Emulation and Programming Accessories**

| Part Number | Pin Package | Flex-Pod Kit[45] | Foot Kit[46] | Adapter |
|---|---|---|---|---|
| CY8C21234-24SXI | 16-pin SOIC | CY3250-21X34 | CY3250-16SOIC-FK | Adapters can be found at http://www.emulation.com. |
| CY8C21334-24PVXI | 20-pin SSOP | CY3250-21X34 | CY3250-20SSOP-FK | |
| CY8C21534-24PVXI | 28-pin SSOP | CY3250-21X34 | CY3250-28SSOP-FK | |

**Notes**
45. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
46. Foot kit includes surface mount feet that can be soldered to the target PCB.

## Ordering Information

| Package | Ordering Code | Flash (Bytes) | SRAM (Bytes) | Switch Mode Pump | Temperature Range | Digital Blocks | Analog Blocks | Digital I/O Pins | Analog Inputs | Analog Outputs | XRES Pin |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 16-Pin (150-Mil) SOIC | CY8C21234-24SXI | 8 K | 512 | Yes | –40 °C to +85 °C | 4 | 4 | 12 | 12[47] | 0 | No |
| 16-Pin (150-Mil) SOIC (Tape and Reel) | CY8C21234-24SXIT | 8 K | 512 | Yes | –40 °C to +85 °C | 4 | 4 | 12 | 12[47] | 0 | No |
| 20-Pin (210-Mil) SSOP | CY8C21334-24PVXI | 8 K | 512 | No | –40 °C to +85 °C | 4 | 4 | 16 | 16[47] | 0 | Yes |
| 20-Pin (210-Mil) SSOP (Tape and Reel) | CY8C21334-24PVXIT | 8 K | 512 | No | –40 °C to +85 °C | 4 | 4 | 16 | 16[47] | 0 | Yes |
| 28-Pin (210-Mil) SSOP | CY8C21534-24PVXI | 8 K | 512 | No | –40 °C to +85 °C | 4 | 4 | 24 | 24[47] | 0 | Yes |
| 28-Pin (210-Mil) SSOP (Tape and Reel) | CY8C21534-24PVXIT | 8 K | 512 | No | –40 °C to +85 °C | 4 | 4 | 24 | 24[47] | 0 | Yes |
| 32-Pin (5 × 5 mm 1.00 max) Sawn QFN | CY8C21434-24LTXI | 8 K | 512 | No | –40 °C to +85 °C | 4 | 4 | 28 | 28[47] | 0 | Yes |
| 32-Pin (5 × 5 mm 1.00 max) Sawn QFN [48] (Tape and Reel) | CY8C21434-24LTXIT | 8 K | 512 | No | –40 °C to +85 °C | 4 | 4 | 28 | 28[47] | 0 | Yes |
| 32-Pin (5 × 5 mm 0.60 max) Thin Sawn QFN | CY8C21434-24LQXI | 8 K | 512 | No | –40 °C to +85 °C | 4 | 4 | 28 | 28[47] | 0 | Yes |
| 32-Pin (5 × 5 mm 0.60 max) Thin Sawn QFN (Tape and Reel) | CY8C21434-24LQXIT | 8 K | 512 | No | –40 °C to +85 °C | 4 | 4 | 28 | 28[47] | 0 | Yes |
| 32-Pin (5 × 5 mm 1.00 max) Sawn QFN [48] | CY8C21634-24LTXI | 8 K | 512 | Yes | –40 °C to +85 °C | 4 | 4 | 26 | 26[47] | 0 | Yes |
| 32-Pin (5 × 5 mm 1.00 max) Sawn QFN [48] (Tape and Reel) | CY8C21634-24LTXIT | 8 K | 512 | Yes | –40 °C to +85 °C | 4 | 4 | 26 | 26[47] | 0 | Yes |
| 56-Pin OCD SSOP | CY8C21001-24PVXI | 8 K | 512 | Yes | –40 °C to +85 °C | 4 | 4 | 26 | 26[47] | 0 | Yes |
| | CY8C21434-12X14I | Please contact sales office or Field Applications Engineer (FAE) for more information. | | | | | | | | | |

**Note** For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

**Notes**
47. All Digital I/O Pins also connect to the common analog mux.
48. Refer to the section 32-pin Part Pinout on page 12 for pin differences.

## Acronyms

Table 32 lists the acronyms that are used in this document.

**Table 32. Acronyms Used in this Datasheet**

| Acronym | Description | Acronym | Description |
|---|---|---|---|
| AC | alternating current | MIPS | million instructions per second |
| ADC | analog-to-digital converter | OCD | on-chip debug |
| API | application programming interface | PCB | printed circuit board |
| CMOS | complementary metal oxide semiconductor | PDIP | plastic dual-in-line package |
| CPU | central processing unit | PGA | programmable gain amplifier |
| CRC | cyclic redundancy check | PLL | phase-locked loop |
| CT | continuous time | POR | power on reset |
| DAC | digital-to-analog converter | PPOR | precision power on reset |
| DC | direct current | PRS | pseudo-random sequence |
| DTMF | dual-tone multi-frequency | PSoC® | Programmable System-on-Chip |
| ECO | external crystal oscillator | PWM | pulse width modulator |
| EEPROM | electrically erasable programmable read-only memory | QFN | quad flat no leads |
| GPIO | general purpose I/O | RTC | real time clock |
| ICE | in-circuit emulator | SAR | successive approximation |
| IDE | integrated development environment | SC | switched capacitor |
| ILO | internal low speed oscillator | SLIMO | slow IMO |
| IMO | internal main oscillator | SMP | switch-mode pump |
| I/O | input/output | SOIC | small-outline integrated circuit |
| IrDA | infrared data association | SPI™ | serial peripheral interface |
| ISSP | in-system serial programming | SRAM | static random access memory |
| LCD | liquid crystal display | SROM | supervisory read only memory |
| LED | light-emitting diode | SSOP | shrink small-outline package |
| LPC | low power comparator | UART | universal asynchronous receiver / transmitter |
| LVD | low voltage detect | USB | universal serial bus |
| MAC | multiply-accumulate | WDT | watchdog timer |
| MCU | microcontroller unit | XRES | external reset |

## Reference Documents

*CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM)* (001-14463)

*Design Aids – Reading and Writing PSoC® Flash - AN2015* (001-40459)

*Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages* – available at http://www.amkor.com.

# Document Conventions

## Units of Measure

Table 33 lists the units of measures.

**Table 33. Units of Measure**

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|---|---|---|---|
| kB | 1024 bytes | µH | micro henry |
| dB | decibels | µs | microsecond |
| °C | degree Celsius | ms | millisecond |
| µF | microfarad | ns | nanosecond |
| fF | femto farad | ps | picosecond |
| pF | picofarad | µV | microvolt |
| kHz | kilohertz | mV | millivolts |
| MHz | megahertz | mVpp | millivolts peak-to-peak |
| rt-Hz | root hertz | nV | nano volt |
| kΩ | kilo ohm | V | volt |
| Ω | ohm | µW | microwatt |
| µA | microampere | W | watt |
| mA | milliampere | mm | millimeter |
| nA | nano ampere | ppm | parts per million |
| pA | pico ampere | % | percent |
| mH | millihenry | | |

## Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

# Glossary

| | |
|---|---|
| active high | 1. A logic signal having its asserted state as the logic 1 state.<br>2. A logic signal having the logic 1 state as the higher voltage of the two states. |
| analog blocks | The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more. |
| analog-to-digital (ADC) | A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation. |
| Application programming interface (API) | A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications. |
| asynchronous | A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal. |
| bandgap reference | A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference. |
| bandwidth | 1. The frequency range of a message or information processing system measured in hertz.<br>2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum. |

## Glossary (continued)

| | |
|---|---|
| bias | 1. A systematic deviation of a value from a reference value.<br>2. The amount by which the average of a set of values departs from a reference value.<br>3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device. |
| block | 1. A functional unit that performs a single function, such as an oscillator.<br>2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block. |
| buffer | 1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written.<br>2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device.<br>3. An amplifier used to lower the output impedance of a system. |
| bus | 1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns.<br>2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0].<br>3. One or more conductors that serve as a common connection for a group of related devices. |
| clock | The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks. |
| comparator | An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements. |
| compiler | A program that translates a high level language, such as C, into machine language. |
| configuration space | In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’. |
| crystal oscillator | An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components. |
| cyclic redundancy check (CRC) | A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression. |
| data bus | A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions. |
| debugger | A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory. |
| dead band | A period of time when neither of two or more signals are in their active state or in transition. |
| digital blocks | The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI. |
| digital-to-analog (DAC) | A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation. |

## CY8C21X34 Errata Summary

The following table defines the errata applicability to available CY8C21X34 family devices. An "X" indicates that the errata pertains to the selected device.

**Note** Errata items, in the table below, are hyperlinked. Click on any item entry to jump to its description.

| Items | Part Number | Silicon Revision | Fix Status |
|---|---|---|---|
| [1.]. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes | CY8C21X34 | A | No fix is currently planned. |
| [2]. I2C Errors | CY8C21X34 | A | No fix is currently planned. |

### 1. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

- **Problem Definition**
  Asynchronous Digital Communications Interfaces may fail framing beyond 0 °C to 70 °C. This problem does not affect end-product usage between 0 °C and 70 °C.
- **Parameters Affected**
  The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
- **Trigger Condition(S)**
  The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the datasheet limit of ±2.5% when operated beyond the temperature range of 0 °C to +70 °C.
- **Scope of Impact**
  This problem may affect UART, IrDA, and FSK implementations.
- **Workaround**
  Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.
- **Fix Status**
  No fix is currently planned.

### 2. $I^2C$ Errors

- **Problem Definition**
  The $I^2C$ block exhibits occasional data and bus corruption errors when the $I^2C$ master initiates transactions while the device is transitioning in to or out of sleep mode.
- **Parameters Affected**
  Affects reliability of $I^2C$ communication to device, between $I^2C$ master, and third party $I^2C$ slaves.
- **Trigger Condition(S)**
  Triggered by transitions into and out of the device's sleep mode.
- **Scope of Impact**
  This problem may affect UART, IrDA, and FSK implementations.
- **Workaround**
  Firmware workarounds are available in firmware. Generally the workaround consists of disconnecting the $I^2C$ block from the bus prior to going to sleep modes. $I^2C$ transactions during sleep are supported by a protocol in which the master wakes the device prior to the $I^2C$ transaction
- **Fix Status**
  Will not be fixed.

## Document History Page (continued)

| Document Title: CY8C21634/CY8C21534/CY8C21434/CY8C21334/CY8C21234, PSoC® Programmable System-on-Chip™<br>Document Number: 38-12025 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *R | 2762499 | JVY | 09/11/2009 | Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows:<br>Modified $F_{IMO6}$ and $T_{WRITE}$ specifications.<br>Replaced $T_{RAMP}$ (time) specification with $SR_{POWER\_UP}$ (slew rate) specification.<br>Added note [11] to Flash Endurance specification.<br>Added $I_{OH}$, $I_{OL}$, $DC_{ILO}$, $F_{32K\_U}$, $T_{POWERUP}$, $T_{ERASEALL}$, $T_{PROGRAM\_HOT}$, and $T_{PROGRAM\_COLD}$ specifications. |
| *S | 2900687 | MAXK / NJF | 03/30/2010 | Updated The Analog Multiplexer System.<br>Updated Cypress website links.<br>Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings.<br>Removed DC Low Power Comparator section.<br>Updated 5-V and 3.3-V AC Chip-Level Specifications.<br>Removed AC Low Power Comparator and AC Analog Mux Bus sections.<br>Updated note in Packaging Information and package diagrams.<br>Added 56 SSOP values for Thermal Impedances, Solder Reflow Specifications.<br>Removed Third Party Tools and Build a PSoC Emulator into your Board.<br>Updated Ordering Code Definitions.<br>Removed inactive parts from Ordering Information<br>Removed obsolete package spec 001-06392.<br>Updated links in Sales, Solutions, and Legal Information. |
| *T | 2937578 | VMAD | 05/26/2010 | Updated content to match current style guide and data sheet template.<br>No technical updates. |
| *U | 3005573 | NJF | 09/02/10 | Added PSoC Device Characteristics table.<br>Added DC $I^2C$ Specifications table.<br>Added $F_{32K\_U}$ max limit.<br>Added Tjit_IMO specification, removed existing jitter specifications.<br>Updated Units of Measure, Acronyms, Glossary, and References sections.<br>Updated solder reflow specifications.<br>No specific changes were made to AC Digital Block Specifications table and $I^2C$ Timing Diagram. They were updated for clearer understanding.<br>Template and styles update. |
| *V | 3068269 | ARVM | 10/21/2010 | Removed pruned parts CY8C21434-24LKXI and CY8C21434-24LKXIT from Ordering Information. |
| *W | 3281271 | VMAD | 08/23/2011 | Under Table 20 on page 28 “Notes” section, the text “2.4 V < $V_{CC}$ < 3.0 V” is changed to “2.4 V < $V_{DD}$ < 3.0 V”.<br>Updated Solder Reflow Specifications.<br>Changed package diagram from 51-85188 *D to 001-30999 *C for QFN32 package. |
| *X | 3383568 | GIR | 10/05/2011 | The text “Pin must be left floating” is included under Description of NC pin in CY8C21001 56-pin SSOP Pin Definitions on page 14.<br>Changed spec 001-30999 from 32-Pin (5 × 5 mm 0.93 Max) Sawn QFN to 32-Pin (5 × 5 mm 1.0 Max) Sawn QFN<br>Removed pruned parts CY8C21434-24LCXI and CY8C21434-24LCXIT from the Ordering Information table. |
| *Y | 3659297 | YLIU | 07/26/2012 | Updated Packaging Information (Removed spec 001-44368). |

## Document History Page (continued)

| Document Title: CY8C21634/CY8C21534/CY8C21434/CY8C21334/CY8C21234, PSoC® Programmable System-on-Chip™<br>Document Number: 38-12025 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| AD | 4338103 | PRKU | 04/15/2014 | Updated Pin Information:<br>Updated CY8C21234 16-pin SOIC Pin Definitions (corresponding to CY8C21234):<br>Added Note 9 and referred the same note in the description of pin 6 and pin 8.<br>Updated CY8C21334 20-pin SSOP Pin Definitions (corresponding to CY8C21334):<br>Added Note 11 and referred the same note in the description of pin 5 and pin 10.<br>Updated CY8C21534 28-pin SSOP Pin Definitions (corresponding to CY8C21534):<br>Added Note 13 and referred the same note in the description of pin 9 and pin 14.<br>Updated CY8C21434/CY8C21634 32-pin QFN Pin Definitions (corresponding to CY8C21434/CY8C21634):<br>Added Note 16 and referred the same note in the description of pin 7, pin 12 and pin 32.<br>Updated CY8C21001 56-pin SSOP Pin Definitions (corresponding to CY8C21001):<br>Added Note 18 and referred the same note in the description of pin 17, pin 18 and pin 28.<br>Updated Packaging Information:<br>Updated “Important Note” below Figure 18.<br>Updated Thermal Impedances:<br>Updated Note 43 referred in Table 29. |
| AE | 4531967 | DCHE | 10/10/2014 | Added More Information.<br>Added PSoC Designer. |
| AF | 4593771 | DIMA | 12/11/2014 | Updated Pin Information:<br>Updated CY8C21001 56-pin SSOP Pin Definitions:<br>Referred Note 18 in description of pin 1.<br>Updated Packaging Information:<br>spec 51-85077 – Changed revision from *E to *F.<br>spec 51-85079 – Changed revision from *E to *F. |
| AG | 4670626 | DCHE | 02/25/2015 | Updated Errata:<br>Replaced CY8C21234 with CY8C21X34 in all instances. |
| AH | 5394304 | DCHE | 08/08/2016 | Updated to new template.<br>Completing Sunset Review. |

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