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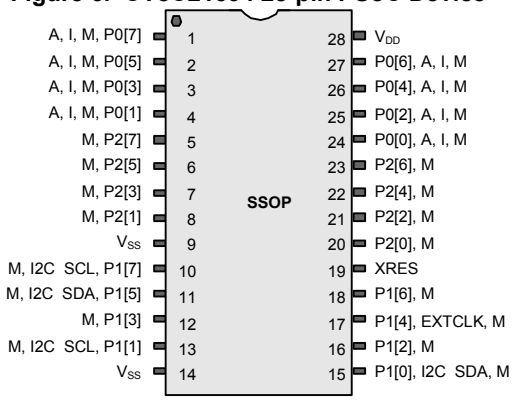
Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 28x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21434-24ltxi

28-pin Part Pinout

Figure 6. CY8C21534 28-pin PSoC Device



CY8C21534 28-pin SSOP Pin Definitions

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input and column output
3	I/O	I, M	P0[3]	Analog column mux input and column output, integrating input
4	I/O	I, M	P0[1]	Analog column mux input, integrating input
5	I/O	M	P2[7]	
6	I/O	M	P2[5]	
7	I/O	I, M	P2[3]	Direct switched capacitor block input
8	I/O	I, M	P2[1]	Direct switched capacitor block input
9	Power		V_{SS}	Ground connection [13]
10	I/O	M	P1[7]	I^2C SCL
11	I/O	M	P1[5]	I^2C SDA
12	I/O	M	P1[3]	
13	I/O	M	P1[1]	I^2C SCL, ISSP-SCLK[14]
14	Power		V_{SS}	Ground connection [13]
15	I/O	M	P1[0]	I^2C SDA, ISSP-SDATA[14]
16	I/O	M	P1[2]	
17	I/O	M	P1[4]	Optional external clock input (EXTCLK)
18	I/O	M	P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	I, M	P2[0]	Direct switched capacitor block input
21	I/O	I, M	P2[2]	Direct switched capacitor block input
22	I/O	M	P2[4]	
23	I/O	M	P2[6]	
24	I/O	I, M	P0[0]	Analog column mux input
25	I/O	I, M	P0[2]	Analog column mux input
26	I/O	I, M	P0[4]	Analog column mux input
27	I/O	I, M	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage

LEGEND A: Analog, I: Input, O = Output, and M = Analog Mux Input.

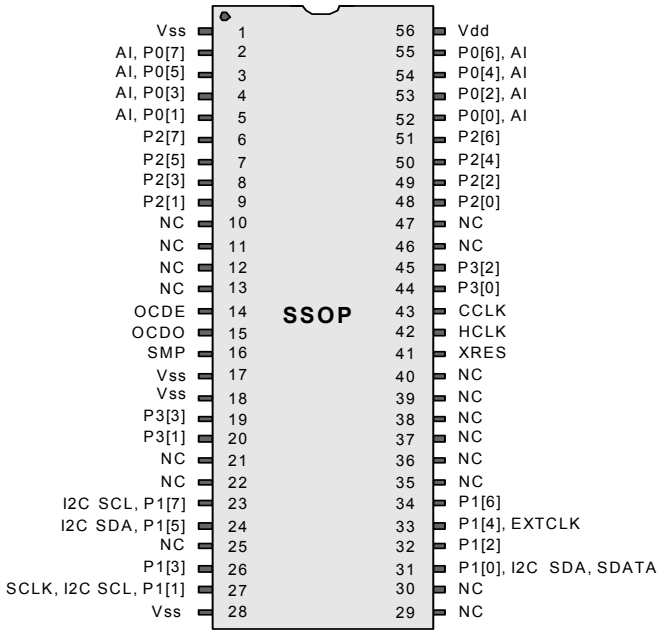
Notes
13. All V_{SS} pins should be brought out to one common GND plane.
14. These are the ISSP pins, which are not high Z at POR. See the *PSoC Technical Reference Manual* for details.

56-pin Part Pinout

The 56-pin SSOP part is for the CY8C21001 on-chip debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Figure 10. CY8C21001 56-pin PSoC Device



CY8C21001 56-pin SSOP Pin Definitions

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	Power		V_{SS}	Ground connection [18]
2	I/O	I	P0[7]	Analog column mux input
3	I/O	I	P0[5]	Analog column mux input and column output
4	I/O	I	P0[3]	Analog column mux input and column output
5	I/O	I	P0[1]	Analog column mux input
6	I/O		P2[7]	
7	I/O		P2[5]	
8	I/O	I	P2[3]	Direct switched capacitor block input
9	I/O	I	P2[1]	Direct switched capacitor block input
10			NC	No connection. Pin must be left floating
11			NC	No connection. Pin must be left floating
12			NC	No connection. Pin must be left floating
13			NC	No connection. Pin must be left floating
14	OCD		OCDE	OCD even data I/O
15	OCD		OCDO	OCD odd data output
16	Power		SMP	SMP connection to required external components
17	Power		V_{SS}	Ground connection [18]
18	Power		V_{SS}	Ground connection [18]
19	I/O		P3[3]	

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C21x34 PSoC device. For up-to-date electrical specifications, visit the Cypress web site at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C as specified, except where noted.

Refer to Table 16 on page 26 for the electrical specifications for the IMO using SLIMO mode.

Figure 11. Voltage versus CPU Frequency

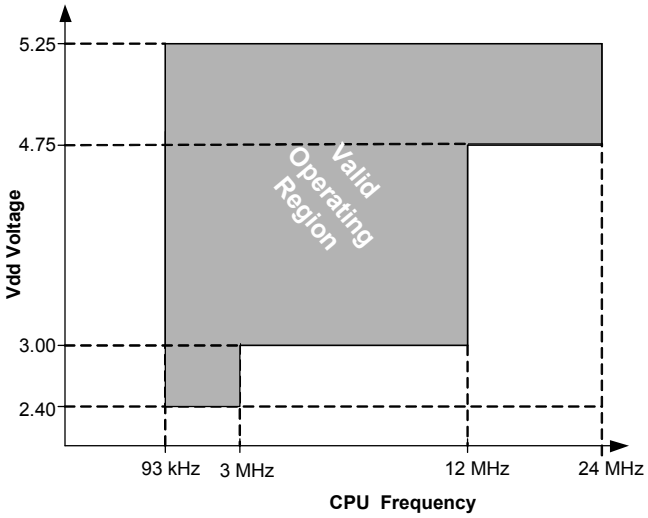
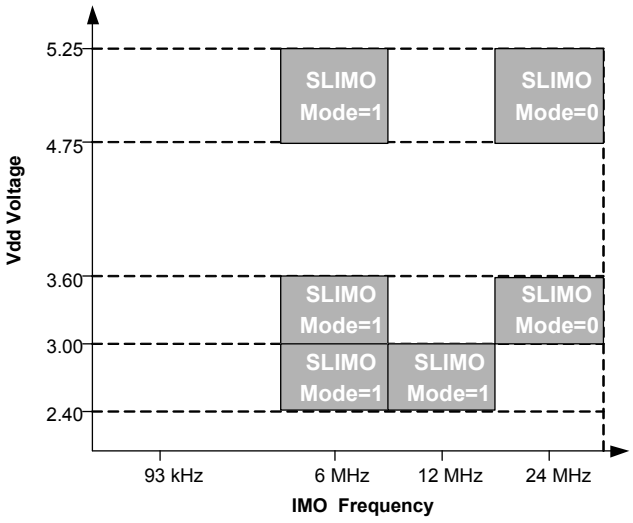


Figure 14. IMO Frequency Trim Options



DC Electrical Characteristics

DC Chip-Level Specifications

Table 5 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 5. DC Chip-level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	See Table 13 on page 24
I_{DD}	Supply current, IMO = 24 MHz	–	3	4	mA	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz
I_{DD3}	Supply current, IMO = 6 MHz using SLIMO mode.	–	1.2	2	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz
I_{DD27}	Supply current, IMO = 6 MHz using SLIMO mode.	–	1.1	1.5	mA	Conditions are V_{DD} = 2.55 V, T_A = 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz
I_{SB27}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	□µA	V_{DD} = 2.55 V, 0 °C ≤ T_A ≤ 40 °C
I_{SB}	Sleep (mode) current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C
V_{REF}	Reference voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate V_{DD} V_{DD} = 3.0 V to 5.25 V
V_{REF27}	Reference voltage (Bandgap)	1.16	1.30	1.33	V	Trimmed for appropriate V_{DD} V_{DD} = 2.4 V to 3.0 V
AGND	Analog ground	V_{REF} – 0.003	V_{REF}	V_{REF} + 0.003	V	

DC General-Purpose I/O Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

Table 6. 5-V and 3.3-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]))
I_{OH}	High level source current	10	–	–	mA	V_{OH} = V_{DD} – 1.0 V, see the limitations of the total current in the note for V_{OH}
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.0 to 5.25
V_{IH}	Input high level	2.1	–		V	V_{DD} = 3.0 to 5.25
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent Temp = 25 °C
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent Temp = 25 °C

Table 7. 2.7-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 0.4	–	–	V	I_{OH} = 2.5 mA (6.25 Typ), V_{DD} = 2.4 to 3.0 V (16 mA maximum, 50 mA Typ combined I_{OH} budget)
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 10 mA, V_{DD} = 2.4 to 3.0 V (90 mA maximum combined I_{OL} budget)
I_{OH}	High level source current	2.5	–	–	mA	V_{OH} = V_{DD} – 0.4 V, see the limitations of the total current in the note for V_{OH}
I_{OL}	Low level sink current	10	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input low level	–	–	0.75	V	V_{DD} = 2.4 to 3.0
V_{IH}	Input high level	2.0	–	–	V	V_{DD} = 2.4 to 3.0
V_H	Input hysteresis	–	90	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent Temp = 25 °C
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent Temp = 25 °C

DC Operational Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 8. 5-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins 7-to-1)	–	200	–	pA	Gross tested to 1 µA
I_{EBOA00}	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 µA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0.0	–	V_{DD} – 1.0	V	
G_{OLOA}	Open loop gain	–	80	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	µA	

Table 9. 3.3-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA
I_{EBOA00}	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 µA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0	–	V_{DD} – 1.0	V	
G_{OLOA}	Open loop gain	–	80	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	µA	

Table 10. 2.7-V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA
I_{EBOA00}	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 µA
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0	–	V_{DD} – 1.0	V	
G_{OLOA}	Open loop gain	–	80	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	µA	

DC Switch Mode Pump Specifications

Table 11 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Figure 12. Basic Switch Mode Pump Circuit

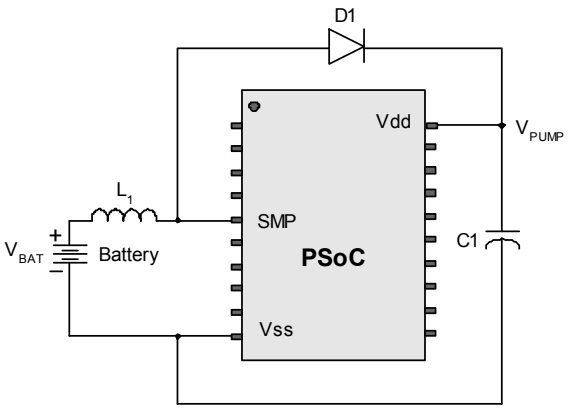


Table 11. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP5V}	5 V output voltage from pump	4.75	5.0	5.25	V	Configured as in Note 20 Average, neglecting ripple SMP trip voltage is set to 5.0 V
V_{PUMP3V}	3.3 V output voltage from pump	3.00	3.25	3.60	V	Configured as in Note 20 Average, neglecting ripple. SMP trip voltage is set to 3.25 V
V_{PUMP2V}	2.6 V output voltage from pump	2.45	2.55	2.80	V	Configured as in Note 20 Average, neglecting ripple. SMP trip voltage is set to 2.55 V
I_{PUMP}	Available output current V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.3 V, V_{PUMP} = 2.55 V	 5 8 8	 – – –	 – – –	 mA mA mA	Configured as in Note 20 SMP trip voltage is set to 5.0 V SMP trip voltage is set to 3.25 V SMP trip voltage is set to 2.55 V
V_{BAT5V}	Input voltage range from battery	1.8	–	5.0	V	Configured as in Note 20 SMP trip voltage is set to 5.0 V
V_{BAT3V}	Input voltage range from battery	1.0	–	3.3	V	Configured as in Note 20 SMP trip voltage is set to 3.25 V
V_{BAT2V}	Input voltage range from battery	1.0	–	2.8	V	Configured as in Note 20 SMP trip voltage is set to 2.55 V
$V_{BATSTART}$	Minimum input voltage from battery to start pump	1.2	–	–	V	Configured as in Note 20 0 °C ≤ T_A ≤ 100. 1.25 V at T_A = –40 °C
ΔV_{PUMP_Line}	Line regulation (over Vi range)	–	5	–	$\%V_O$	Configured as in Note 20 V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 13 on page 24
ΔV_{PUMP_Load}	Load regulation	–	5	–	$\%V_O$	Configured as in Note 20 V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 13 on page 24
ΔV_{PUMP_Ripple}	Output voltage ripple (depends on cap/load)	–	100	–	mVpp	Configured as in Note 20 Load is 5 mA
E_3	Efficiency	35	50	–	%	Configured as in Note 20 Load is 5 mA. SMP trip voltage is set to 3.25 V

Note
20. L_1 = 2 mH inductor, C_1 = 10 mF capacitor, D_1 = Schottky diode. See Figure 12 on page 23.

Table 17. 2.7-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12} [33]	IMO frequency for 12 MHz	11.04	12	12.96 [34, 35]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 14 on page 20. SLIMO mode = 1
F_{IMO6} [33]	IMO frequency for 6 MHz	5.52	6	6.48 [34, 35]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 14 on page 20. SLIMO mode = 1
F_{CPU1}	CPU frequency (2.7 V nominal)	0.093	3	3.15[34]	MHz	12 MHz only for SLIMO mode = 0
F_{BLK27}	Digital PSoC block frequency (2.7 V nominal)	0	12	12.5[34,35]	MHz	Refer to AC Digital Block Specifications on page 29
F_{32K1}	ILO frequency	8	32	96	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the *PSoC Technical Reference Manual* for details on this timing
t_{XRST}	External reset pulse width	10	–	–	µs	
DC_{ILO}	IILO duty cycle	20	50	80	%	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the *PSoC Technical Reference Manual*.
t_{jit_IMO}	12 MHz IMO cycle-to-cycle jitter (RMS)[36]	–	400	1000	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)[36]	–	600	1300	ps	N = 32
	12 MHz IMO period jitter (RMS)[36]	–	100	500	ps	

Notes
33. Errata: The worst case IMO frequency deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
34. 2.4 V < V_{DD} < 3.0 V.
35. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” available at http://www.cypress.com for information on maximum frequency for user modules.
36. Refer to Cypress Jitter Specifications Application Note AN5054 “Understanding Datasheet Jitter Specifications for Cypress Timing Products” at www.cypress.com under Application Notes for more information.

AC General Purpose I/O Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

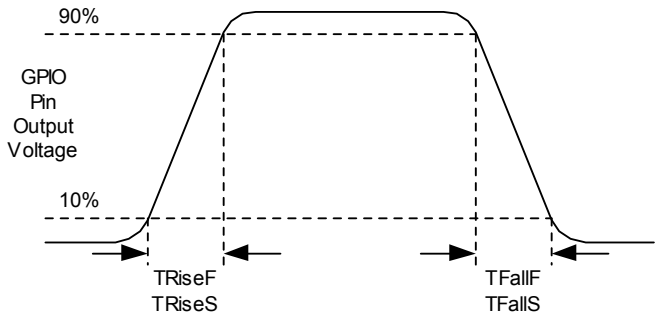
Table 18. 5-V and 3.3-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal strong mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% to 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% to 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	7	27	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	7	22	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%

Table 19. 2.7 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	3	MHz	Normal strong mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%

Figure 13. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 20. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP}	Comparator mode response time, 50 mV overdrive	–	–	100 200	ns ns	V_{DD} ≥ 3.0 V 2.4 V < V_{DD} < 3.0 V

Table 22. 2.7-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block input clock frequency	–	–	12.7	MHz	2.4 V < V_{DD} < 3.0 V
Timer	Capture pulse width	100[38]	–	–	ns	
	Input clock frequency, with or without capture	–	–	12.7	MHz	
Counter	Enable input pulse width	100	–	–	ns	
	Input clock frequency, no enable input	–	–	12.7	MHz	
	Input clock frequency, enable input	–	–	12.7	MHz	
Dead Band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	100	–	–	ns	
	Disable mode	100	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	
CRCPRS (PRS Mode)	Input clock frequency	–	–	12.7	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	12.7	MHz	
SPIM	Input clock frequency	–	–	6.35	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	
	Width of SS_ Negated between transmissions	100	–	–	ns	
Transmitter	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 23. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

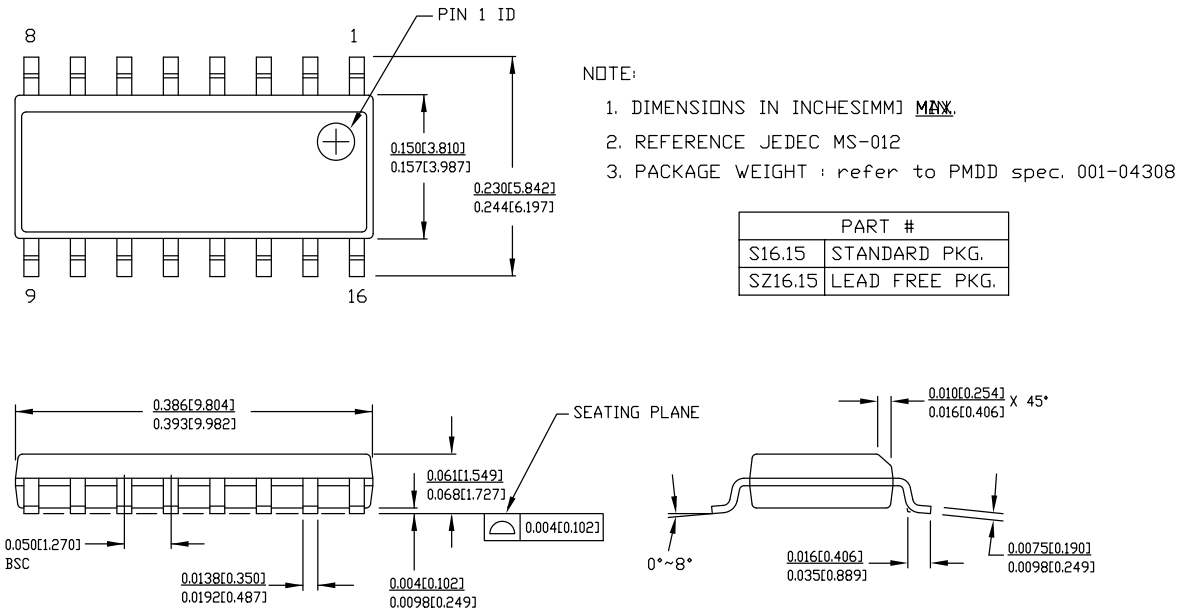
Note
38. 100 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

Packaging Information

This section shows the packaging specifications for the CY8C21x34 PSoC device with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Figure 15. 16-pin SOIC (150 Mils) Package Outline, 51-85068



51-85068 *E

Thermal Impedances

Table 29. Thermal Impedances per Package

Package	Typical θ_{JA} [42]	Typical θ_{JC}
16-pin SOIC	123 °C/W	55 °C/W
20-pin SSOP	117 °C/W	41 °C/W
28-pin SSOP	96 °C/W	39 °C/W
32-pin QFN[43] 5 × 5 mm 0.60 Max	27 °C/W	15 °C/W
32-pin QFN[43] 5 × 5 mm 1.00 Max	22 °C/W	12 °C/W
56-pin SSOP	48 °C/W	24 °C/W

Solder Reflow Specifications

Table 30 shows the solder reflow temperature limits that must not be exceeded.

Table 30. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
16-pin SOIC	260 °C	30 seconds
20-pin SSOP	260 °C	30 seconds
28-pin SSOP	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds
56-pin SSOP	260 °C	30 seconds

Notes
42. $T_J = T_A + \text{Power} \times \theta_{JA}$
43. To achieve the thermal impedance specified for the QFN package, refer to *Application Note EROS - Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices* available at http://www.cypress.com.
44. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

This section presents the development tools available for all current PSoC device families including the CY8C21x34 family.

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com and includes a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation, and the software interface allows you to run, halt, and single step the processor, and view the content of specific memory locations. Advance emulation features also supported through PSoC Designer. The kit includes:

- PSoC Designer software CD
- ICE-Cube in-circuit emulator
- ICE Flex-Pod for CY8C29x66 family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240 V power supply, Euro-Plug adapter
- iMAGEcraft C compiler
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466-24PXI 28-PDIP chip samples

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows you to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- 28-pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- Two 28-pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. The board includes both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB board
- LCD module
- MIniProg programming unit
- Mini USB cable
- PSoC Designer and example projects CD
- Getting Started guide
- Wire pack

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular programmer base
- Three programming module cards
- MiniProg programming unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 programmer unit
- PSoC ISSP software CD
- 110 ~ 240 V power supply, Euro-Plug adapter
- USB 2.0 cable

Accessories (Emulation and Programming)

Table 31. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit[45]	Foot Kit[46]	Adapter
CY8C21234-24SXI	16-pin SOIC	CY3250-21X34	CY3250-16SOIC-FK	Adapters can be found at http://www.emulation.com.
CY8C21334-24PVXI	20-pin SSOP	CY3250-21X34	CY3250-20SSOP-FK	
CY8C21534-24PVXI	28-pin SSOP	CY3250-21X34	CY3250-28SSOP-FK	

Notes
45. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
46. Foot kit includes surface mount feet that can be soldered to the target PCB.

Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
16-Pin (150-Mil) SOIC	CY8C21234-24SXI	8 K	512	Yes	–40 °C to +85 °C	4	4	12	12[47]	0	No
16-Pin (150-Mil) SOIC (Tape and Reel)	CY8C21234-24SXIT	8 K	512	Yes	–40 °C to +85 °C	4	4	12	12[47]	0	No
20-Pin (210-Mil) SSOP	CY8C21334-24PVXI	8 K	512	No	–40 °C to +85 °C	4	4	16	16[47]	0	Yes
20-Pin (210-Mil) SSOP (Tape and Reel)	CY8C21334-24PVXIT	8 K	512	No	–40 °C to +85 °C	4	4	16	16[47]	0	Yes
28-Pin (210-Mil) SSOP	CY8C21534-24PVXI	8 K	512	No	–40 °C to +85 °C	4	4	24	24[47]	0	Yes
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C21534-24PVXIT	8 K	512	No	–40 °C to +85 °C	4	4	24	24[47]	0	Yes
32-Pin (5 × 5 mm 1.00 max) Sawn QFN	CY8C21434-24LTXI	8 K	512	No	–40 °C to +85 °C	4	4	28	28[47]	0	Yes
32-Pin (5 × 5 mm 1.00 max) Sawn QFN [48] (Tape and Reel)	CY8C21434-24LTXIT	8 K	512	No	–40 °C to +85 °C	4	4	28	28[47]	0	Yes
32-Pin (5 × 5 mm 0.60 max) Thin Sawn QFN	CY8C21434-24LQXI	8 K	512	No	–40 °C to +85 °C	4	4	28	28[47]	0	Yes
32-Pin (5 × 5 mm 0.60 max) Thin Sawn QFN (Tape and Reel)	CY8C21434-24LQXIT	8 K	512	No	–40 °C to +85 °C	4	4	28	28[47]	0	Yes
32-Pin (5 × 5 mm 1.00 max) Sawn QFN [48]	CY8C21634-24LTXI	8 K	512	Yes	–40 °C to +85 °C	4	4	26	26[47]	0	Yes
32-Pin (5 × 5 mm 1.00 max) Sawn QFN [48] (Tape and Reel)	CY8C21634-24LTXIT	8 K	512	Yes	–40 °C to +85 °C	4	4	26	26[47]	0	Yes
56-Pin OCD SSOP	CY8C21001-24PVXI	8 K	512	Yes	–40 °C to +85 °C	4	4	26	26[47]	0	Yes
	CY8C21434-12X14I	Please contact sales office or Field Applications Engineer (FAE) for more information.									

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Notes
47. All Digital I/O Pins also connect to the common analog mux.
48. Refer to the section 32-pin Part Pinout on page 12 for pin differences.

Document Conventions

Units of Measure

Table 33 lists the units of measures.

Table 33. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	µH	micro henry
dB	decibels	µs	microsecond
°C	degree Celsius	ms	millisecond
µF	microfarad	ns	nanosecond
fF	femto farad	ps	picosecond
pF	picofarad	µV	microvolt
kHz	kilohertz	mV	millivolts
MHz	megahertz	mVpp	millivolts peak-to-peak
rt-Hz	root hertz	nV	nano volt
kΩ	kilo ohm	V	volt
Ω	ohm	µW	microwatt
µA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nano ampere	ppm	parts per million
pA	pico ampere	%	percent
mH	millihenry		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary (continued)

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Errata

This section describes the errata for the PSoC® Programmable System-on-Chip CY8C21X34. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8C21X34	CY8C21234-24SXI
	CY8C21234-24SXIT
	CY8C21334-24PVXI
	CY8C21334-24PVXIT
	CY8C21534-24PVXI
	CY8C21534-24PVXIT
	CY8C21434-24LFXI
	CY8C21434-24LFXIT
	CY8C21434-24LKXI
	CY8C21434-24LKXIT
	CY8C21634-24LFXI
	CY8C21634-24LFXIT
	CY8C21434-24LTXI
	CY8C21434-24LTXIT
	CY8C21434-24LQXI
	CY8C21434-24LQXIT
	CY8C21634-24LTXI
	CY8C21634-24LTXIT
	CY8C21001-24PVXI

CY8C21X34 Qualification Status

Product Status: Production

Document History Page

Document Title: CY8C21634/CY8C21534/CY8C21434/CY8C21334/CY8C21234, PSoC® Programmable System-on-Chip™ Document Number: 38-12025				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	227340	HMT	See ECN	New silicon and document (Revision **).
*A	235992	SFV	See ECN	Updated Overview and Electrical Spec. chapters, along with revisions to the 24-Pin pinout part. Revised the register mapping tables. Added a SSOP 28-Pin part.
*B	248572	SFV	See ECN	Changed title to include all part #s. Changed 28-Pin SSOP from CY8C21434 to CY8C21534. Changed pin 9 on the 28-Pin SSOP from SMP pin to Vss pin. Added SMP block to architecture diagram. Update Electrical Specifications. Added another 32-Pin MLF part: CY8C21634.
*C	277832	HMT	See ECN	Verify datasheet standards from SFV memo. Add Analog Input Mux to applicable pin outs. Update PSoC Characteristics table. Update diagrams and specs. Final.
*D	285293	HMT	See ECN	Update 2.7 V DC GPIO spec. Add Reflow Peak Temp. table.
*E	301739	HMT	See ECN	DC Chip-Level Specification changes. Update links to new CY.com Portal.
*F	329104	HMT	See ECN	Re-add pinout ISSP notation. Fix TMP register names. Clarify ADC feature. Update Electrical Specifications. Update Reflow Peak Temp. table. Add 32 MLF E-PAD dimensions. Add ThetaJC to Thermal Impedance table. Fix 20-Pin package order number. Add CY logo. Update CY copyright.
*G	352736	HMT	See ECN	Add new color and logo. Add URL to preferred dimensions for mounting MLF packages. Update Transmitter and Receiver AC Digital Block Electrical Specifications.
*H	390152	HMT	See ECN	Clarify MLF thermal pad connection info. Replace 16-Pin 300-MIL SOIC with correct 150-MIL.
*I	413404	HMT	See ECN	Update 32-Pin QFN E-Pad dimensions and rev. *A. Update CY branding and QFN convention.
*J	430185	HMT	See ECN	Add new 32-Pin 5x5 mm 0.60 thickness QFN package and diagram, CY8C21434-24LKXI. Update thermal resistance data. Add 56-Pin SSOP on-chip debug non-production part, CY8C21001-24PVXI. Update typical and recommended Storage Temperature per industrial specs. Update copyright and trademarks.
*K	677717	HMT	See ECN	Add CapSense SNR requirement reference. Add new Dev. Tool section. Add CY8C20x34 to PSoC Device Characteristics table. Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Update rev. of 32-Lead (5x5 mm 0.60 MAX) QFN package diagram.
*L	2147847	UVS / PYRS	02/27/08	Added 32-Pin QFN Sawn pin diagram, package diagram, and ordering information.
*M	2273246	UVS / AESA	04/01/08	Added 32 pin thin sawn package diagram.
*N	2618124	OGNE / PYRS	12/09/08	Added Note in Ordering Information section. Changed title from PSoC Mixed-Signal Array to PSoC Programmable System-on-Chip
*O	2684145	SNV / AESA	04/06/2009	Updated 32-Pin Sawn QFN package dimension for CY8C21434-24LTXIT Updated Getting Started, Development Tools, and Designing with PSoC Designer Sections
*P	2693024	DPT / PYRS	04/16/2009	Updated 32-Pin Sawn QFN package diagram
*Q	2720594	BRW	06/22/09	Corrected ohm symbol and parenthesis in figure caption (Fig.25) Removed references to mixed-sginal array from the text. Updated Development Tools Selection section.

Document History Page (continued)

Document Title: CY8C21634/CY8C21534/CY8C21434/CY8C21334/CY8C21234, PSoC® Programmable System-on-Chip™ Document Number: 38-12025				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*Z	3902039	VNJ	02/12/2013	Updated Electrical Specifications (Updated AC Electrical Characteristics (Updated AC Chip-Level Specifications (Updated Table 16 (Changed minimum value of F_{IMO6} parameter from 5.5 MHz to 5.52 MHz, changed maximum value of F_{IMO6} parameter from 6.5 MHz to 6.48 MHz), updated Table 17 (Changed minimum value of F_{IMO12} parameter from 11.5 MHz to 11.04 MHz, changed maximum value of F_{IMO12} parameter from 12.7 MHz to 12.96 MHz, changed minimum value of F_{IMO6} parameter from 5.5 MHz to 5.52 MHz, changed maximum value of F_{IMO6} parameter from 6.5 MHz to 6.48 MHz)))). Updated Packaging Information: spec 51-85068 – Changed revision from *D to *E. spec 001-30999 – Changed revision from *C to *D. spec 001-48913 – Changed revision from *B to *C. spec 51-85062 – Changed revision from *E to *F.
AA	3993249	SLAN	05/07/2013	Added Errata.
AB	4076892	SLAN	07/25/2013	Added Errata footnotes (Notes 1, 2, 3, 4, 5, 8, 28, 33, 40). Updated Features: Added Note 1 and referred in “Internal ±2.5% 24- / 48-MHz main oscillator”. Added Note 2 and referred in “I^2C” under “Additional system resources”. Updated PSoC Functional Overview: Updated The PSoC Core: Added Note 3 and referred in “24 MHz”. Added Note 4 and referred in “I^2C” under “System resources provide these additional capabilities”. Updated The Digital System: Added Note 4 and referred in “I^2C slave and multi-master”. Updated Additional System Resources: Added Note 5 and referred in “I^2C”. Updated Development Tools: Added Note 8 and referred in “I^2C” under “Built-in support for communication interfaces”. Updated Electrical Specifications: Updated AC Electrical Characteristics: Updated AC Chip-Level Specifications: Added Note 28 and referred in “F_{IMO24}” and “F_{IMO6}” parameters in Table 16. Added Note 33 and referred in “F_{IMO12}” and “F_{IMO6}” parameters in Table 17. Updated AC I2C [40] Specifications: Added Note 40 and referred in the heading. Updated to new template. Completing Sunset Review.
AC	4143112	DCHE	10/01/2013	Updated Packaging Information: spec 001-48913 – Changed revision from *C to *D. Updated Ordering Information (Updated part numbers). Updated Reference Documents: Removed references of spec 001-14503 and spec 001-17397 as these specs are obsolete.