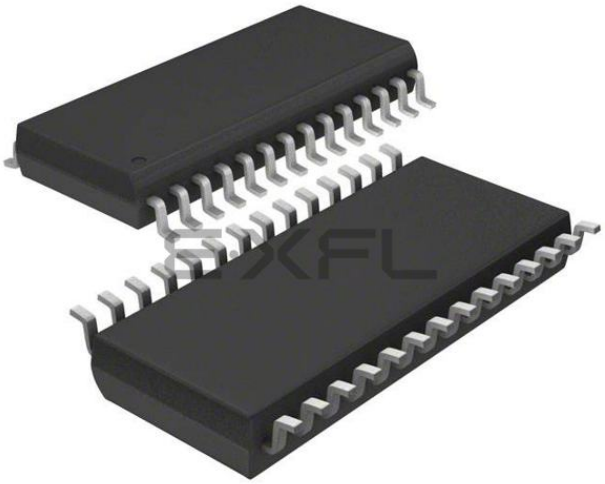

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 28x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21534-24pvxi

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C [8] slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

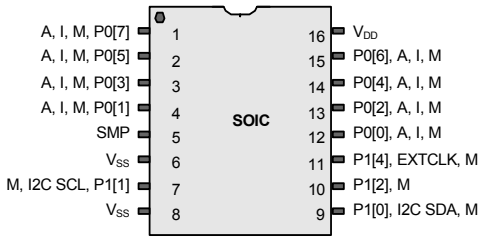
Note
8. Errata:The I^2C block exhibits occasional data and bus corruption errors when the I^2C master initiates transactions while the device is transitioning in to or out of sleep mode.

Pin Information

The CY8C21x34 PSoC device is available in a variety of packages which are listed in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of Digital I/O.

16-pin Part Pinout

Figure 4. CY8C21234 16-pin PSoC Device



CY8C21234 16-pin SOIC Pin Definitions

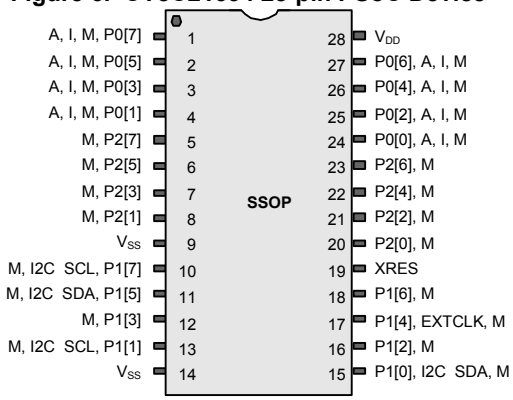
Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input
3	I/O	I, M	P0[3]	Analog column mux input, integrating input
4	I/O	I, M	P0[1]	Analog column mux input, integrating input
5	Power		SMP	Switch-mode pump (SMP) connection to required external components
6	Power		V_{SS}	Ground connection [9]
7	I/O	M	P1[1]	I^2C serial clock (SCL), ISSP-SCLK[10]
8	Power		V_{SS}	Ground connection [9]
9	I/O	M	P1[0]	I^2C serial data (SDA), ISSP-SDATA[10]
10	I/O	M	P1[2]	
11	I/O	M	P1[4]	Optional external clock input (EXTCLK)
12	I/O	I, M	P0[0]	Analog column mux input
13	I/O	I, M	P0[2]	Analog column mux input
14	I/O	I, M	P0[4]	Analog column mux input
15	I/O	I, M	P0[6]	Analog column mux input
16	Power		V_{DD}	Supply voltage

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Notes
9. All V_{SS} pins should be brought out to one common GND plane.
10. These are the ISSP pins, which are not High Z at POR. See the *PSoC Technical Reference Manual* for details.

28-pin Part Pinout

Figure 6. CY8C21534 28-pin PSoC Device



CY8C21534 28-pin SSOP Pin Definitions

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input and column output
3	I/O	I, M	P0[3]	Analog column mux input and column output, integrating input
4	I/O	I, M	P0[1]	Analog column mux input, integrating input
5	I/O	M	P2[7]	
6	I/O	M	P2[5]	
7	I/O	I, M	P2[3]	Direct switched capacitor block input
8	I/O	I, M	P2[1]	Direct switched capacitor block input
9	Power		V_{SS}	Ground connection [13]
10	I/O	M	P1[7]	I^2C SCL
11	I/O	M	P1[5]	I^2C SDA
12	I/O	M	P1[3]	
13	I/O	M	P1[1]	I^2C SCL, ISSP-SCLK[14]
14	Power		V_{SS}	Ground connection [13]
15	I/O	M	P1[0]	I^2C SDA, ISSP-SDATA[14]
16	I/O	M	P1[2]	
17	I/O	M	P1[4]	Optional external clock input (EXTCLK)
18	I/O	M	P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	I, M	P2[0]	Direct switched capacitor block input
21	I/O	I, M	P2[2]	Direct switched capacitor block input
22	I/O	M	P2[4]	
23	I/O	M	P2[6]	
24	I/O	I, M	P0[0]	Analog column mux input
25	I/O	I, M	P0[2]	Analog column mux input
26	I/O	I, M	P0[4]	Analog column mux input
27	I/O	I, M	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage

LEGEND A: Analog, I: Input, O = Output, and M = Analog Mux Input.

Notes
13. All V_{SS} pins should be brought out to one common GND plane.
14. These are the ISSP pins, which are not high Z at POR. See the *PSoC Technical Reference Manual* for details.

32-pin Part Pinout

Figure 7. CY8C21434 32-pin PSoC Device

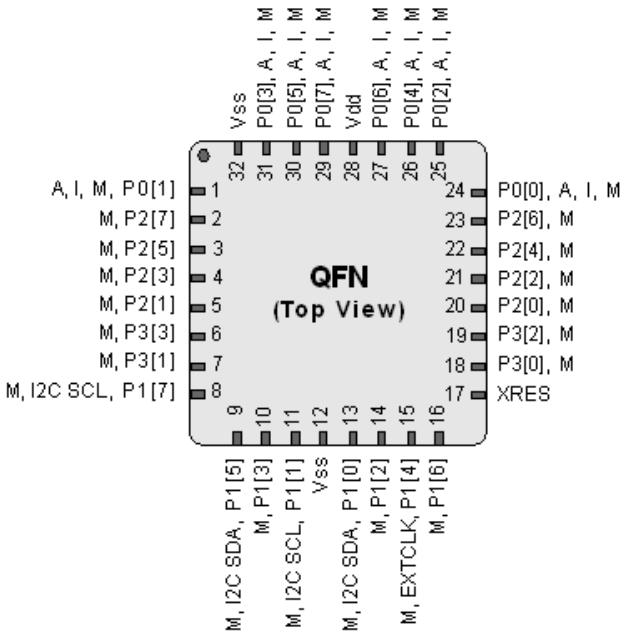


Figure 7. CY8C21634 32-pin PSoC Device

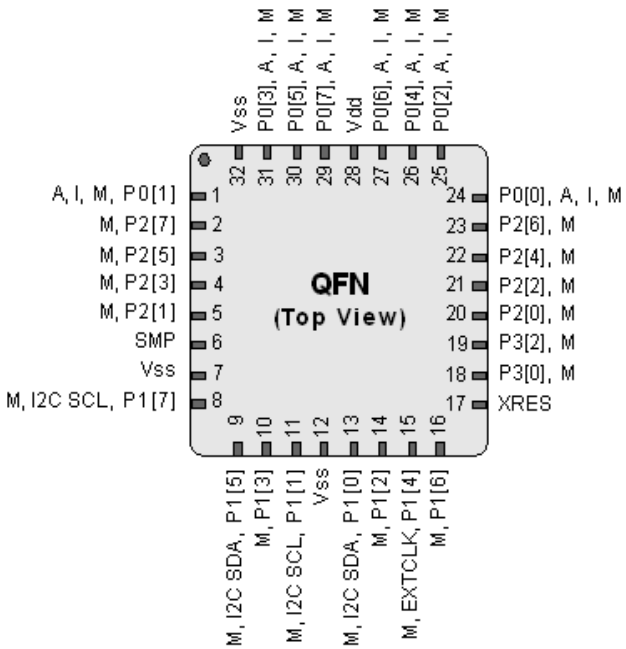


Figure 8. CY8C21434 32-pin Sawn PSoC Device Sawn

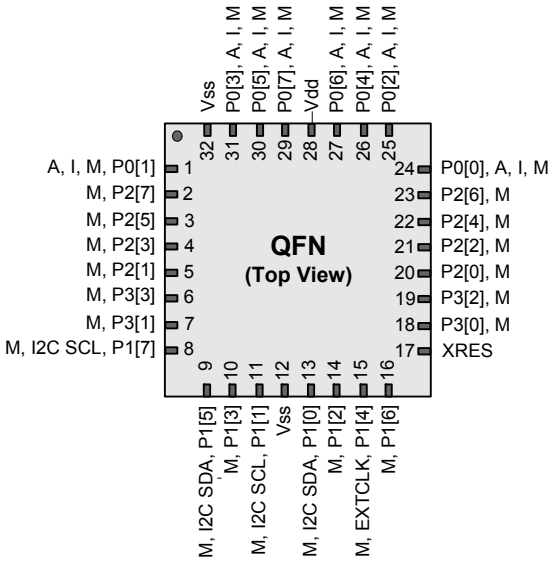
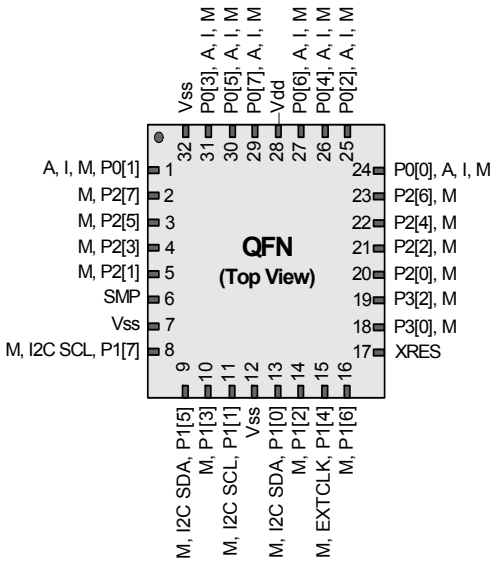


Figure 9. CY8C21634 32-pin Sawn PSoC Device Sawn



CY8C21434/CY8C21634 32-pin QFN Pin Definitions

Pin No. [15]	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[1]	Analog column mux input, integrating input
2	I/O	M	P2[7]	
3	I/O	M	P2[5]	
4	I/O	M	P2[3]	
5	I/O	M	P2[1]	
6	I/O	M	P3[3]	In CY8C21434 part
6	Power		SMP	SMP connection to required external components in CY8C21634 part
7	I/O	M	P3[1]	In CY8C21434 part
7	Power		V_{SS}	Ground connection in CY8C21634 part [16]
8	I/O	M	P1[7]	I^2C SCL
9	I/O	M	P1[5]	I^2C SDA
10	I/O	M	P1[3]	
11	I/O	M	P1[1]	I^2C SCL, ISSP-SCLK[17]
12	Power		V_{SS}	Ground connection [16]
13	I/O	M	P1[0]	I^2C SDA, ISSP-SDATA[17]
14	I/O	M	P1[2]	
15	I/O	M	P1[4]	Optional external clock input (EXTCLK)
16	I/O	M	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	M	P3[0]	
19	I/O	M	P3[2]	
20	I/O	M	P2[0]	
21	I/O	M	P2[2]	
22	I/O	M	P2[4]	
23	I/O	M	P2[6]	
24	I/O	I, M	P0[0]	Analog column mux input
25	I/O	I, M	P0[2]	Analog column mux input
26	I/O	I, M	P0[4]	Analog column mux input
27	I/O	I, M	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage
29	I/O	I, M	P0[7]	Analog column mux input
30	I/O	I, M	P0[5]	Analog column mux input
31	I/O	I, M	P0[3]	Analog column mux input, integrating input
32	Power		V_{SS}	Ground connection [16]

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Notes
15. The center pad on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
16. All V_{SS} pins should be brought out to one common GND plane.
17. These are the ISSP pins, which are not high Z at POR. See the *PSoC Technical Reference Manual* for details.

Register Reference

This chapter lists the registers of the CY8C21x34 PSoC device. For detailed register information, see the *PSoC Technical Reference Manual*.

Register Conventions

The register conventions specific to this section are listed in Table 2.

Table 2. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set to 1, the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and must not be accessed.

Table 11. DC Switch Mode Pump (SMP) Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
E_2	Efficiency	35	80	–	%	For I load = 1mA, V_{PUMP} = 2.55 V, V_{BAT} = 1.3 V, 10 µH inductor, 1 µF capacitor, and Schottky diode
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

DC Analog Mux Bus Specifications

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 12. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400 800	Ω	V_{DD} ≥ 2.7 V 2.4 V ≤ V_{DD} ≤ 2.7 V
R_{VDD}	Resistance of initialization switch to V_{DD}	–	–	800	Ω	

DC POR and LVD Specifications

Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 13. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 2.5 V during startup, the reset from the XRES pin, or reset from watchdog
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.70	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[21]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[22]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	
	V_{DD} value for pump trip					
V_{PUMP0}	VM[2:0] = 000b	2.45	2.55	2.62[23]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[24]	V	
V_{PUMP4}	VM[2:0] = 100b	4.54	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.62	4.73	4.83	V	
V_{PUMP6}	VM[2:0] = 110b	4.71	4.82	4.92	V	
V_{PUMP7}	VM[2:0] = 111b	4.89	5.00	5.12	V	

Notes
21. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
22. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
23. Always greater than 50 mV above V_{LVD0}.
24. Always greater than 50 mV above V_{LVD3}.

DC Programming Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 14. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	2.7		5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[25]	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash endurance (total)[26]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I^2C Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤T_A ≤85 °C, 3.0 V to 3.6 V and –40 °C ≤T_A ≤85 °C, or 2.4 V to 3.0 V and –40 °C ≤T_A ≤85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 15. DC I^2C Specifications[27]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	2.4 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	2.4 V ≤ V_{DD} ≤ 5.25 V

Notes

25. The 50,000 cycle flash endurance per block is only guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V, and 4.75 V to 5.25 V.
26. A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36×2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and ensure that no single block ever sees more than 50,000 cycles). For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note AN2015 (Design Aids - Reading and Writing PSoC® Flash) for more information.
27. All GPIO meet the DC GPIO VIL and VIH specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the above specs.

AC Electrical Characteristics

AC Chip-Level Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 16. 5-V and 3.3-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24} [28]	IMO frequency for 24 MHz	23.4	24	24.6[29,30]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 14 on page 20. SLIMO mode = 0
F_{IMO6} [28]	IMO frequency for 6 MHz	5.52	6	6.48 [29,30]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See Figure 14 on page 20. SLIMO mode = 1
F_{CPU1}	CPU frequency (5 V nominal)	0.091	24	24.6[29]	MHz	24 MHz only for SLIMO mode = 0
F_{CPU2}	CPU frequency (3.3 V nominal)	0.091	12	12.3[30]	MHz	SLIMO mode = 0
F_{BLK5}	Digital PSoC block frequency (5 V nominal)	0	48	49.2[29,31]	MHz	Refer to AC Digital Block Specifications on page 29
F_{BLK33}	Digital PSoC block frequency (3.3 V nominal)	0	24	24.6[31]	MHz	
F_{32K1}	ILO frequency	15	32	64	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the system resets section of the *PSoC Technical Reference Manual* for details on this timing
t_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	46.8	48.0	49.2[29,30]	MHz	Trimmed. Using factory trim values
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the *PSoC Technical Reference Manual*
t_{jit_IMO}	24-MHz IMO cycle-to-cycle jitter (RMS)[32]	–	200	700	ps	
	24-MHz IMO long term N cycle-to-cycle jitter (RMS)[32]	–	300	900	ps	N = 32
	24-MHz IMO period jitter (RMS)[32]	–	100	400	ps	

Notes
28. Errata: The worst case IMO frequency deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
29. 4.75 V < V_{DD} < 5.25 V.
30. 3.0 V < V_{DD} < 3.6 V. See application note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3 V.
31. See the individual user module datasheets for information on maximum frequencies for user modules.
32. Refer to Cypress Jitter Specifications Application Note AN5054 “Understanding Datasheet Jitter Specifications for Cypress Timing Products” at www.cypress.com under Application Notes for more information.

AC General Purpose I/O Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

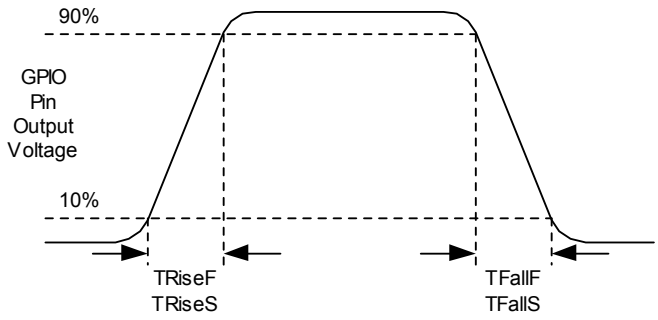
Table 18. 5-V and 3.3-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal strong mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% to 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% to 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	7	27	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	7	22	–	ns	V_{DD} = 3 to 5.25 V, 10% to 90%

Table 19. 2.7 V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	3	MHz	Normal strong mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10% to 90%

Figure 13. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 20. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP}	Comparator mode response time, 50 mV overdrive	–	–	100 200	ns ns	V_{DD} ≥ 3.0 V 2.4 V < V_{DD} < 3.0 V

AC Digital Block Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 21. 5-V and 3.3-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No capture, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With capture	–	–	24.6	MHz	
	Capture pulse width	50[37]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With enable input	–	–	24.6	MHz	
	Enable input pulse width	50[37]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[37]	–	–	ns	
	Disable mode	50[37]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[37]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	

Note
37. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 22. 2.7-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block input clock frequency	–	–	12.7	MHz	2.4 V < V_{DD} < 3.0 V
Timer	Capture pulse width	100[38]	–	–	ns	
	Input clock frequency, with or without capture	–	–	12.7	MHz	
Counter	Enable input pulse width	100	–	–	ns	
	Input clock frequency, no enable input	–	–	12.7	MHz	
	Input clock frequency, enable input	–	–	12.7	MHz	
Dead Band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	100	–	–	ns	
	Disable mode	100	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	
CRCPRS (PRS Mode)	Input clock frequency	–	–	12.7	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	12.7	MHz	
SPIM	Input clock frequency	–	–	6.35	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	
	Width of SS_ Negated between transmissions	100	–	–	ns	
Transmitter	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 23. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Note
38. 100 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

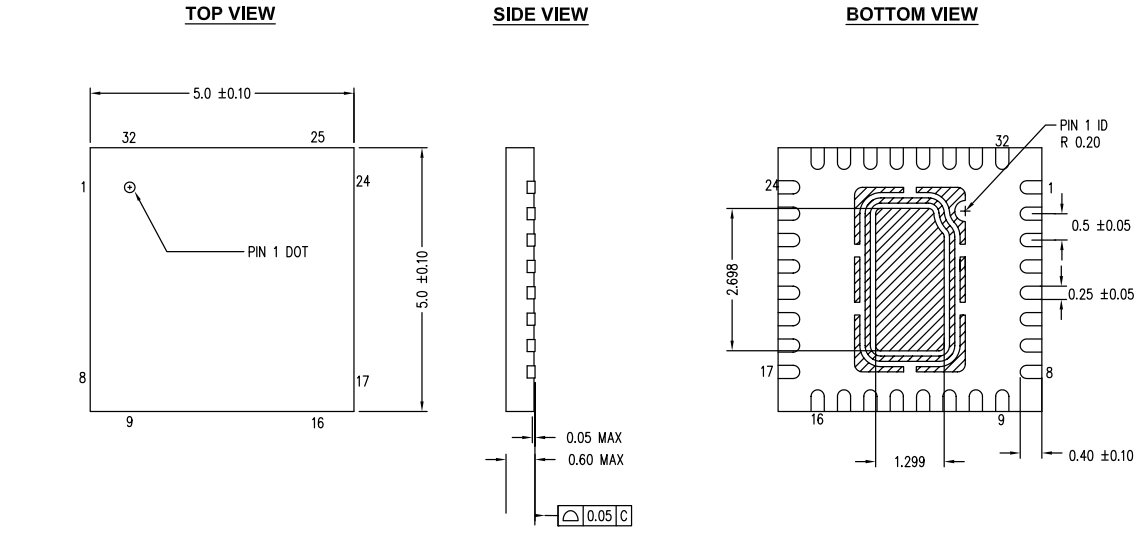
Table 24. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 25. 2.7-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

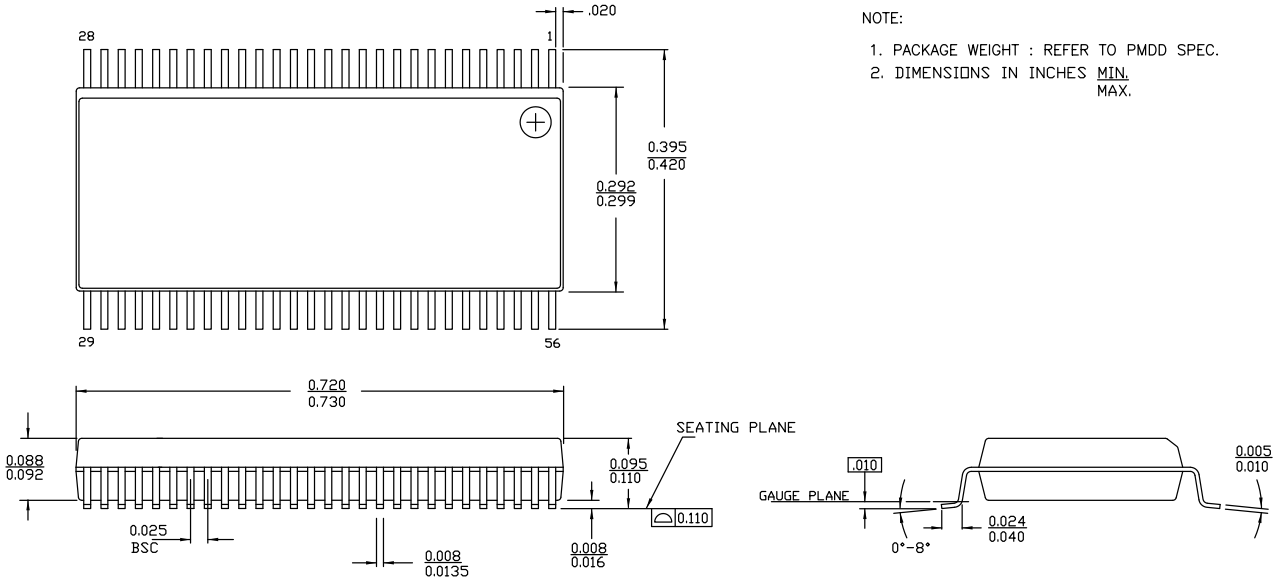
Figure 19. 32-pin QFN (5 × 5 × 0.55 mm) LQ32A 1.3 × 2.7 E-Pad (Sawn Type) Package Outline, 001-48913



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 38mg ± 4 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-48913 *D

Figure 20. 56-pin SSOP (300 Mils) Package Outline, 51-85062



NOTE:
1. PACKAGE WEIGHT : REFER TO PMDD SPEC.
2. DIMENSIONS IN INCHES MIN.
MAX.

51-85062 *F

Development Tool Selection

This section presents the development tools available for all current PSoC device families including the CY8C21x34 family.

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com and includes a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation, and the software interface allows you to run, halt, and single step the processor, and view the content of specific memory locations. Advance emulation features also supported through PSoC Designer. The kit includes:

- PSoC Designer software CD
- ICE-Cube in-circuit emulator
- ICE Flex-Pod for CY8C29x66 family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240 V power supply, Euro-Plug adapter
- iMAGEcraft C compiler
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466-24PXI 28-PDIP chip samples

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows you to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-pin CY8C29466-24PXI PDIP PSoC device sample
- 28-pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- Two 28-pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. The board includes both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB board
- LCD module
- MIniProg programming unit
- Mini USB cable
- PSoC Designer and example projects CD
- Getting Started guide
- Wire pack

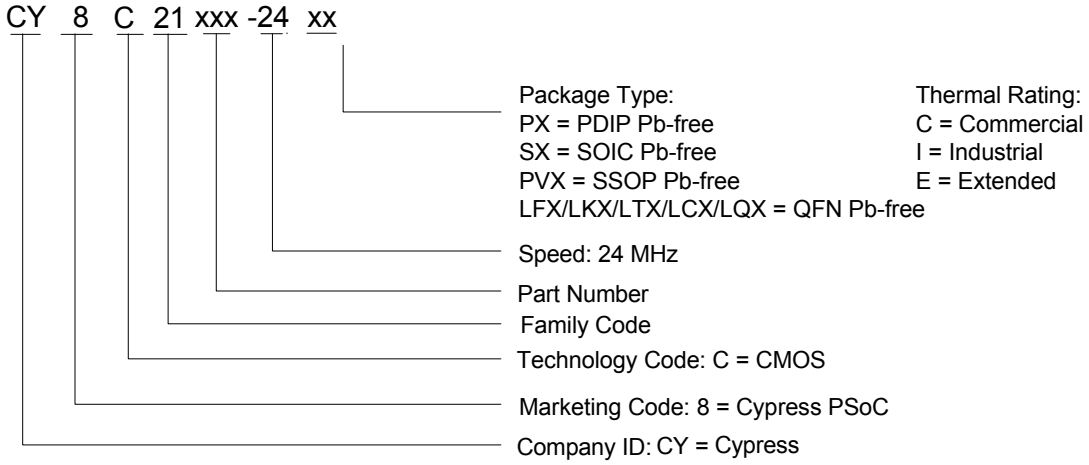
Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
16-Pin (150-Mil) SOIC	CY8C21234-24SXI	8 K	512	Yes	–40 °C to +85 °C	4	4	12	12[47]	0	No
16-Pin (150-Mil) SOIC (Tape and Reel)	CY8C21234-24SXIT	8 K	512	Yes	–40 °C to +85 °C	4	4	12	12[47]	0	No
20-Pin (210-Mil) SSOP	CY8C21334-24PVXI	8 K	512	No	–40 °C to +85 °C	4	4	16	16[47]	0	Yes
20-Pin (210-Mil) SSOP (Tape and Reel)	CY8C21334-24PVXIT	8 K	512	No	–40 °C to +85 °C	4	4	16	16[47]	0	Yes
28-Pin (210-Mil) SSOP	CY8C21534-24PVXI	8 K	512	No	–40 °C to +85 °C	4	4	24	24[47]	0	Yes
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C21534-24PVXIT	8 K	512	No	–40 °C to +85 °C	4	4	24	24[47]	0	Yes
32-Pin (5 × 5 mm 1.00 max) Sawn QFN	CY8C21434-24LTXI	8 K	512	No	–40 °C to +85 °C	4	4	28	28[47]	0	Yes
32-Pin (5 × 5 mm 1.00 max) Sawn QFN [48] (Tape and Reel)	CY8C21434-24LTXIT	8 K	512	No	–40 °C to +85 °C	4	4	28	28[47]	0	Yes
32-Pin (5 × 5 mm 0.60 max) Thin Sawn QFN	CY8C21434-24LQXI	8 K	512	No	–40 °C to +85 °C	4	4	28	28[47]	0	Yes
32-Pin (5 × 5 mm 0.60 max) Thin Sawn QFN (Tape and Reel)	CY8C21434-24LQXIT	8 K	512	No	–40 °C to +85 °C	4	4	28	28[47]	0	Yes
32-Pin (5 × 5 mm 1.00 max) Sawn QFN [48]	CY8C21634-24LTXI	8 K	512	Yes	–40 °C to +85 °C	4	4	26	26[47]	0	Yes
32-Pin (5 × 5 mm 1.00 max) Sawn QFN [48] (Tape and Reel)	CY8C21634-24LTXIT	8 K	512	Yes	–40 °C to +85 °C	4	4	26	26[47]	0	Yes
56-Pin OCD SSOP	CY8C21001-24PVXI	8 K	512	Yes	–40 °C to +85 °C	4	4	26	26[47]	0	Yes
	CY8C21434-12X14I	Please contact sales office or Field Applications Engineer (FAE) for more information.									

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Notes
47. All Digital I/O Pins also connect to the common analog mux.
48. Refer to the section 32-pin Part Pinout on page 12 for pin differences.

Ordering Code Definitions



Document Conventions

Units of Measure

Table 33 lists the units of measures.

Table 33. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	µH	micro henry
dB	decibels	µs	microsecond
°C	degree Celsius	ms	millisecond
µF	microfarad	ns	nanosecond
fF	femto farad	ps	picosecond
pF	picofarad	µV	microvolt
kHz	kilohertz	mV	millivolts
MHz	megahertz	mVpp	millivolts peak-to-peak
rt-Hz	root hertz	nV	nano volt
kΩ	kilo ohm	V	volt
Ω	ohm	µW	microwatt
µA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nano ampere	ppm	parts per million
pA	pico ampere	%	percent
mH	millihenry		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Errata

This section describes the errata for the PSoC® Programmable System-on-Chip CY8C21X34. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8C21X34	CY8C21234-24SXI
	CY8C21234-24SXIT
	CY8C21334-24PVXI
	CY8C21334-24PVXIT
	CY8C21534-24PVXI
	CY8C21534-24PVXIT
	CY8C21434-24LFXI
	CY8C21434-24LFXIT
	CY8C21434-24LKXI
	CY8C21434-24LKXIT
	CY8C21634-24LFXI
	CY8C21634-24LFXIT
	CY8C21434-24LTXI
	CY8C21434-24LTXIT
	CY8C21434-24LQXI
	CY8C21434-24LQXIT
	CY8C21634-24LTXI
	CY8C21634-24LTXIT
	CY8C21001-24PVXI

CY8C21X34 Qualification Status

Product Status: Production

Document History Page

Document Title: CY8C21634/CY8C21534/CY8C21434/CY8C21334/CY8C21234, PSoC® Programmable System-on-Chip™ Document Number: 38-12025				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	227340	HMT	See ECN	New silicon and document (Revision **).
*A	235992	SFV	See ECN	Updated Overview and Electrical Spec. chapters, along with revisions to the 24-Pin pinout part. Revised the register mapping tables. Added a SSOP 28-Pin part.
*B	248572	SFV	See ECN	Changed title to include all part #s. Changed 28-Pin SSOP from CY8C21434 to CY8C21534. Changed pin 9 on the 28-Pin SSOP from SMP pin to Vss pin. Added SMP block to architecture diagram. Update Electrical Specifications. Added another 32-Pin MLF part: CY8C21634.
*C	277832	HMT	See ECN	Verify datasheet standards from SFV memo. Add Analog Input Mux to applicable pin outs. Update PSoC Characteristics table. Update diagrams and specs. Final.
*D	285293	HMT	See ECN	Update 2.7 V DC GPIO spec. Add Reflow Peak Temp. table.
*E	301739	HMT	See ECN	DC Chip-Level Specification changes. Update links to new CY.com Portal.
*F	329104	HMT	See ECN	Re-add pinout ISSP notation. Fix TMP register names. Clarify ADC feature. Update Electrical Specifications. Update Reflow Peak Temp. table. Add 32 MLF E-PAD dimensions. Add ThetaJC to Thermal Impedance table. Fix 20-Pin package order number. Add CY logo. Update CY copyright.
*G	352736	HMT	See ECN	Add new color and logo. Add URL to preferred dimensions for mounting MLF packages. Update Transmitter and Receiver AC Digital Block Electrical Specifications.
*H	390152	HMT	See ECN	Clarify MLF thermal pad connection info. Replace 16-Pin 300-MIL SOIC with correct 150-MIL.
*I	413404	HMT	See ECN	Update 32-Pin QFN E-Pad dimensions and rev. *A. Update CY branding and QFN convention.
*J	430185	HMT	See ECN	Add new 32-Pin 5x5 mm 0.60 thickness QFN package and diagram, CY8C21434-24LKXI. Update thermal resistance data. Add 56-Pin SSOP on-chip debug non-production part, CY8C21001-24PVXI. Update typical and recommended Storage Temperature per industrial specs. Update copyright and trademarks.
*K	677717	HMT	See ECN	Add CapSense SNR requirement reference. Add new Dev. Tool section. Add CY8C20x34 to PSoC Device Characteristics table. Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Update rev. of 32-Lead (5x5 mm 0.60 MAX) QFN package diagram.
*L	2147847	UVS / PYRS	02/27/08	Added 32-Pin QFN Sawn pin diagram, package diagram, and ordering information.
*M	2273246	UVS / AESA	04/01/08	Added 32 pin thin sawn package diagram.
*N	2618124	OGNE / PYRS	12/09/08	Added Note in Ordering Information section. Changed title from PSoC Mixed-Signal Array to PSoC Programmable System-on-Chip
*O	2684145	SNV / AESA	04/06/2009	Updated 32-Pin Sawn QFN package dimension for CY8C21434-24LTXIT Updated Getting Started, Development Tools, and Designing with PSoC Designer Sections
*P	2693024	DPT / PYRS	04/16/2009	Updated 32-Pin Sawn QFN package diagram
*Q	2720594	BRW	06/22/09	Corrected ohm symbol and parenthesis in figure caption (Fig.25) Removed references to mixed-sginal array from the text. Updated Development Tools Selection section.