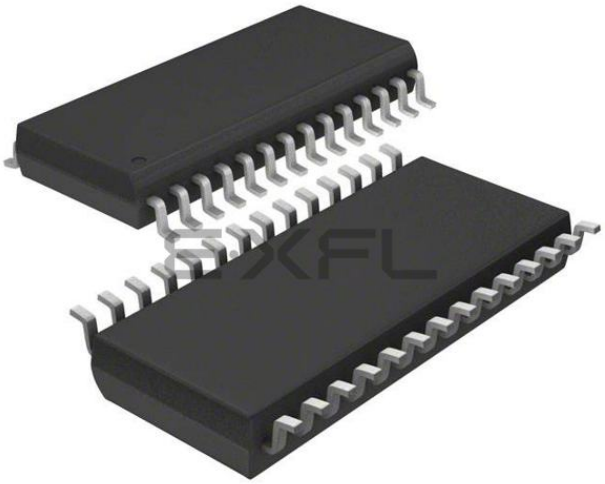

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | M8C |
| Core Size | 8-Bit |
| Speed | 12MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 24 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 5.25V |
| Data Converters | A/D 28x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21534-12pvxet |

## PSoC Functional Overview

The PSoC family consists of many devices with on-chip controllers. These devices are designed to replace multiple traditional microcontroller unit (MCU)-based system components with one, low-cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture makes it possible for you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture, as illustrated in the Logic Block Diagram on page 1, comprises of four main areas: the core, the system resources, the digital system, and the analog system. Configurable global bus resources allow all the device resources to be combined into a complete custom system. Each CY8C21x34 PSoC device includes four digital blocks and four analog blocks. Depending on the PSoC package, up to 24 GPIOs are also included. The GPIOs provide access to the global digital and analog interconnects.

### The PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep, and watchdog timers, and an internal main oscillator (IMO) and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a two-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor.

System resources provide additional capability, such as digital clocks for increased flexibility, $I^2C$ functionality for implementing an $I^2C$ master, slave, or multi-master, an internal voltage reference that provides an absolute value of 1.3 V to a number of PSoC subsystems, and various system resets supported by the M8C.

The digital system is composed of an array of digital PSoC blocks, which can be configured into any number of digital peripherals. The digital blocks can be connected to the GPIO through a series of global buses that can route any signal to any pin. This frees designs from the constraints of a fixed peripheral controller.

The analog system is composed of four analog PSoC blocks, supporting comparators and analog-to-digital conversion with up to 10 bits of precision.

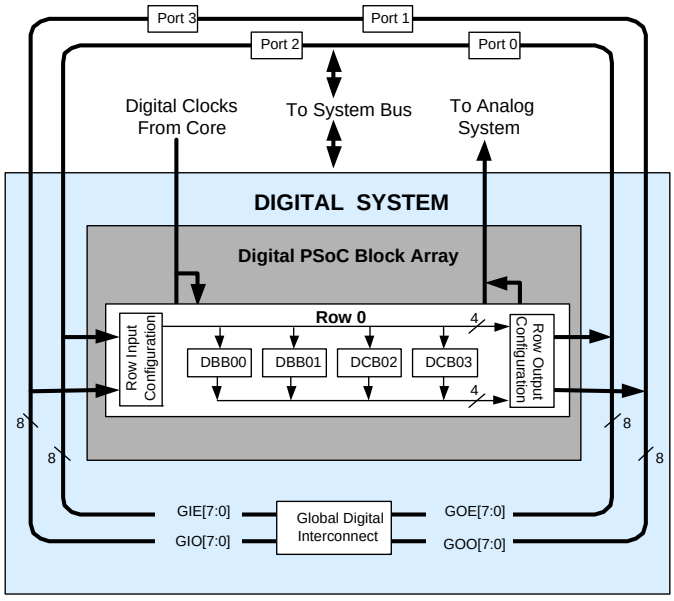
### The Digital System

The digital system is composed of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include those listed.

- PWMs (8- to 32-bit)
- PWMs with dead band (8- to 24-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- Full or half-duplex 8-bit UART with selectable parity
- SPI master and slave
- $I^2C$ master, slave, or multi-master (implemented in a dedicated $I^2C$ block)
- Cyclical redundancy checker/generator (16-bit)
- Infrared Data Association (IrDA)
- PRS generators (8- to 32-bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

**Figure 1. Digital System Block Diagram**




Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows you the optimum choice of system resources for your application. Family resources are shown in Table 1 on page 5.

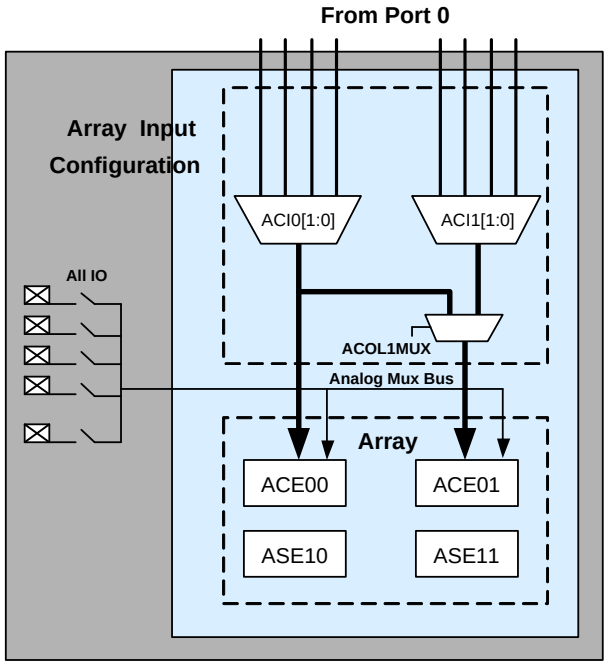
## The Analog System

The analog system is composed of four configurable blocks, allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the common PSoC analog functions for this device (most available as user modules) are listed.

- ADCs (single or dual, with up to 10-bit resolution)
- Pin-to-pin comparator
- Single-ended comparators (up to two) with absolute (1.3 V) reference or 8-bit DAC reference
- 1.3 V reference (as a system resource)

In most PSoC devices, analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks. The CY8C21x34 devices provide limited functionality type ‘E’ analog blocks. Each column contains one CT type ‘E’ block and one SC type ‘E’ block. Refer to the *PSoC Programmable System-on-Chip Technical Reference Manual* for detailed information on the CY8C21x34’s type ‘E’ analog blocks.

**Figure 2. Analog System Block Diagram**




*The Analog Multiplexer System*

The analog mux bus can connect to every GPIO pin. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and ADCs. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combination.

## Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful for complete systems. Brief statements describing the merits of each system resource are presented.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The $I^2C$ module provides communication up to 400 kHz over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal 1.3-V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system

### PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have a varying number of digital and analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC device covered by this data sheet is highlighted in Table 1.

**Table 1. PSoC Device Characteristics**

| PSoC Part Number | Digital I/O | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size |
|---|---|---|---|---|---|---|---|---|---|
| CY8C29x66[1] | up to 64 | 4 | 16 | up to 12 | 4 | 4 | 12 | 2 K | 32 K |
| CY8C28xxx | up to 44 | up to 3 | up to 12 | up to 44 | up to 4 | up to 6 | up to 12 + 4[2] | 1 K | 16 K |
| CY8C27x43 | up to 44 | 2 | 8 | up to 12 | 4 | 4 | 12 | 256 | 16 K |
| CY8C24x94[1] | up to 56 | 1 | 4 | up to 48 | 2 | 2 | 6 | 1 K | 16 K |
| CY8C24x23A[1] | up to 24 | 1 | 4 | up to 12 | 2 | 2 | 6 | 256 | 4 K |
| CY8C23x33 | up to 26 | 1 | 4 | up to 12 | 2 | 2 | 4 | 256 | 8 K |
| CY8C22x45[1] | up to 38 | 2 | 8 | up to 38 | 0 | 4 | 6[2] | 1 K | 16 K |
| CY8C21x45[1] | up to 24 | 1 | 4 | up to 24 | 0 | 4 | 6[2] | 512 | 8 K |
| CY8C21x34[1] | up to 28 | 1 | 4 | up to 28 | 0 | 2 | 4[2] | 512 | 8 K |
| CY8C21x23 | up to 16 | 1 | 4 | up to 8 | 0 | 2 | 4[2] | 256 | 4 K |
| CY8C20x34[1] | up to 28 | 0 | 0 | up to 28 | 0 | 0 | 3[2,3] | 512 | 8 K |
| CY8C20xx6 | up to 36 | 0 | 0 | up to 36 | 0 | 0 | 3[2,3] | up to 2 K | up to 32 K |

## Getting Started

For in-depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

### Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

### Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

### Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

### CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

### Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

### Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

**Notes**
1. Automotive qualified devices available in this group.
2. Limited analog functionality.
3. Two analog blocks and one CapSense® block.

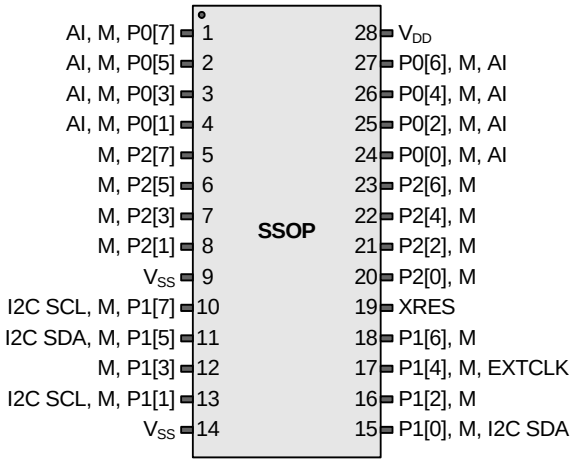
## 28-pin Part Pinout

### Table 3. 28-pin Part Pinout (SSOP)

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | I/O | I, M | P0[7] | Analog column mux input |
| 2 | I/O | I, M | P0[5] | Analog column mux input |
| 3 | I/O | I, M | P0[3] | Analog column mux input, $C_{MOD}$ capacitor pin |
| 4 | I/O | I, M | P0[1] | Analog column mux input, $C_{MOD}$ capacitor pin |
| 5 | I/O | M | P2[7] | |
| 6 | I/O | M | P2[5] | |
| 7 | I/O | M | P2[3] | |
| 8 | I/O | M | P2[1] | |
| 9 | Power | | $V_{SS}$ | Ground connection |
| 10 | I/O | M | P1[7] | $I^2C$ serial clock (SCL) |
| 11 | I/O | M | P1[5] | $I^2C$ serial data (SDA) |
| 12 | I/O | M | P1[3] | |
| 13 | I/O | M | P1[1] | $I^2C$ serial clock (SCL), ISSP-SCLK[5] |
| 14 | Power | | $V_{SS}$ | Ground connection |
| 15 | I/O | M | P1[0] | $I^2C$ serial data (SDA), ISSP-SDATA[5] |
| 16 | I/O | M | P1[2] | |
| 17 | I/O | M | P1[4] | Optional external clock (EXTCLK) input |
| 18 | I/O | M | P1[6] | |
| 19 | Input | | XRES | Active high external reset with internal pull-down |
| 20 | I/O | M | P2[0] | |
| 21 | I/O | M | P2[2] | |
| 22 | I/O | M | P2[4] | |
| 23 | I/O | M | P2[6] | |
| 24 | I/O | I, M | P0[0] | Analog column mux input |
| 25 | I/O | I, M | P0[2] | Analog column mux input |
| 26 | I/O | I, M | P0[4] | Analog column mux input |
| 27 | I/O | I, M | P0[6] | Analog column mux input |
| 28 | Power | | $V_{DD}$ | Supply voltage |

**LEGEND** A = Analog, I = Input, O = Output, and M = Analog Mux Input.

### Figure 4. CY8C21534 28-pin PSoC Device




**Note**
5. These are the ISSP pins, which are not high Z when coming out of POR. See the *PSoC Technical Reference Manual* for details.

# Registers

## Register Conventions

This section lists the registers of the automotive CY8C21x34 PSoC device. For detailed register information, reference the *PSoC Technical Reference Manual*.

The register conventions specific to this section are listed in Table 4.

**Table 4. Register Conventions**

| Convention | Description |
|---|---|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

## Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are Reserved and must not be accessed.

**Table 5. Register Map 0 Table: User Space**

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DR | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0GS | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1GS | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | | 87 | | | C7 | |
| PRT2DR | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2IE | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2GS | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2DM2 | 0B | RW | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | CUR_PP | D0 | RW |
| | 11 | | | 51 | | | 91 | | STK_PP | D1 | RW |
| | 12 | | | 52 | | | 92 | | | D2 | |
| | 13 | | | 53 | | | 93 | | IDX_PP | D3 | RW |
| | 14 | | | 54 | | | 94 | | MVR_PP | D4 | RW |
| | 15 | | | 55 | | | 95 | | MVW_PP | D5 | RW |
| | 16 | | | 56 | | | 96 | | I2C_CFG | D6 | RW |
| | 17 | | | 57 | | | 97 | | I2C_SCR | D7 | # |
| | 18 | | | 58 | | | 98 | | I2C_DR | D8 | RW |
| | 19 | | | 59 | | | 99 | | I2C_MSCR | D9 | # |
| | 1A | | | 5A | | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | | 5B | | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | | 5E | | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | | 5F | | | 9F | | | DF | |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | AMUX_CFG | 61 | RW | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | PWM_CR | 62 | RW | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | | 63 | | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | | E4 | |
| DBB01DR1 | 25 | W | | 65 | | | A5 | | | E5 | |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | ADC0_CR | 68 | # | | A8 | | | E8 | |
| DCB02DR1 | 29 | W | ADC1_CR | 69 | # | | A9 | | | E9 | |
| DCB02DR2 | 2A | RW | | 6A | | | AA | | | EA | |
| DCB02CR0 | 2B | # | | 6B | | | AB | | | EB | |
| DCB03DR0 | 2C | # | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03DR1 | 2D | W | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03DR2 | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| DCB03CR0 | 2F | # | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACE01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | DAC_D | FD | RW |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and must not be accessed. # Access is bit specific.

**Table 6. Register Map 1 Table: Configuration Space**

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DM0 | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0DM1 | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0IC0 | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0IC1 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DM0 | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1DM1 | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1IC0 | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1IC1 | 07 | RW | | 47 | | | 87 | | | C7 | |
| PRT2DM0 | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2DM1 | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2IC0 | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2IC1 | 0B | RW | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | GDI_O_IN | D0 | RW |
| | 11 | | | 51 | | | 91 | | GDI_E_IN | D1 | RW |
| | 12 | | | 52 | | | 92 | | GDI_O_OU | D2 | RW |
| | 13 | | | 53 | | | 93 | | GDI_E_OU | D3 | RW |
| | 14 | | | 54 | | | 94 | | | D4 | |
| | 15 | | | 55 | | | 95 | | | D5 | |
| | 16 | | | 56 | | | 96 | | | D6 | |
| | 17 | | | 57 | | | 97 | | | D7 | |
| | 18 | | | 58 | | | 98 | | MUX_CR0 | D8 | RW |
| | 19 | | | 59 | | | 99 | | MUX_CR1 | D9 | RW |
| | 1A | | | 5A | | | 9A | | MUX_CR2 | DA | RW |
| | 1B | | | 5B | | | 9B | | MUX_CR3 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | OSC_GO_EN | DD | RW |
| | 1E | | | 5E | | | 9E | | OSC_CR4 | DE | RW |
| | 1F | | | 5F | | | 9F | | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | CMP_GO_EN | 64 | RW | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | ADC0_TR | E5 | RW |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | ADC1_TR | E6 | RW |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | | E7 | |
| DCB02FN | 28 | RW | | 68 | | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | | 69 | | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | CLK_CR3 | 6B | RW | | AB | | ECO_TR | EB | W |
| DCB03FN | 2C | RW | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03IN | 2D | RW | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03OU | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| | 2F | | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACE01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | DAC_CR | FD | RW |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and must not be accessed. # Access is bit specific.

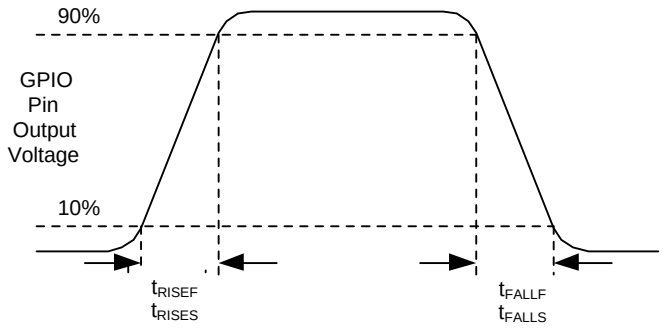
*AC GPIO Specifications*

Table 16 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

**Table 16. AC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO operating frequency | 0 | – | 12.6[14] | MHz | Normal Strong Mode |
| $t_{RISEF}$ | Rise time, normal strong mode, Cload = 50 pF | 2 | – | 22 | ns | 10% to 90% |
| $t_{FALLF}$ | Fall time, normal strong mode, Cload = 50 pF | 2 | – | 22 | ns | 10% to 90% |
| $t_{RISES}$ | Rise time, slow strong mode, Cload = 50 pF | 7 | 27 | – | ns | 10% to 90% |
| $t_{FALLS}$ | Fall time, slow strong mode, Cload = 50 pF | 7 | 22 | – | ns | 10% to 90% |

**Figure 7. GPIO Timing Diagram**




*AC Operational Amplifier Specifications*

Table 17 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

**Table 17. AC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{COMP}$ | Comparator mode response time, 50 mV overdrive | – | – | 150 | ns | |

**Note**
14. Accuracy derived from Internal Main Oscillator with appropriate trim for $V_{DD}$ range.

*AC Digital Block Specifications*

Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

**Table 18. AC Digital Block Specifications**

| Function | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| All functions | Block input clock frequency | – | – | 25.2[16] | MHz | |
| Timer | Input clock frequency | | | | | |
| | No capture | – | – | 25.2[16] | MHz | |
| | With capture | – | – | 25.2[16] | MHz | |
| | Capture pulse width | 50[15] | – | – | ns | |
| Counter | Input clock frequency | | | | | |
| | No enable input | – | – | 25.2[16] | MHz | |
| | With enable input | – | – | 25.2[16] | MHz | |
| | Enable input pulse width | 50[15] | – | – | ns | |
| Dead Band | Kill pulse width | | | | | |
| | Asynchronous restart mode | 20 | – | – | ns | |
| | Synchronous restart mode | 50[15] | – | – | ns | |
| | Disable mode | 50[15] | – | – | ns | |
| | Input clock frequency | – | – | 25.2[16] | MHz | |
| CRCPRS (PRS Mode) | Input clock frequency | – | – | 25.2[16] | MHz | |
| CRCPRS (CRC Mode) | Input clock frequency | – | – | 25.2[16] | MHz | |
| SPIM | Input clock frequency | – | – | 4.2[16] | MHz | The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2. |
| SPIS | Input clock (SCLK) frequency | – | – | 2.1[16] | MHz | The input clock is the SPI SCLK in SPIS mode. |
| | Width of SS_ negated between transmissions | 50[15] | – | – | ns | |
| Transmitter | Input clock frequency | – | – | 8.4[16] | MHz | The baud rate is equal to the input clock frequency divided by 8. |
| Receiver | Input clock frequency | – | – | 25.2[16] | MHz | The baud rate is equal to the input clock frequency divided by 8. |

**Note**
15. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).
16. Accuracy derived from IMO with appropriate trim for $V_{DD}$ range.

*AC External Clock Specifications*

Table 19 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

**Table 19. AC External Clock Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency | 0.093 | – | 24.24 | MHz | |
| – | High period | 20.6 | – | 5300 | ns | |
| – | Low period | 20.6 | – | – | ns | |
| – | Power-up IMO to switch | 150 | – | – | µs | |

*AC Programming Specifications*

Table 20 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

**Table 20. AC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{RSCLK}$ | Rise time of SCLK | 1 | – | 20 | ns | |
| $t_{FSCLK}$ | Fall time of SCLK | 1 | – | 20 | ns | |
| $t_{SSCLK}$ | Data setup time to falling edge of SCLK | 40 | – | – | ns | |
| $t_{HSCLK}$ | Data hold time from falling edge of SCLK | 40 | – | – | ns | |
| $F_{SCLK}$ | Frequency of SCLK | 0 | – | 8 | MHz | |
| $t_{ERASEB}$ | Flash erase time (block) | – | 10 | 40[17] | ms | |
| $t_{WRITE}$ | Flash block write time | – | 40 | 160[17] | ms | |
| $t_{DSCLK}$ | Data Out delay from falling edge of SCLK | – | – | 50 | ns | |
| $t_{PRGH}$ | Total flash block program time ($t_{ERASEB}$ + $t_{WRITE}$), hot | – | – | 100[17] | ms | $T_J \geq 0$ °C |
| $t_{PRGC}$ | Total flash block program time ($t_{ERASEB}$ + $t_{WRITE}$), cold | – | – | 200[17] | ms | $T_J < 0$ °C |

**Note**
17. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor, and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.

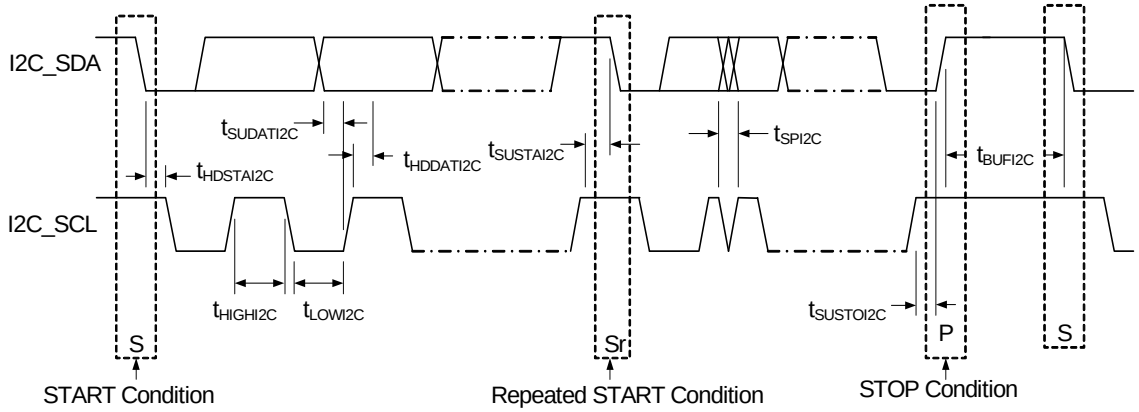
*AC I²C Specifications*

Table 21 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ $T_A$ ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

**Table 21. AC Characteristics of the I²C SDA and SCL Pins**

| Symbol | Description | Standard Mode | | Fast Mode | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $F_{SCLI2C}$ | SCL clock frequency | 0 | 100[18] | 0 | 400[18] | kHz | |
| $t_{HDSTAI2C}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | µs | |
| $t_{LOWI2C}$ | LOW period of the SCL clock | 4.7 | – | 1.3 | – | µs | |
| $t_{HIGHI2C}$ | HIGH period of the SCL clock | 4.0 | – | 0.6 | – | µs | |
| $t_{SUSTAI2C}$ | Setup time for a repeated START condition | 4.7 | – | 0.6 | – | µs | |
| $t_{HDDATI2C}$ | Data hold time | 0 | – | 0 | – | µs | |
| $t_{SUDATI2C}$ | Data setup time | 250 | – | 100[19] | – | ns | |
| $t_{SUSTOI2C}$ | Setup time for STOP condition | 4.0 | – | 0.6 | – | µs | |
| $t_{BUFI2C}$ | Bus free time between a STOP and START condition | 4.7 | – | 1.3 | – | µs | |
| $t_{SPI2C}$ | Pulse width of spikes are suppressed by the input filter. | – | – | 0 | 50 | ns | |

**Figure 8. Definition for Timing for Fast/Standard Mode on the I²C Bus**




**Notes**

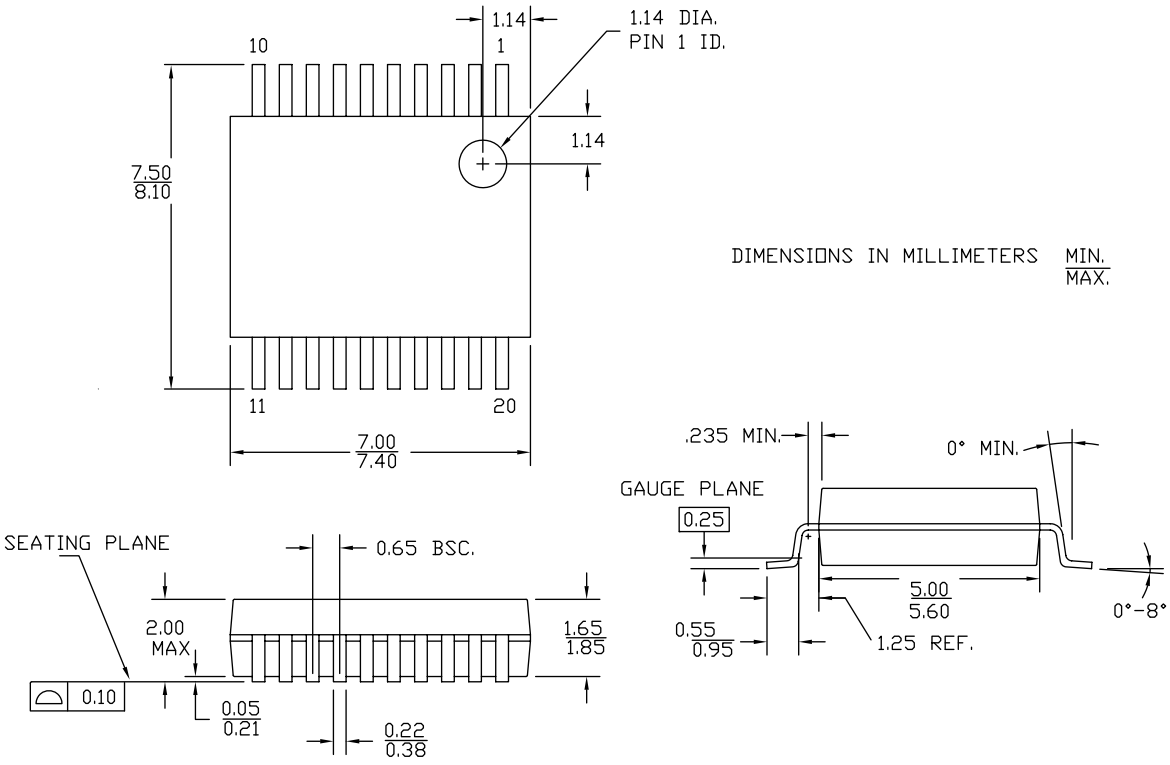
18. $F_{SCLI2C}$ is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 24 MHz, nominal. If SysClk is at a lower frequency, then the $F_{SCLI2C}$ specification adjusts accordingly
19. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $t_{SUDATI2C} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

## Packaging Information

This section illustrates the packaging specifications for the automotive CY8C21x34 PSoC device, along with the thermal impedances for each package.

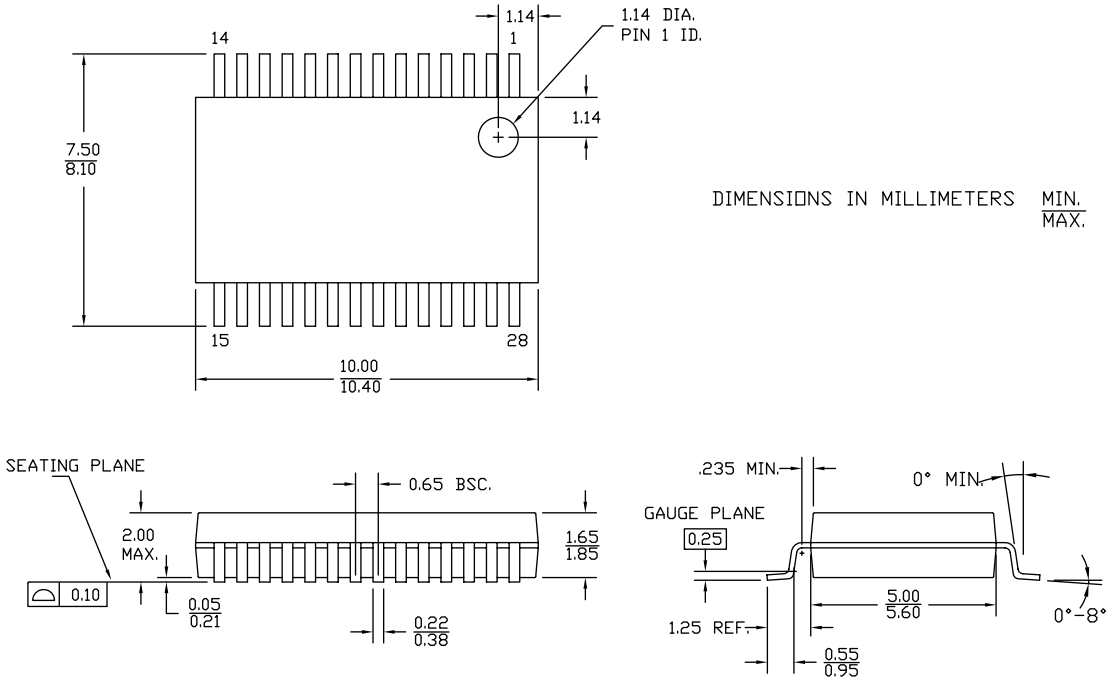
**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

**Figure 9. 20-Pin SSOP (210 Mils)**




51-85077 *F

**Figure 10. 28-Pin SSOP (210 Mils)**




51-85079 *F

## Thermal Impedances

**Table 22. Thermal Impedances per Package**

| Package | Typical $\theta_{JA}$ [20] | Typical $\theta_{JC}$ |
|---|---|---|
| 20-pin SSOP | 117 °C/W | 41 °C/W |
| 28-pin SSOP | 96 °C/W | 39 °C/W |

## Solder Reflow Specifications

Table 23 shows the solder reflow temperature limits that must not be exceeded.

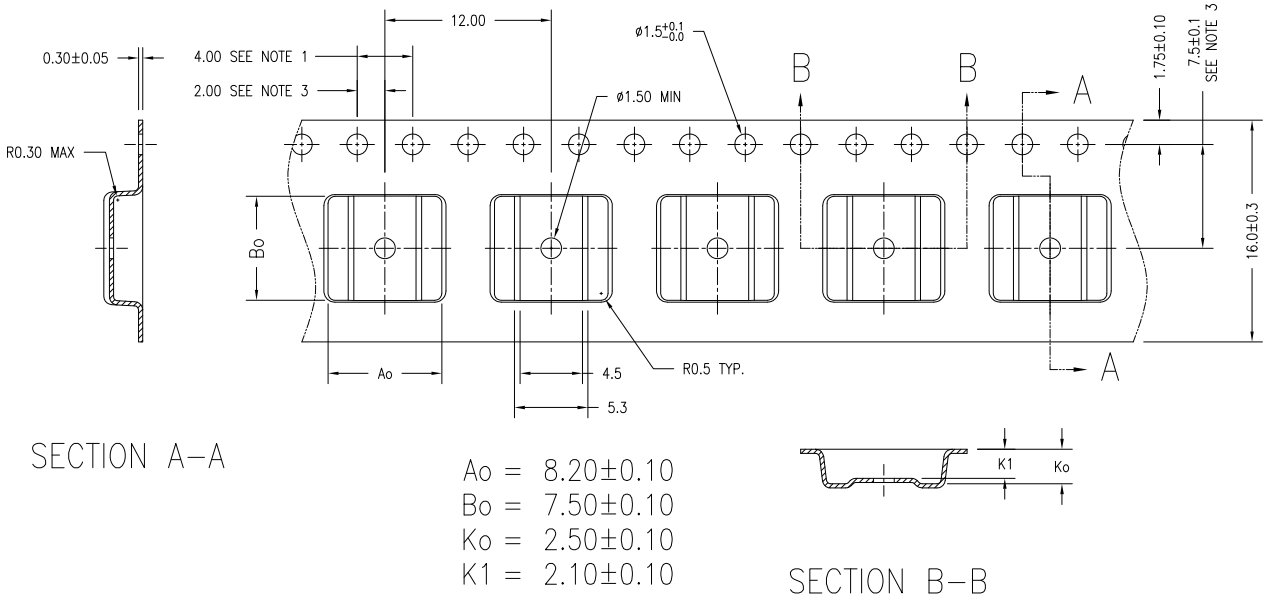
**Table 23. Solder Reflow Specifications**

| Package | Maximum Peak Temperature ($T_C$) | Maximum Time above $T_C$ – 5 °C |
|---|---|---|
| 20-pin SSOP | 260 °C | 30 seconds |
| 28-pin SSOP | 260 °C | 30 seconds |

**Note**
20. $T_J = T_A + \text{Power} \times \theta_{JA}$

## Tape and Reel Information

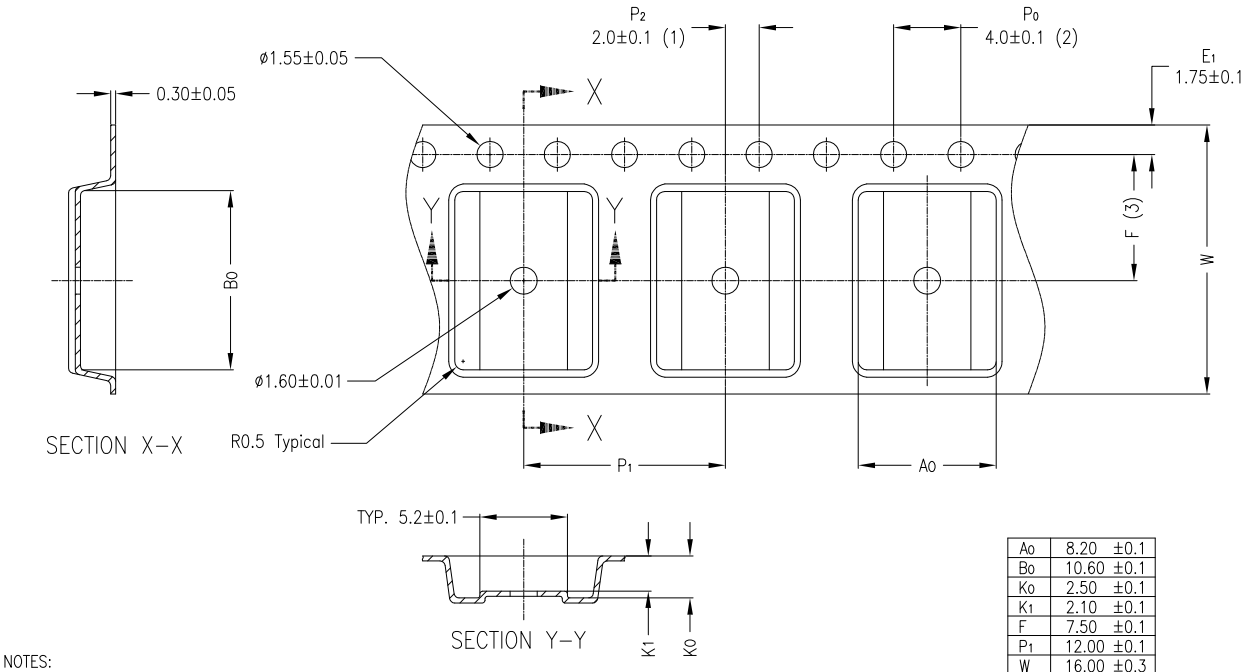
**Figure 11. 20-Pin SSOP Carrier Tape Drawing**




NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

51-51101 *C

**Figure 12. 28-Pin SSOP Carrier Tape Drawing**




| | |
|---|---|
| A0 | 8.20 ±0.1 |
| B0 | 10.60 ±0.1 |
| K0 | 2.50 ±0.1 |
| K1 | 2.10 ±0.1 |
| F | 7.50 ±0.1 |
| P1 | 12.00 ±0.1 |
| W | 16.00 ±0.3 |

NOTES:
( 1 ) Measured from centerline of sprocket hole to centerline of pocket.
( 2 ) Cumulative tolerance of 10 sprocket holes is ± 0.10.
( 3 ) Measured from centerline of sprocket hole to centerline of pocket
4 Material: Conductive Polystyrene
5 Camber not to exceed 1mm in 100mm
6 Supplier P/N: SSOP28–3 CL3 22B3 Lxx W16

51-51100 *D

**Table 24. Tape and Reel Specifications**

| Package | Cover Tape Width (mm) | Hub Size (inches) | Minimum Leading Empty Pockets | Minimum Trailing Empty Pockets | Standard Full Reel Quantity |
|---|---|---|---|---|---|
| 20-pin SSOP | 13.3 | 4 | 42 | 25 | 2000 |
| 28-pin SSOP | 13.3 | 7 | 42 | 25 | 1000 |

## Development Tool Selection

This section presents the development tools available for the automotive CY8C21x34 family.

### Software

*PSoC Designer*

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

*PSoC Programmer*

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube in-circuit emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

### Development Kits

All development kits can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

*CY3215-DK Basic Development Kit*

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the contents of specific memory locations. Advanced emulation features are also supported through PSoC Designer. The kit includes:

- ICE-Cube Unit
- 28-Pin PDIP Emulation Pod for CY8C29466-24PXI
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Samples (two)
- PSoC Designer Software CD
- ISSP Cable
- MiniEval Socket Programming and Evaluation board
- Backward Compatibility Cable (for connecting to legacy Pods)
- Universal 110/220 Power Supply (12 V)
- European Plug Adapter
- USB 2.0 Cable
- Getting Started Guide
- Development Kit Registration form

*CY3280-BK1*

The CY3280-BK1 Universal CapSense Control Kit is designed for easy prototyping and debug of CapSense designs with pre-defined control circuitry and plug-in hardware. The kit comes with a control boards for CY8C20x34 and CY8C21x34 devices as well as a breadboard module and a button(5)/slider module.

### Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

*CY3210-PSoCEval1*

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, an RS-232 port, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

*CY3235-ProxDet*

The CY3235-ProxDet CapSense Proximity Detection Demonstration Kit allows quick and easy demonstration of a PSoC CapSense-enabled device (CY8C21x34) to accurately sense the proximity of a hand or finger along the length of a wire antenna. The kit includes:

- Proximity Detection Demo Board w/Antenna
- I2C to USB Debugging/Communication Bridge
- USB Cable (6 feet)
- Supporting Software CD
- CY3235-ProxDet Quick Start Guide
- 1 CY8C24894 PSoC device on I2C-USB Bridge
- 1 CY8C21434 PSoC device on Proximity Detection Demo Board

*CY3210-21X34 Evaluation Pod (EvalPod)*

PSoC EvalPods are pods that connect to the ICE In-Circuit Emulator (CY3215-DK kit) to allow debugging capability. They can also function as a standalone device without debugging capability. The EvalPod has a 28-pin DIP footprint on the bottom for easy connection to development kits or other hardware. The top of the EvalPod has prototyping headers for easy connection to the device's pins. CY3210-21X34 provides evaluation of the CY8C21x34 PSoC device family.

## Document Conventions

### Units of Measure

The following table lists the units of measure that are used in this document.

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|---|---|---|---|
| °C | degree Celsius | ms | millisecond |
| dB | decibel | mV | millivolt |
| KB | 1024 bytes | nA | nanoampere |
| Kbit | 1024 bits | ns | nanosecond |
| kHz | kilohertz | W | ohm |
| kΩ | kilohm | pA | picoampere |
| MHz | megahertz | pF | picofarad |
| µA | microampere | ps | picosecond |
| µs | microsecond | V | volt |
| µV | microvolt | W | watt |
| mA | milliampere | | |

## Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, ‘01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or ‘0x’ are in decimal format.

## Glossary

| | |
|---|---|
| active high | 1. A logic signal having its asserted state as the logic 1 state.<br>2. A logic signal having the logic 1 state as the higher voltage of the two states. |
| analog blocks | The basic programmable Opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more. |
| analog-to-digital converter (ADC) | A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog converter (DAC) performs the reverse operation. |
| Application programming interface (API) | A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications. |
| asynchronous | A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal. |
| bandgap reference | A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference. |
| bandwidth | 1. The frequency range of a message or information processing system measured in hertz.<br>2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum. |
| bias | 1. A systematic deviation of a value from a reference value.<br>2. The amount by which the average of a set of values departs from a reference value.<br>3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device. |

## Glossary (continued)

| | |
|---|---|
| modulator | A device that imposes a signal on a carrier. |
| noise | 1. A disturbance that affects a signal and that may distort the information carried by the signal.<br>2. The random variations of one or more characteristics of any entity such as voltage, current, or data. |
| oscillator | A circuit that may be crystal controlled and is used to generate a clock frequency. |
| parity | A technique for testing transmitted data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity). |
| phase-locked loop (PLL) | An electronic circuit that controls an *oscillator* so that it maintains a constant phase angle relative to a reference signal. |
| pinouts | The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names. |
| port | A group of pins, usually eight. |
| power-on reset (POR) | A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset. |
| PSoC® | Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress. |
| PSoC Designer™ | The software for Cypress' Programmable System-on-Chip technology. |
| pulse width modulator (PWM) | An output in the form of duty cycle which varies as a function of the applied value. |
| RAM | An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in. |
| register | A storage device with a specific capacity, such as a bit or byte. |
| reset | A means of bringing a system back to a known state. See hardware reset and software reset. |
| ROM | An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in. |
| serial | 1. Pertaining to a process in which all events occur one after the other.<br>2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel. |
| settling time | The time it takes for an output signal or value to stabilize after the input has changed from one value to another. |
| shift register | A memory storage device that sequentially shifts a word either left or right to output a stream of serial data. |
| slave device | A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device. |

## Document History Page (continued)

| Document Title: CY8C21334/CY8C21534, Automotive – Extended Temperature PSoC® Programmable System-on-Chip™<br>Document Number: 38-12038 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *H | 3118809 | BTK / NJF | 08/11/2011 | Updated $I^2C$ timing diagram to improve clarity.<br>Updated wording, formatting, and notes of the AC Digital Block Specifications table to improve clarify.<br>Added $V_{DDP}$, $V_{DDLV}$, and $V_{DDHV}$ electrical specifications to give more information for programming the device.<br>Updated solder reflow temperature specifications to give more clarity.<br>Updated the jitter specifications.<br>Updated PSoC Device Characteristics table.<br>Updated the $F_{32KU}$ electrical specification.<br>Updated DC POR and LVD Specifications to add specs for all POR and LVD levels.<br>Updated note for $R_{PD}$ electrical specification.<br>Updated note for the $T_{STG}$ electrical specification to add more clarity.<br>Added Tape and Reel Information section.<br>Updated Reference Information Section.<br>Added $F_{IMO6}$ electrical specification and Figure 6 on page 13.<br>Changed $F_{IMO24}$ electrical specification to give it a ±5% frequency accuracy.<br>Updated $F_{CPU1}$, $F_{BLK5}$, $F_{MAX}$, and $F_{GPIO}$ electrical specifications and all AC Digital Block Specifications to support a ±5% accuracy oscillator. |
| *I | 3523799 | SMYU | 02/13/2012 | Updated Tape and Reel Information (51-51100 and 51-51101) |
| *J | 3904247 | JICG | 02/14/2013 | Updated Packaging Information (Updated Tape and Reel Information (spec 51-51101 – Changed revision from *B to *C)). |
| *K | 5166373 | SNPR | 03/08/2016 | Updated Packaging Information:<br>spec 51-85077 – Changed revision from *E to *F.<br>spec 51-85079 – Changed revision from *E to *F.<br>Updated Tape and Reel Information:<br>spec 51-51100 – Changed revision from *C to *D.<br>Updated to new template.<br>Completing Sunset Review. |
| *L | 5655080 | SNPR | 03/09/2017 | Updated to new template.<br>Completing Sunset Review. |

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