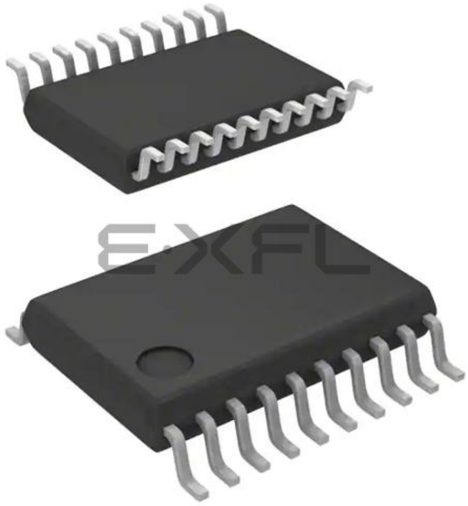


Welcome to E-XFL.COM

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

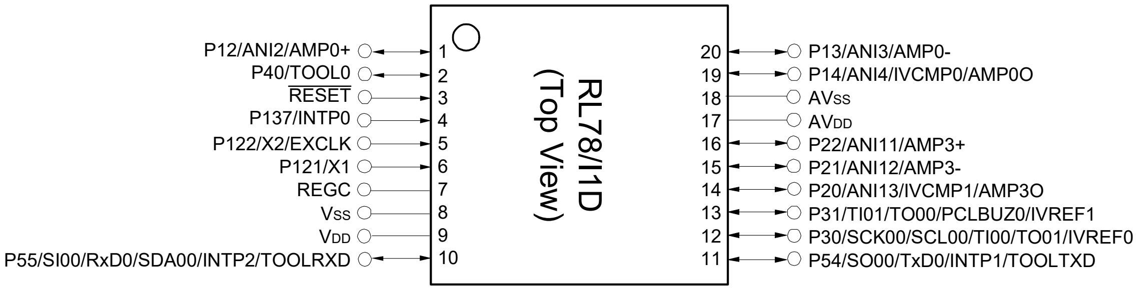
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CSI, I²C, UART/USART |
| Peripherals | LVD, POR, WDT |
| Number of I/O | 11 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 3.6V |
| Data Converters | A/D 6x8/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-LSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 20-LSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1176agsp-30 |

## 1.3 Pin Configuration (Top View)

### 1.3.1 20-pin products

<R> • 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)




**Caution 1. Connect the REGC pin to $V_{SS}$ pin via a capacitor (0.47 to 1 $\mu$F).**

**Caution 2. Make $AV_{SS}$ pin the same potential as $V_{SS}$ pin.**

**Caution 3. Make $AV_{DD}$ pin the same potential as $V_{DD}$ pin.**

**Remark** For pin identification, see **1.4 Pin Identification**.

## 1.4 Pin Identification

| | |
|---|---|
| ANI0 to ANI13, ANI16 to ANI18 | : Analog input |
| $AV_{DD}$ | : Analog power supply |
| $AV_{REFM}$ | : A/D converter reference potential (- side) input |
| $AV_{REFP}$ | : A/D converter reference potential (+ side) input |
| $AV_{SS}$ | : Analog ground |
| EXCLK | : External clock input (main system clock) |
| EXCLKS | : External clock input (subsystem clock) |
| INTP0 to INTP6 | : External interrupt input |
| IVCMP0, IVCMP1 | : Comparator input |
| IVREF0, IVREF1 | : Comparator reference input |
| KR0 to KR3 | : Key return |
| P00 to P04 | : Port 0 |
| P10 to P17 | : Port 1 |
| P20 to P25 | : Port 2 |
| P30 to P33 | : Port 3 |
| P40 | : Port 4 |
| P50 to P57 | : Port 5 |
| P60 to P63 | : Port 6 |
| P121 to P124 | : Port 12 |
| P130, P137 | : Port 13 |

| | |
|---|---|
| PCLBUZ0, PCLBUZ1 | : Programmable clock output/buzzer output |
| REGC | : Regulator capacitance |
| $\overline{\text{RESET}}$ | : Reset |
| RTC1HZ | : Real-time clock correction clock (1 Hz) output |
| RxD0 | : Receive data |
| SCK00, SCK01 | : Serial clock input/output |
| SCL00, SCL01 | : Serial clock input/output |
| SDA00, SDA01 | : Serial data input/output |
| SI00, SI01 | : Serial data input |
| SO00, SO01 | : Serial data output |
| $\overline{\text{SSI00}}$ | : Serial interface chip select input |
| TI00 to TI03 | : Timer input |
| TO00 to TO03 | : Timer output |
| TOOL0 | : Data input/output for tool |
| TOOLRXD, TOOLTXD | : Data input/output for external device |
| TxD0 | : Transmit data |
| VCOUT0, VCOUT1 | : Comparator output |
| AMP0+, AMP1+, AMP2+, AMP3+ | : Operational amplifier (+side) input |
| AMP0-, AMP1-, AMP2-, AMP3- | : Operational amplifier (-side) input |
| AMP0O, AMP1O, AMP2O, AMP3O | : Operational amplifier output |
| $V_{DD}$ | : Power supply |
| $V_{SS}$ | : Ground |
| X1, X2 | : Crystal oscillator (main system clock) |
| XT1, XT2 | : Crystal oscillator (subsystem clock) |

## 2.3 DC Characteristics

### 2.3.1 Pin characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V)**
**($T_A$ = +85 to +105°C, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V)** **(1/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high Note 1 | $I_{OH1}$ | Per pin for P00 to P04, P30 to P33, P40, P50 to P57, P130 | $T_A$ = -40 to +85°C | | | -10.0 Note 2 | mA |
| | | | $T_A$ = +85 to +105°C | | | -3.0 Note 2 | mA |
| | | Total of P00 to P04, P40, P130 (When duty ≤ 70% Note 3) | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | -10.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | -5.0 | mA |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | -2.5 | mA |
| | | Total of P30 to P33, P50 to P57 (When duty ≤ 70% Note 3) | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | | -19.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | -10.0 | mA |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | -5.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | | | | -29.0 | mA |
| | $I_{OH2}$ | Per pin for P10 to P17, P20 to P25 | | | | -0.1 Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | | -1.4 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from the $V_{DD}$ pin to an output pin.
**Note 2.** Do not exceed the total current value.
**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)
  <Example> Where n = 80% and $I_{OH}$ = -10.0 mA
  Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

**Caution P30 and P51 to P56 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

<R> **Note 1.** Total current flowing into $V_{DD}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$ or $V_{SS}$. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, operational amplifier, comparator, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

**Note 2.** When the HALT instruction is executed in the flash memory.

**Note 3.** When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.

**Note 4.** When the high-speed system clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.

**Note 5.** When the high-speed system clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and high-speed on-chip oscillator clock are stopped. When RTCLPC = 1 and ultra-low-power consumption oscillation is set (AMPHS1, AMPHS0) = (1, 0). The values include the current flowing into the real-time clock. However, the values do not include the current flowing into the 12-bit interval timer and watchdog timer.

**Note 6.** When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, high-speed system clock, and sub clock are stopped.

**Note 7.** When the high-speed system clock, high-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{IH}$: High-speed on-chip oscillator clock frequency (24 MHz max.)

**Remark 3.** $f_{IM}$: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

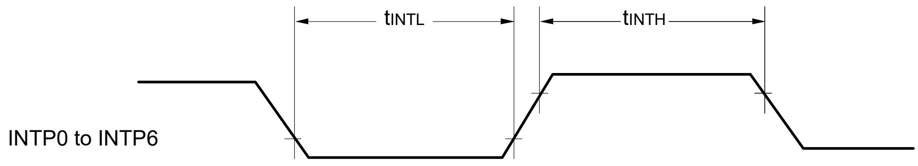
**Remark 4.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**Remark 5.** $f_{SX}$: Sub clock frequency (XT1 clock oscillation frequency)

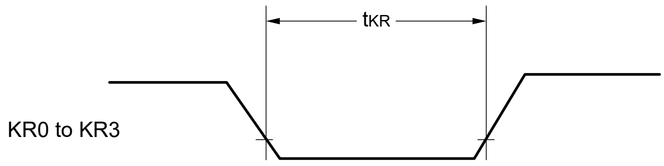
**Remark 6.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency or low-speed on-chip oscillator clock frequency)

**Remark 7.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

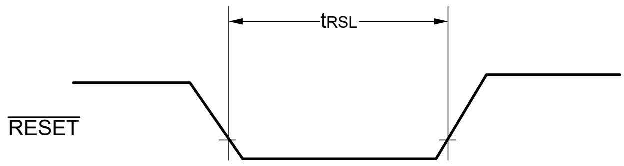
Interrupt Request Input Timing



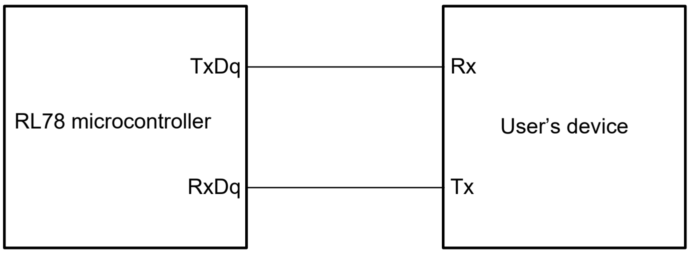

Key Interrupt Input Timing



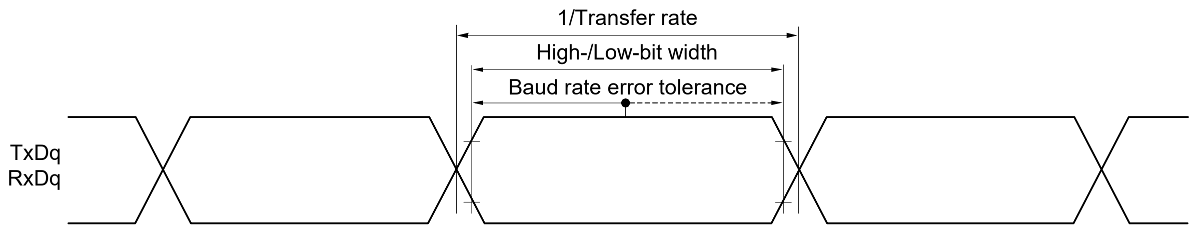

$\overline{\text{RESET}}$ Input Timing



**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remark 1.** q: UART number (q = 0), g: PIM and POM number (g = 5)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

### (3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode MIN. | HS (high-speed main) Mode MAX. | LS (low-speed main) Mode MIN. | LS (low-speed main) Mode MAX. | LP (Low-power main) mode MIN. | LP (Low-power main) mode MAX. | LV (low-voltage main) Mode MIN. | LV (low-voltage main) Mode MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ $f_{CLK}$/4 | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | 167 | | 500 | | 4000 | | 1000 | | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | 250 | | | | | | | | |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | — | | | | | | | | |
| | | | 1.7 V ≤ $V_{DD}$ ≤ 3.6 V | — | | — | | — | | | | |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | — | | — | | — | | | | |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | $t_{KCY1}$/2 - 18 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | $t_{KCY1}$/2 - 38 | | | | | | | | |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | | | | | | | |
| | | 1.7 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | $t_{KCY1}$/2 - 100 | | |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | | | |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 58 | | 110 | | 110 | | 110 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 75 | | | | | | | | |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | | | | | | | |
| | | 1.7 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | 220 | | |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | | | |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 19 | | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | | | | | | | |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | | | |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 30 pF Note 4 | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 33.4 | | 33.4 | | 33.4 | | 33.4 | ns |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | | | | | | |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | | |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

### (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 5 | $t_{KCY2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | $f_{MCK}$ > 16 MHz | 8/$f_{MCK}$ | | — | — | — | — | — | — | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 6/$f_{MCK}$ and 500 | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | |
| | | 1.7 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | | | |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | | | |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | $t_{KCY2}$/2 - 8 | | $t_{KCY2}$/2 - 8 | | $t_{KCY2}$/2 - 8 | | $t_{KCY2}$/2 - 8 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | $t_{KCY2}$/2 - 18 | | $t_{KCY2}$/2 - 18 | | $t_{KCY2}$/2 - 18 | | $t_{KCY2}$/2 - 18 | | |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | | | | | | | |
| | | 1.7 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | $t_{KCY2}$/2 - 66 | | |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | | | |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 1/$f_{MCK}$ + 30 | | | | | | | | |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | | | | | | | |
| | | 1.7 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | 1/$f_{MCK}$ + 40 | | |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | | | |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | | | | | | | |
| | | 1.7 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | 1/$f_{MCK}$ + 250 | | |
| | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | | | |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note 4 | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 2/$f_{MCK}$ + 44 | | 2/$f_{MCK}$ + 110 | | 2/$f_{MCK}$ + 110 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 3.6 V | | 2/$f_{MCK}$ + 75 | | | | | | | |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | | | | | | |
| | | | 1.7 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | 2/$f_{MCK}$ + 220 | |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 3.6 V | | — | | — | | — | | | |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SOp output lines.

**Note 5.** The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

**Caution** **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 01))

**Note 1.** The value must also be equal to or less than $f_{MCK}/4$.

**Note 2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** **Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

**(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output)**

**($T_A$ = +85 to 105°C, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ $f_{CLK}$/4 | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 1000 | | ns |
| | | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 2300 | | ns |
| SCKp high-level width | $t_{KH1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 340 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 916 | | ns |
| SCKp low-level width | $t_{KL1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 36 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 100 | | ns |

**Caution** **Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

### (8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = +85 to 105°C, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V)** **(2/2)**

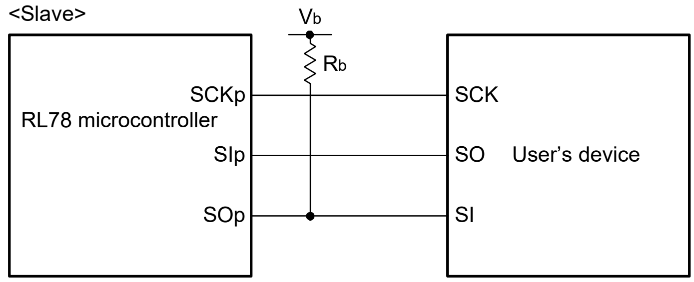
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 354 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 958 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 390 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 966 | ns |
| SIp setup time (to SCKp↓) Note 2 | $t_{SIK1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 88 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 220 | | ns |
| SIp hold time (from SCKp↓) Note 2 | $t_{KSI1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↑ to SOp output Note 2 | $t_{KSO1}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 50 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 3, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 50 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
**Note 3.** Use it with $V_{DD}$ ≥ $V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**CSI mode connection diagram (during communication at different potential)**




**Remark 1.** $R_b$[Ω]: Communication line (SOp) pull-up resistance, $C_b$[F]: Communication line (SOp) load capacitance,
$V_b$[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 01))

### (10) Communication at different potential (1.8 V, 2.5 V) (simplified $I^2C$ mode)

**($T_A$ = -40 to 85°C, 1.8 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | | 250 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | | 300 Note 1 | | 250 Note 1 | | 300 Note 1 | kHz |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 300 Note 1 | | 300 Note 1 | | 250 Note 1 | | 300 Note 1 | kHz |
| Hold time when SCLr = "L" | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1150 | | 1550 | | 1550 | | 1550 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1550 | | 1550 | | 1550 | | 1550 | | ns |
| Hold time when SCLr = "H" | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 200 | | 610 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 600 | | 610 | | 610 | | 610 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 610 | | 610 | | 610 | | 610 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 135 Note 3 | | $1/f_{MCK}$ + 190 Note 2 | | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | $1/f_{MCK}$ + 190 Note 3 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | 0 | 405 | ns |

**Note 1.** The value must also be equal to or less than $f_{MCK}/4$.
**Note 2.** Use it with $V_{DD}$ ≥ $V_b$.
**Note 3.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

### (10) Communication at different potential (1.8 V, 2.5 V) (simplified I²C mode)

**($T_A$ = +85 to 105°C, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 100 Note 1 | kHz |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = "L" | $t_{LOW}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 4600 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 4650 | | ns |
| Hold time when SCLr = "H" | $t_{HIGH}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 500 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 2400 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1830 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 340 Note 3 | | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 760 Note 3 | | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1/$f_{MCK}$ + 570 Note 3 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 1420 | ns |
| | | 2.4 V ≤ $V_{DD}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 1215 | ns |

**Note 1.** The value must also be equal to or less than $f_{MCK}$/4.

**Note 2.** Use it with $V_{DD}$ ≥ $V_b$.

**Note 3.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** **Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**(1) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), conversion target: ANI2 to ANI13**

**($T_A$ = -40 to +85°C, 1.6 V ≤ AVREFP ≤ AVDD = VDD ≤ 3.6 V, VSS = 0 V, AVSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | 8 | | 12 | bit |
| | | | 1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | 8 | | 10 Note 1 | |
| | | | 1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | 8 Note 2 | | |
| Overall error Note 3 | AINL | 12-bit resolution | 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±6.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±5.0 | |
| | | 8-bit resolution | 1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±2.5 | |
| Conversion time | tCONV | ADTYP = 0, 12-bit resolution | 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | 3.375 | | | μs |
| | | ADTYP = 0, 10-bit resolution Note 1 | 1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | 6.75 | | | |
| | | ADTYP = 0, 8-bit resolution Note 2 | 1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | 13.5 | | | |
| | | ADTYP = 1, 8-bit resolution | 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | 2.5625 | | | |
| | | | 1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | 5.125 | | | |
| | | | 1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | 10.25 | | | |
| Zero-scale error Note 3 | EZS | 12-bit resolution | 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±4.5 | LSB |
| | | 10-bit resolution | 1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±4.5 | |
| | | 8-bit resolution | 1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±2.0 | |
| Full-scale error Note 3 | EFS | 12-bit resolution | 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±4.5 | LSB |
| | | 10-bit resolution | 1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±4.5 | |
| | | 8-bit resolution | 1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±2.0 | |
| Integral linearity error Note 3 | ILE | 12-bit resolution | 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±2.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±1.5 | |
| | | 8-bit resolution | 1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±1.0 | |
| Differential linearity error Note 3 | DLE | 12-bit resolution | 2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±1.5 | LSB |
| | | 10-bit resolution | 1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±1.5 | |
| | | 8-bit resolution | 1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V | | | ±1.0 | |
| Analog input voltage | VAIN | | | 0 | | AVREFP | V |

**Note 1.** Cannot be used for lower 2 bit of ADCR register
**Note 2.** Cannot be used for lower 4 bit of ADCR register
**Note 3.** Excludes quantization error (±1/2 LSB).

**Caution Always use AVDD pin with the same potential as the VDD pin.**

**(3) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), conversion target: ANI16 to ANI18, internal reference voltage, temperature sensor output voltage**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 3.6 V, 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 12 | bit |
| | | | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 10 Note 1 | |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 Note 2 | | | |
| Overall error Note 3 | AINL | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±7.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.5 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.0 | |
| Conversion time | $t_{CONV}$ | ADTYP = 0, 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 4.125 | | | μs |
| | | ADTYP = 0, 10-bit resolution Note 1 | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 9.5 | | | |
| | | ADTYP = 0, 8-bit resolution Note 2 | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 57.5 | | | |
| | | ADTYP = 1, 8-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 3.3125 | | | |
| | | | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 7.875 | | | |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 54.25 | | | |
| Zero-scale error Note 3 | $E_{ZS}$ | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.5 | |
| Full-scale error Note 3 | $E_{FS}$ | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.5 | |
| Integral linearity error Note 3 | ILE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.5 | |
| Differential linearity error Note 3 | DLE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | LSB |
| | | 10-bit resolution | 1.8 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | |
| | | 8-bit resolution | 1.6 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.5 | |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage (1.8 V ≤ $V_{DD}$ ≤ 3.6 V) | | $V_{BGR}$ Note 4 | | | |
| | | Temperature sensor output voltage (1.8 V ≤ $V_{DD}$ ≤ 3.6 V) | | $V_{TMP25}$ Note 4 | | | |

**Note 1.** Cannot be used for lower 2 bits of ADCR register

**Note 2.** Cannot be used for lower 4 bits of ADCR register

**Note 3.** Excludes quantization error (±1/2 LSB).

**Note 4.** Refer to **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

**(5) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVSS (ADREFM = 0), conversion target: ANI0 to ANI13, ANI16 to ANI18**

**($T_A$ = -40 to +85°C, 1.8 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = internal reference voltage, Reference voltage (-) = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 16 | | | μs |
| Zero-scale error Note | EZS | 8-bit resolution | | | ±4.0 | LSB |
| Integral linearity error Note | ILE | 8-bit resolution | | | ±2.0 | LSB |
| Differential linearity error Note | DLE | 8-bit resolution | | | ±2.5 | LSB |
| Analog input voltage | $V_{AIN}$ | | 0 | | $V_{BGR}$ | V |

**Note** Excludes quantization error (±1/2 LSB).

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

**(6) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), conversion target: ANI2 to ANI13**

**($T_A$ = +85 to +105°C, 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 12 | bit |
| Overall error Note | AINL | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±6.0 | LSB |
| Conversion time | $t_{CONV}$ | ADTYP = 0, 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 3.375 | | | μs |
| Zero-scale error Note | EZS | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±4.5 | LSB |
| Full-scale error Note | EFS | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±4.5 | LSB |
| Integral linearity error Note | ILE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | LSB |
| Differential linearity error Note | DLE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±1.5 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $AV_{REFP}$ | V |

**Note** Excludes quantization error (±1/2 LSB).

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

**(7) When reference voltage (+) = AVDD (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = AVSS (ADREFM = 0), conversion target: ANI0 to ANI13**

**($T_A$ = +85 to +105°C, 2.4 V ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = $AV_{DD}$, Reference voltage (-) = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 12 | bit |
| Overall error Note | AINL | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±7.5 | LSB |
| Conversion time | $t_{CONV}$ | ADTYP = 0, 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | 3.375 | | | μs |
| Zero-scale error Note | $E_{ZS}$ | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±6.0 | LSB |
| Full-scale error Note | $E_{FS}$ | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±6.0 | LSB |
| Integral linearity error Note | ILE | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.0 | LSB |
| Differential linearity error Note | DLE | 12-bit resolution | 2.4 V ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $AV_{DD}$ | V |

**Note** Excludes quantization error (±1/2 LSB).

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

**(8) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), conversion target ANI16 to ANI18, internal reference voltage, temperature sensor output voltage**

**($T_A$ = +85 to +105°C, 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = 0 V, $AV_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | $R_{ES}$ | | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 8 | | 12 | bit |
| Overall error Note 1 | AINL | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | ADTYP = 0, 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | 4.125 | | | μs |
| Zero-scale error Note 1 | $E_{ZS}$ | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | LSB |
| Full-scale error Note 1 | $E_{FS}$ | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±5.0 | LSB |
| Integral linearity error Note 1 | ILE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±3.0 | LSB |
| Differential linearity error Note 1 | DLE | 12-bit resolution | 2.4 V ≤ $AV_{REFP}$ ≤ $AV_{DD}$ ≤ 3.6 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage (2.4 V ≤ $V_{DD}$ ≤ 3.6 V) | | $V_{BGR}$ Note 2 | | | |
| | | Temperature sensor output voltage (2.4 V ≤ $V_{DD}$ ≤ 3.6 V) | | $V_{TMP25}$ Note 2 | | | |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** Refer to **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

**Caution Always use $AV_{DD}$ pin with the same potential as the $V_{DD}$ pin.**

### (2) LVD Detection Voltage of Interrupt & Reset Mode

**($T_A$ = -40 to +85°C, $V_{PDR}$ ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDA0}$ | $V_{POC0}$, $V_{POC1}$, $V_{POC2}$ = 0, 0, 0, falling reset voltage | | 1.60 | 1.63 | 1.66 | V |
| | $V_{LVDA1}$ | LVIS0, LVIS1 = 1, 0 | Rising release reset voltage | 1.74 | 1.77 | 1.81 | V |
| | | | Falling interrupt voltage | 1.70 | 1.73 | 1.77 | V |
| | $V_{LVDA2}$ | LVIS0, LVIS1 = 0, 1 | Rising release reset voltage | 1.84 | 1.88 | 1.91 | V |
| | | | Falling interrupt voltage | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDA3}$ | LVIS0, LVIS1 = 0, 0 | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDB0}$ | $V_{POC0}$, $V_{POC1}$, $V_{POC2}$ = 0, 0, 1, falling reset voltage | | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDB1}$ | LVIS0, LVIS1 = 1, 0 | Rising release reset voltage | 1.94 | 1.98 | 2.02 | V |
| | | | Falling interrupt voltage | 1.90 | 1.94 | 1.98 | V |
| | $V_{LVDB2}$ | LVIS0, LVIS1 = 0, 1 | Rising release reset voltage | 2.05 | 2.09 | 2.13 | V |
| | | | Falling interrupt voltage | 2.00 | 2.04 | 2.08 | V |
| | $V_{LVDB3}$ | LVIS0, LVIS1 = 0, 0 | Rising release reset voltage | 3.07 | 3.13 | 3.19 | V |
| | | | Falling interrupt voltage | 3.00 | 3.06 | 3.12 | V |
| | $V_{LVDC0}$ | $V_{POC0}$, $V_{POC1}$, $V_{POC2}$ = 0, 1, 0, falling reset voltage | | 2.40 | 2.45 | 2.50 | V |
| | $V_{LVDC1}$ | LVIS0, LVIS1 = 1, 0 | Rising release reset voltage | 2.56 | 2.61 | 2.66 | V |
| | | | Falling interrupt voltage | 2.50 | 2.55 | 2.60 | V |
| | $V_{LVDC2}$ | LVIS0, LVIS1 = 0, 1 | Rising release reset voltage | 2.66 | 2.71 | 2.76 | V |
| | | | Falling interrupt voltage | 2.60 | 2.65 | 2.70 | V |
| | $V_{LVDD0}$ | $V_{POC0}$, $V_{POC1}$, $V_{POC2}$ = 0, 1, 1, falling reset voltage | | 2.70 | 2.75 | 2.81 | V |
| | $V_{LVDD1}$ | LVIS0, LVIS1 = 1, 0 | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDD2}$ | LVIS0, LVIS1 = 0, 1 | Rising release reset voltage | 2.96 | 3.02 | 3.08 | V |
| | | | Falling interrupt voltage | 2.90 | 2.96 | 3.02 | V |

**($T_A$ = +85 to +105°C, $V_{PDR}$ ≤ $AV_{DD}$ = $V_{DD}$ ≤ 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDD0}$ | $V_{POC0}$, $V_{POC1}$, $V_{POC2}$ = 0, 1, 1, falling reset voltage | | 2.64 | 2.75 | 2.86 | V |
| | $V_{LVDD1}$ | LVIS0, LVIS1 = 1, 0 | Rising release reset voltage | 2.81 | 2.92 | 3.03 | V |
| | | | Falling interrupt voltage | 2.75 | 2.86 | 2.97 | V |
| | $V_{LVDD2}$ | LVIS0, LVIS1 = 0, 1 | Rising release reset voltage | 2.90 | 3.02 | 3.14 | V |
| | | | Falling interrupt voltage | 2.85 | 2.96 | 3.07 | V |

## 2.6.7 Power supply voltage rising slope characteristics

**($T_A$ = -40 to +105°C, $V_{SS}$ = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 2.4 AC Characteristics.**