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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f117aagsp-50

1.4 Pin Identification

ANI0 to ANI13, ANI16 to ANI18 : Analog input
AV_{DD} : Analog power supply
AV_{REFM} : A/D converter reference potential (- side) input
AV_{REFP} : A/D converter reference potential (+ side) input
AV_{SS} : Analog ground
EXCLK : External clock input (main system clock)
EXCLKS : External clock input (subsystem clock)
INTP0 to INTP6 : External interrupt input
IVCMP0, IVCMP1 : Comparator input
IVREF0, IVREF1 : Comparator reference input
KR0 to KR3 : Key return
P00 to P04 : Port 0
P10 to P17 : Port 1
P20 to P25 : Port 2
P30 to P33 : Port 3
P40 : Port 4
P50 to P57 : Port 5
P60 to P63 : Port 6
P121 to P124 : Port 12
P130, P137 : Port 13
PCLBUZ0, PCLBUZ1 : Programmable clock output/buzzer output
REGC : Regulator capacitance
$\overline{\text{RESET}}$: Reset
RTC1HZ : Real-time clock correction clock (1 Hz) output
RxD0 : Receive data
SCK00, SCK01 : Serial clock input/output
SCL00, SCL01 : Serial clock input/output
SDA00, SDA01 : Serial data input/output
SI00, SI01 : Serial data input
SO00, SO01 : Serial data output
$\overline{\text{SSI00}}$: Serial interface chip select input
TI00 to TI03 : Timer input
TO00 to TO03 : Timer output
TOOL0 : Data input/output for tool
TOOLRXD, TOOLTXD : Data input/output for external device
TxD0 : Transmit data
VCOUT0, VCOUT1 : Comparator output
AMP0+, AMP1+, AMP2+, AMP3+ : Operational amplifier (+side) input
AMP0-, AMP1-, AMP2-, AMP3- : Operational amplifier (-side) input
AMP0O, AMP1O, AMP2O, AMP3O : Operational amplifier output
V_{DD} : Power supply
V_{SS} : Ground
X1, X2 : Crystal oscillator (main system clock)
XT1, XT2 : Crystal oscillator (subsystem clock)

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

(T_A = +85 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) **(3/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P04, P30 to P33, P40, P50 to P57, P130	Normal input buffer	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P30, P32, P33, P51, P52, P54 to P57	TTL input buffer 3.3 V ≤ V_{DD} ≤ 3.6 V	2.0		V_{DD}	V
			TTL input buffer 1.6 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
	V_{IH3}	P10 to P17, P20 to P25		0.7 AV_{DD}		AV_{DD}	V
	V_{IH4}	P60 to P63		0.7 V_{DD}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P04, P30 to P33, P40, P50 to P57, P130	Normal input buffer	0		0.2 V_{DD}	V
	V_{IL2}	P30, P32, P33, P51, P52, P54 to P57	TTL input buffer 3.3 V ≤ V_{DD} ≤ 3.6 V	0		0.5	V
			TTL input buffer 1.6 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P10 to P17, P20 to P25		0		0.3 AV_{DD}	V
	V_{IL4}	P60 to P63		0		0.3 V_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V

Caution The maximum value of V_{IH} of pins P30 and P51 to P56 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

(T_A = +85 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) **(1/4)**

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 24 MHz Note 3, T_A = -40 to +105°C	Basic operation	V_{DD} = 3.0 V			1.4		mA
			HS (high-speed main) mode	f_{IH} = 24 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			3.2	6.3	mA
				f_{IH} = 24 MHz Note 3, T_A = +85 to +105°C	Normal operation	V_{DD} = 3.0 V				6.7	
				f_{IH} = 16 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			2.4	4.6	
				f_{IH} = 16 MHz Note 3, T_A = +85 to +105°C	Normal operation	V_{DD} = 3.0 V				4.9	
			LS (low-speed main) mode (MCSEL = 0)	f_{IH} = 8 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			1.1	2.0	mA
						V_{DD} = 2.0 V			1.1	2.0	
			LS (low-speed main) mode (MCSEL = 1)	f_{IH} = 4 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			0.72	1.30	mA
						V_{DD} = 2.0 V			0.72	1.30	
<R>				f_{IM} = 4 MHz Note 7, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			0.58	1.10	
<R>						V_{DD} = 2.0 V			0.58	1.10	
<R>			LV (low-voltage main) mode	f_{IH} = 3 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			1.2	1.8	mA
						V_{DD} = 2.0 V			1.2	1.8	
			LP (low-power main) mode Note 5 (MCSEL = 1)	f_{IH} = 1 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			290	480	µA
						V_{DD} = 2.0 V			290	480	
				f_{IM} = 1 MHz Note 5, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			124	230	
						V_{DD} = 2.0 V			124	230	
			HS (high-speed main) mode	f_{MX} = 20 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V	Square wave input		2.7	5.3	mA
							Resonator connection		2.8	5.5	
				f_{MX} = 20 MHz Note 2, T_A = +85 to +105°C	Normal operation	V_{DD} = 3.0 V	Square wave input			5.7	
							Resonator connection			5.8	
				f_{MX} = 10 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V	Square wave input		1.8	3.1	
							Resonator connection		1.9	3.2	
				f_{MX} = 10 MHz Note 2, T_A = +85 to +105°C	Normal operation	V_{DD} = 3.0 V	Square wave input			3.4	
							Resonator connection			3.5	
			LS (low-speed main) mode (MCSEL = 0)	f_{MX} = 8 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V	Square wave input		0.9	1.9	mA
							Resonator connection		1.0	2.0	
				f_{MX} = 8 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 2.0 V	Square wave input		0.9	1.9	
							Resonator connection		1.0	2.0	
<R>			LS (low-speed main) mode (MCSEL = 1)	f_{MX} = 4 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V	Square wave input		0.6	1.1	mA
							Resonator connection		0.6	1.2	
<R>				f_{MX} = 4 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 2.0 V	Square wave input		0.6	1.1	
							Resonator connection		0.6	1.2	
			LP (low-power main) mode (MCSEL = 1)	f_{MX} = 1 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V	Square wave input		100	190	µA
							Resonator connection		136	250	
				f_{MX} = 1 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 2.0 V	Square wave input		100	190	
							Resonator connection		136	250	

(**Notes** and **Remarks** are listed on the next page.)

<R>

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, operational amplifier, comparator, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. When the HALT instruction is executed in the flash memory.

Note 3. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.

Note 4. When the high-speed system clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.

Note 5. When the high-speed system clock, middle-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and high-speed on-chip oscillator clock are stopped. When RTCLPC = 1 and ultra-low-power consumption oscillation is set (AMPHS1, AMPHS0) = (1, 0). The values include the current flowing into the real-time clock. However, the values do not include the current flowing into the 12-bit interval timer and watchdog timer.

Note 6. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, high-speed system clock, and sub clock are stopped.

Note 7. When the high-speed system clock, high-speed on-chip oscillator clock, low-speed on-chip oscillator clock, and sub clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_{IM}: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 5. f_{SX}: Sub clock frequency (XT1 clock oscillation frequency)

Remark 6. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency or low-speed on-chip oscillator clock frequency)

Remark 7. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Peripheral Functions (Common to all products)

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

(T_A = +85 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
RTC operating current	I_{RTC} Notes 1, 2, 3	f_{SX} = 32.768 kHz			0.02		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 2, 4	f_{SX} = 32.768 kHz			0.04		μA
8-bit interval timer operating current	I_{TMT} Notes 1, 9	f_{SX} = 32.768 kHz f_{MAIN} stopped (per unit)	8-bit counter mode × 2-channel operation		0.12		μA
			16-bit counter mode operation		0.10		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 6, 10	During maximum-speed conversion	AV_{DD} = 3.0 V		420	720	μA
$AV_{REF(+)}$ current	I_{AVREF} Note 11	AV_{REFP} = 3.0 V, ADREFP1 = 0, ADREFP0 = 1			14.0	25.0	μA
Internal reference voltage (1.45 V) current	I_{ADREF} Notes 1, 12				85.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				85.0		μA
Comparator operating current	I_{CMP} Notes 8, 10	AV_{DD} = 3.6 V, Regulator output voltage = 2.1 V	Comparator high-speed mode Window mode		12.5		μA
			Comparator low-speed mode Window mode		3.0		
			Comparator high-speed mode Standard mode		6.5		
			Comparator low-speed mode Standard mode		1.7		
		AV_{DD} = 3.6 V, Regulator output voltage = 1.8 V	Comparator high-speed mode Window mode		8.0		
			Comparator low-speed mode Window mode		2.2		
			Comparator high-speed mode Standard mode		4.0		
			Comparator low-speed mode Standard mode		1.3		
Operational amplifier operating current	I_{AMP} Notes 10, 13	Low-power consumption mode	One operational amplifier unit operates Note 14		2.5	4.0	μA
			Two operational amplifier units operate Note 14		4.5	8.0	
			Three operational amplifier units operate Note 14		6.5	11.0	
			Four operational amplifier units operate Note 14		8.5	14.0	
		High-speed mode	One operational amplifier unit operates Note 14		140	220	
			Two operational amplifier units operate Note 14		280	410	
			Three operational amplifier units operate Note 14		420	600	
			Four operational amplifier units operate Note 14		560	780	
LVD operating current	I_{LVD} Notes 1, 7				0.10		μA

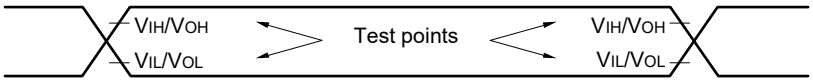
(**Notes** and **Remarks** are listed on the next page.)

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

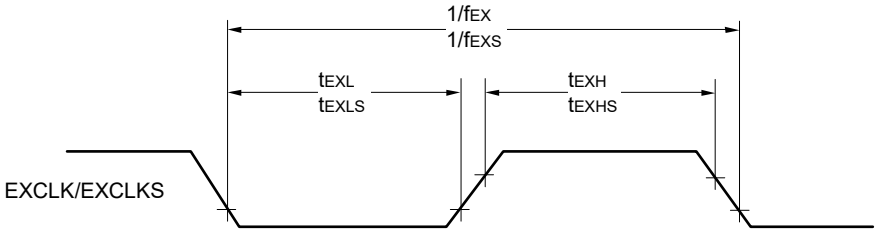
(T_A = +85 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) **(2/2)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
TO00 to TO03 output frequency	f_{TO}	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V			8	MHz
			2.4 V ≤ V_{DD} < 2.7 V			4	
		LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V			4	
		LP (low-power main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V			0.5	
		LV (low-voltage main) mode	1.6 V ≤ V_{DD} ≤ 3.6 V			2	
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V			8	MHz
			2.4 V ≤ V_{DD} < 2.7 V			4	
		LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V			4	
		LP (low-power main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V			1	
		LV (low-voltage main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V			4	
			1.6 V ≤ V_{DD} < 1.8 V			2	
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP6	1.6 V ≤ V_{DD} ≤ 3.6 V	1			µs
Key interrupt input low-level width	t_{KR}	KR0 to KR3	1.8 V ≤ V_{DD} ≤ 3.6 V	250			ns
			1.6 V ≤ V_{DD} < 1.8 V	1			µs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			µs

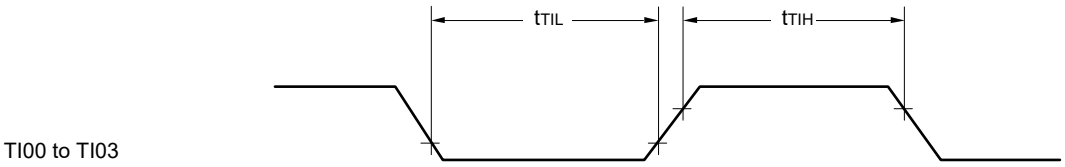
AC Timing Test Points

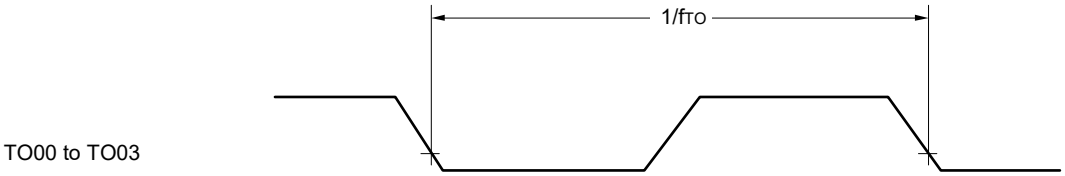


External System Clock Timing



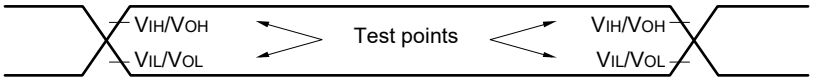
TI/TO Timing





2.5 Peripheral Functions Characteristics

AC Timing Test Points



(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq f_{CLK}/4$	2.7 V ≤ V_{DD} ≤ 3.6 V	167		500		4000		1000		ns
			2.4 V ≤ V_{DD} ≤ 3.6 V	250								
			1.8 V ≤ V_{DD} ≤ 3.6 V	—								
			1.7 V ≤ V_{DD} ≤ 3.6 V	—		—		—				
			1.6 V ≤ V_{DD} ≤ 3.6 V	—		—		—				
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V		t_{KCY1}/2 - 18		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		t_{KCY1}/2 - 38								
		1.8 V ≤ V_{DD} ≤ 3.6 V		—								
		1.7 V ≤ V_{DD} ≤ 3.6 V		—		—		—		t_{KCY1}/2 - 100		
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		—				
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V		58		110		110		110		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		75								
		1.8 V ≤ V_{DD} ≤ 3.6 V		—								
		1.7 V ≤ V_{DD} ≤ 3.6 V		—		—		—		220		
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		—				
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.4 V ≤ V_{DD} ≤ 3.6 V		19		19		19		19		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		—								
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		—				
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4	2.4 V ≤ V_{DD} ≤ 3.6 V		33.4		33.4		33.4		33.4	ns
			1.8 V ≤ V_{DD} ≤ 3.6 V		—							
			1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		—			

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = +85 to +105°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq f_{CLK}/4$	2.7 V ≤ V_{DD} ≤ 3.6 V	250		ns
			2.4 V ≤ V_{DD} ≤ 3.6 V	500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 3.6 V		t_{KCY1}/2 - 36		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		t_{KCY1}/2 - 76		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V		66		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		133		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			38		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 01))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 3.6 V	f_{MCK} > 16 MHz	8/f_{MCK}		—	—	—	—	—	—	ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		
		2.4 V ≤ V_{DD} ≤ 3.6 V		6/f_{MCK} and 500		6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		
		1.8 V ≤ V_{DD} ≤ 3.6 V		—		6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		
		1.7 V ≤ V_{DD} ≤ 3.6 V		—		—		—				
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		—				
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} ≤ 3.6 V		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		
		1.8 V ≤ V_{DD} ≤ 3.6 V		—								
		1.7 V ≤ V_{DD} ≤ 3.6 V		—		—		—		t_{KCY2}/2 - 66		
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		—				
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		2.4 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} + 30								
		1.8 V ≤ V_{DD} ≤ 3.6 V		—								
		1.7 V ≤ V_{DD} ≤ 3.6 V		—		—		—		1/f_{MCK} + 40		
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		—				
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	2.4 V ≤ V_{DD} ≤ 3.6 V		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V		—								
		1.7 V ≤ V_{DD} ≤ 3.6 V		—		—		—		1/f_{MCK} + 250		
		1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		—				
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 3.6 V		2/f_{MCK} + 44		2/f_{MCK} + 110		2/f_{MCK} + 110		2/f_{MCK} + 110	ns
			2.4 V ≤ V_{DD} ≤ 3.6 V		2/f_{MCK} + 75							
			1.8 V ≤ V_{DD} ≤ 3.6 V		—							
			1.7 V ≤ V_{DD} ≤ 3.6 V		—		—		—		2/f_{MCK} + 220	
			1.6 V ≤ V_{DD} ≤ 3.6 V		—		—		—			

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(6) Communication at different potential (1.8 V, 2.5 V) (UART mode) (dedicated baud rate generator output)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Notes 1, 2		reception	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		4.0		1.3		0.1		0.6	Mbps
			1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		4.0		1.3		0.1		0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4,800 bps only.

Note 2. Use it with V_{DD} ≥ Vb.

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 3.6 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 3.6 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)
LP (low-power main) mode: 1 MHz (1.8 V ≤ V_{DD} ≤ 3.6 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 3.6 V)

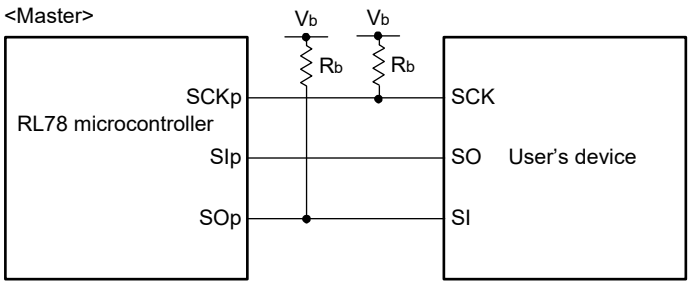
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0), g: PIM and POM number (g = 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

CSI mode connection diagram (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(3) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), conversion target: ANI16 to ANI18, internal reference voltage, temperature sensor output voltage

(TA = -40 to +85°C, 1.6 V ≤ VDD ≤ 3.6 V, 1.6 V ≤ AVREFP ≤ AVDD = VDD ≤ 3.6 V, VSS = 0 V, AVSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	8		12	bit
			1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±7.0	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±3.0	
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	4.125			µs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	3.3125			
			1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	7.875			
			1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	54.25			
Zero-scale error Note 3	EZS	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±5.0	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.5	
Full-scale error Note 3	EFS	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±5.0	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.5	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±3.0	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±1.5	
Analog input voltage	VAIN			0		AVREFP	V
		Internal reference voltage (1.8 V ≤ VDD ≤ 3.6 V)		VBGR Note 4			
		Temperature sensor output voltage (1.8 V ≤ VDD ≤ 3.6 V)		VTMP25 Note 4			

Note 1. Cannot be used for lower 2 bits of ADCR register

Note 2. Cannot be used for lower 4 bits of ADCR register

Note 3. Excludes quantization error (±1/2 LSB).

Note 4. Refer to **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

Caution Always use AVDD pin with the same potential as the VDD pin.

(9) When reference voltage (+) = AVDD (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = AVSS (ADREFM = 0), conversion target: ANI16 to ANI18, internal reference voltage, temperature sensor output voltage

(T_A = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = 0 V, AVSS = 0 V, Reference voltage (+) = AVDD, Reference voltage (-) = AVSS = 0)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AVDD ≤ 3.6 V	8		12	bit
Overall error Note 1	AINL	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±8.5	LSB
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V	4.125			µs
Zero-scale error Note 1	EZS	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±8.0	LSB
Full-scale error Note 1	EFS	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±8.0	LSB
Integral linearity error Note 1	ILE	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±3.5	LSB
Differential linearity error Note 1	DLE	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±2.5	LSB
Analog input voltage	VAIN			0		AVDD	V
		Internal reference voltage (2.4 V ≤ VDD ≤ 3.6 V)		VBGR Note 2			
		Temperature sensor output voltage (2.4 V ≤ VDD ≤ 3.6 V)		VTMP25 Note 2			

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. Refer to **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

Caution Always use AVDD pin with the same potential as the VDD pin.

(10) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVSS (ADREFM = 0), conversion target: ANI0 to ANI13, ANI16 to ANI18

(T_A = +85 to +105°C, 2.4 V ≤ V_{DD}, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = internal reference voltage, Reference voltage (-) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES			8		bit
Conversion time	tCONV	8-bit resolution	16.0			µs
Zero-scale error Note	EZS	8-bit resolution			±4.0	LSB
Integral linearity error Note	ILE	8-bit resolution			±2.0	LSB
Differential linearity error Note	DLE	8-bit resolution			±2.5	LSB
Analog input voltage	VAIN		0		V_{BGR}	V

Note Excludes quantization error (±1/2 LSB).

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

2.6.2 Temperature sensor, internal reference voltage output characteristics

(T_A = -40 to 85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)
(T_A = +85 to 105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tAMP	2.4 V ≤ V_{DD} ≤ 3.6 V	5			µs
		1.8 V ≤ V_{DD} < 2.4 V	10			

2.6.3 Comparator

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

(T_A = +85 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage range	Ivref0	IVREF0 pin		0		V_{DD} - 1.4 Note	V
	Ivref1	IVREF1 pin		1.4 Note		V_{DD}	V
	Ivcmp	IVCMP0, IVCMP1 pins		-0.3		V_{DD} + 0.3	V
Output delay	td	AV_{DD} = 3.0 V Input slew rate > 50 mV/µs	Comparator high-speed mode, standard mode			1.2	µs
			Comparator high-speed mode, window mode			2.0	µs
			Comparator low-speed mode, standard mode		3.0		µs
			Comparator low-speed mode, window mode		4		µs
Operation stabilization wait time	t_{CMP}			100			µs

Note In window mode, make sure that Vref1 - Vref0 ≥ 0.2 V.

2.6.6 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +85°C, $V_{PDR} \leq AV_{DD} = V_{DD} \leq 3.6$ V, $V_{SS} = AV_{SS} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V_{LVD9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V_{LVD10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V_{LVD11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V_{LVD12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V_{LVD13}	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time						300	µs

(T_A = +85 to +105°C, $V_{PDR} \leq AV_{DD} = V_{DD} \leq 3.6$ V, $V_{SS} = AV_{SS} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD2}	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		V_{LVD3}	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		V_{LVD4}	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		V_{LVD5}	Power supply rise time	2.71	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		V_{LVD6}	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		V_{LVD7}	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time						300	µs

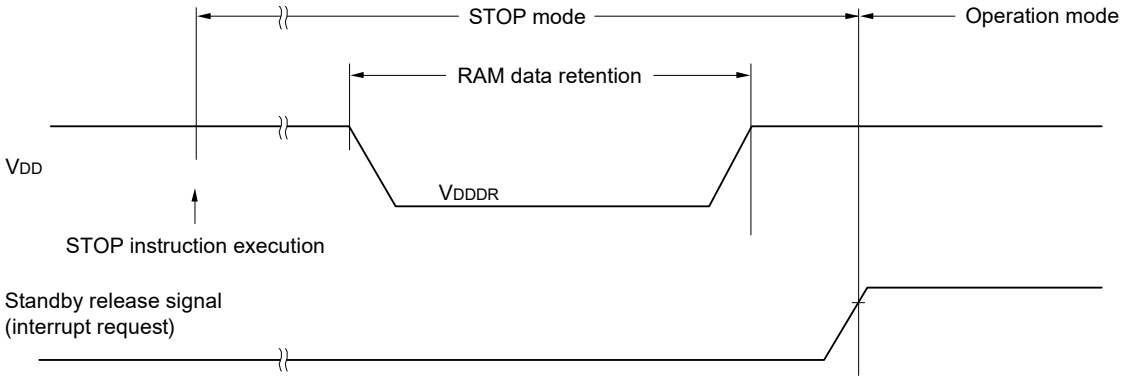
2.7 RAM Data Retention Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

(T_A = +85 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}	T_A = -40 to +85°C	1.46 Note		3.6	V
		T_A = +85 to +105°C	1.44 Note		3.6	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



2.8 Flash Memory Programming Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

(T_A = +85 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}		1		24	MHz
<R> Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years T_A = 85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year T_A = 25°C Note 4		1,000,000		
		Retained for 5 years T_A = 85°C Note 4	100,000			
		Retained for 20 years T_A = 85°C Note 4	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

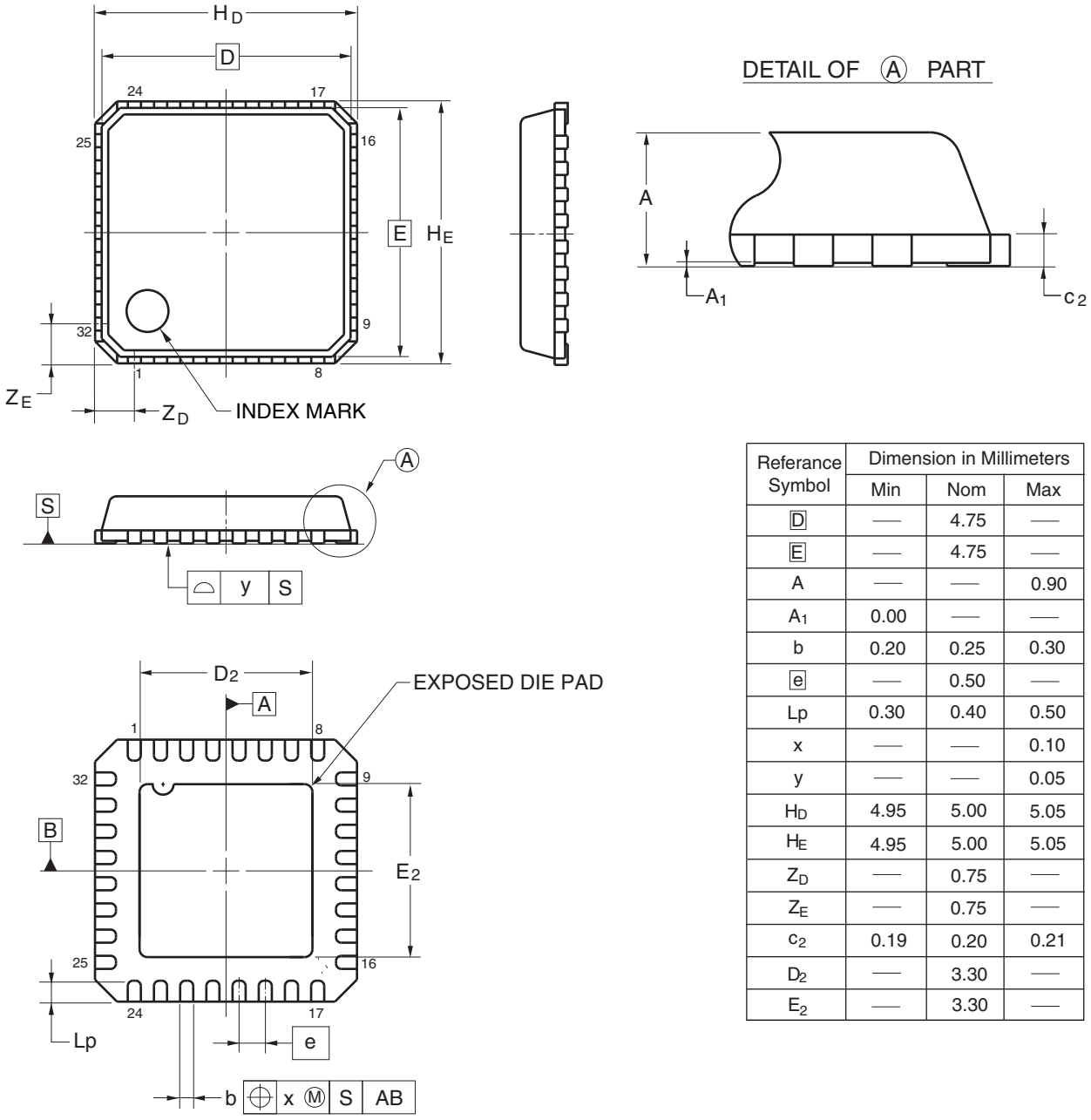
Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

<R> **Note 4.** This temperature is the average value at which data are retained.

3.4 32-pin products

R5F117BCGNA, R5F117BAGNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HVQFN32-5x5-0.50	PVQN0032KE-A	P32K9-50B-BAH	0.058



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.75	—
E	—	4.75	—
A	—	—	0.90
A_1	0.00	—	—
b	0.20	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.10
y	—	—	0.05
H_D	4.95	5.00	5.05
H_E	4.95	5.00	5.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.19	0.20	0.21
D_2	—	3.30	—
E_2	—	3.30	—