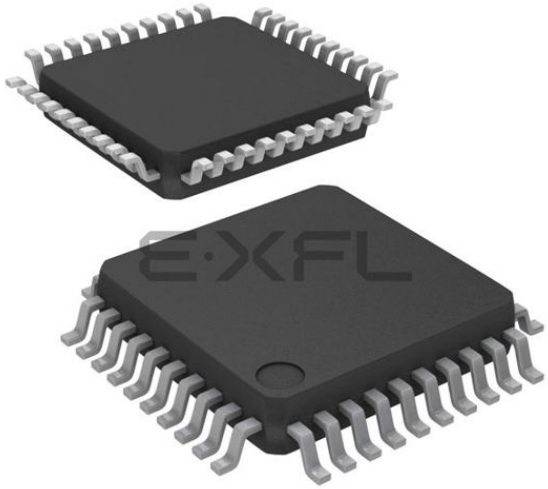
Renesas Electronics America Inc - R5F117BAGFP#50 Datasheet



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What is "Embedded - Microcontrollers"?

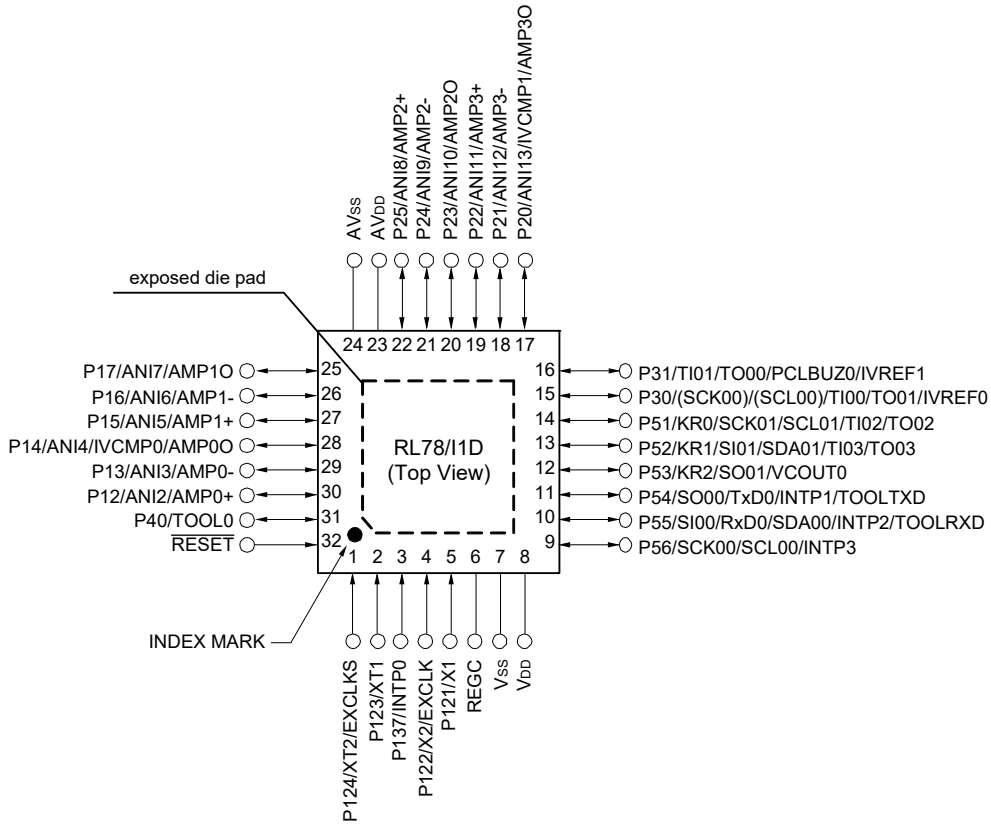
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f117bagfp-50

1.3.4 32-pin products

<R> • 32-pin plastic HVQFN (5 × 5 mm, 0.5 mm pitch)



Caution 1. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).

Caution 2. Make AVSS pin the same potential as VSS pin.

Caution 3. Make AVDD pin the same potential as VDD pin.

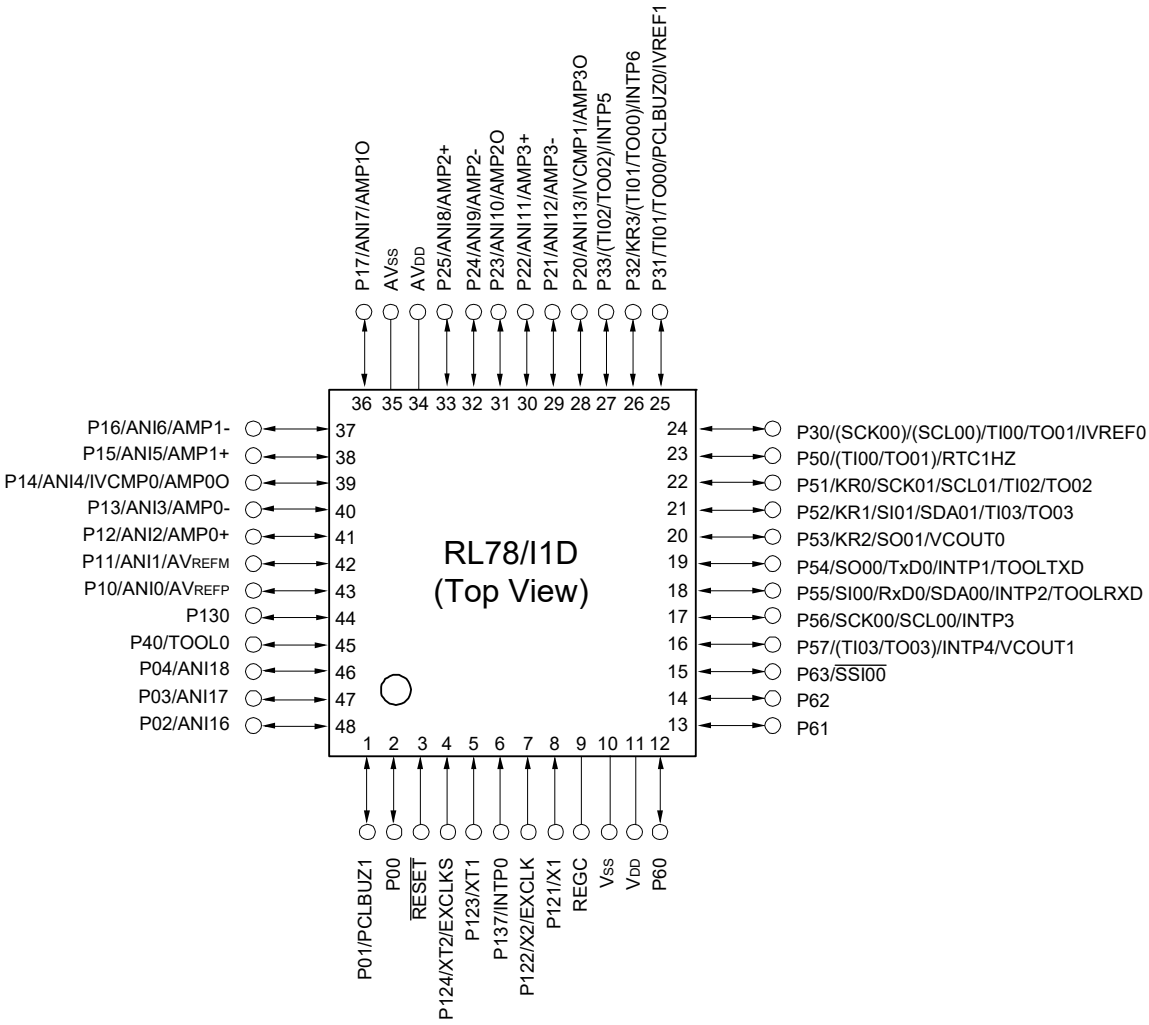
Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

Remark 3. It is recommended to connect an exposed die pad to VSS.

1.3.5 48-pin products

<R> • 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)



Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Caution 2. Make AVss pin the same potential as Vss pin.

Caution 3. Make AVDD pin the same potential as VDD pin.

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

1.6 Outline of Functions

Remark This outline describes the functions at the time when Peripheral I/O redirection register 0 (PIOR0) are set to 00H.

(1/2)

<R>

Item		20-pin	24-pin	30-pin	32-pin	48-pin
		R5F1176x (x = 8, A)	R5F1177x (x = 8, A)	R5F117Ax (x = 8, A, C)	R5F117Bx (x = A, C)	R5F117Gx (x = A, C)
Code flash memory (KB)		8 to 16 KB	8 to 16 KB	8 to 32 KB	16 to 32 KB	16 to 32 KB
Data flash memory (KB)		2 KB	2 KB	2 KB	2 KB	2 KB
RAM		0.7 to 2.0 KB	0.7 to 2.0 KB	0.7 to 3.0 KB Note	2.0 to 3.0 KB Note	2.0 to 3.0 KB Note
Address space		1 MB				
Main system clock	High-speed system clock (f_{MX})	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode:1 to 20 MHz (V_{DD} = 2.7 to 3.6 V), HS (High-speed main) mode:1 to 16 MHz (V_{DD} = 2.4 to 3.6 V), LS (Low-speed main) mode:1 to 8 MHz (V_{DD} = 1.8 to 3.6 V), LV (Low-voltage main) mode:1 to 4 MHz (V_{DD} = 1.6 to 3.6 V), LP (Low-power main) mode:1 MHz (V_{DD} = 1.8 to 3.6 V)				
	High-speed on-chip oscillator clock (f_{IH}) Max: 24 MHz	HS (High-speed main) mode: 1 to 24 MHz (V_{DD} = 2.7 to 3.6 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 3.6 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 3.6 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 3.6 V), LP (Low-power main) mode: 1 MHz (V_{DD} = 1.8 to 3.6 V)				
	Middle-speed on-chip oscillator clock (f_{IM}) Max: 4 MHz					
Subsystem clock	Subsystem clock oscillator (f_{SX}, f_{SXR})	—		XT1 (crystal) oscillation 32.768 kHz (TYP.): V_{DD} = 1.6 to 3.6 V		
	Low-speed on-chip oscillator clock (f_{IL})	15 kHz (TYP.): V_{DD} = 1.6 to 3.6 V				
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f_{IH} = 24 MHz operation)				
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)				
		—		30.5 μs (Subsystem clock oscillator clock: f_{SX} = 32.768 kHz operation)		
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.				
I/O port	Total	14	18	24	26	42
	CMOS I/O	11	15	19	21	33
	CMOS input	3	3	5	5	5
	N-ch open-drain I/O (6 V tolerance)	—	—	—	—	4
Timer	16-bit timer	4 channels				
	Watchdog timer	1 channel				
	Real-time clock	1 channel				
	12-bit interval timer	1 channel				
	8/16-bit interval timer	4 channels (8 bit) / 2 channels (16 bit)				
	Timer output	2	4	3	4	4
	RTC output	—		1 channel • 1 Hz (subsystem clock generator and RTC/other clock: f_{SX} = 32.768 kHz)		

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.

R5F117xC (x = A, B, G): Start address FF300H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

2.3.2 Supply current characteristics

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

(T_A = +85 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) **(1/4)**

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 24 MHz Note 3, T_A = -40 to +105°C	Basic operation	V_{DD} = 3.0 V			1.4		mA
			HS (high-speed main) mode	f_{IH} = 24 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			3.2	6.3	mA
				f_{IH} = 24 MHz Note 3, T_A = +85 to +105°C	Normal operation	V_{DD} = 3.0 V				6.7	
				f_{IH} = 16 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			2.4	4.6	
				f_{IH} = 16 MHz Note 3, T_A = +85 to +105°C	Normal operation	V_{DD} = 3.0 V				4.9	
			LS (low-speed main) mode (MCSEL = 0)	f_{IH} = 8 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			1.1	2.0	mA
						V_{DD} = 2.0 V			1.1	2.0	
			LS (low-speed main) mode (MCSEL = 1)	f_{IH} = 4 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			0.72	1.30	mA
						V_{DD} = 2.0 V			0.72	1.30	
<R>				f_{IM} = 4 MHz Note 7, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			0.58	1.10	
<R>						V_{DD} = 2.0 V			0.58	1.10	
<R>			LV (low-voltage main) mode	f_{IH} = 3 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			1.2	1.8	mA
						V_{DD} = 2.0 V			1.2	1.8	
			LP (low-power main) mode Note 5 (MCSEL = 1)	f_{IH} = 1 MHz Note 3, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			290	480	µA
						V_{DD} = 2.0 V			290	480	
				f_{IM} = 1 MHz Note 5, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V			124	230	
						V_{DD} = 2.0 V			124	230	
			HS (high-speed main) mode	f_{MX} = 20 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V	Square wave input		2.7	5.3	mA
							Resonator connection		2.8	5.5	
				f_{MX} = 20 MHz Note 2, T_A = +85 to +105°C	Normal operation	V_{DD} = 3.0 V	Square wave input			5.7	
							Resonator connection			5.8	
				f_{MX} = 10 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V	Square wave input		1.8	3.1	
							Resonator connection		1.9	3.2	
				f_{MX} = 10 MHz Note 2, T_A = +85 to +105°C	Normal operation	V_{DD} = 3.0 V	Square wave input			3.4	
							Resonator connection			3.5	
			LS (low-speed main) mode (MCSEL = 0)	f_{MX} = 8 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V	Square wave input		0.9	1.9	mA
							Resonator connection		1.0	2.0	
				f_{MX} = 8 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 2.0 V	Square wave input		0.9	1.9	
							Resonator connection		1.0	2.0	
<R>			LS (low-speed main) mode (MCSEL = 1)	f_{MX} = 4 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V	Square wave input		0.6	1.1	mA
							Resonator connection		0.6	1.2	
<R>				f_{MX} = 4 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 2.0 V	Square wave input		0.6	1.1	
							Resonator connection		0.6	1.2	
			LP (low-power main) mode (MCSEL = 1)	f_{MX} = 1 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 3.0 V	Square wave input		100	190	µA
							Resonator connection		136	250	
				f_{MX} = 1 MHz Note 2, T_A = -40 to +85°C	Normal operation	V_{DD} = 2.0 V	Square wave input		100	190	
							Resonator connection		136	250	

(**Notes** and **Remarks** are listed on the next page.)

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

(T_A = +85 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) **(3/4)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 24 MHz Note 4, T_A = -40 to +85°C	V_{DD} = 3.0 V			0.37	1.83	mA
				f_{IH} = 24 MHz Note 4, T_A = +85 to +105°C	V_{DD} = 3.0 V				2.85	
				f_{IH} = 16 MHz Note 4, T_A = -40 to +85°C	V_{DD} = 3.0 V			0.36	1.38	
				f_{IH} = 16 MHz Note 4, T_A = +85 to +105°C	V_{DD} = 3.0 V				2.08	
			LS (low-speed main) mode (MCSEL = 0)	f_{IH} = 8 MHz Note 4, T_A = -40 to +85°C	V_{DD} = 3.0 V			250	710	µA
					V_{DD} = 2.0 V			250	710	
			LS (low-speed main) mode (MCSEL = 1)	f_{IH} = 4 MHz Note 4, T_A = -40 to +85°C	V_{DD} = 3.0 V			204	400	µA
					V_{DD} = 2.0 V			204	400	
				f_{IM} = 4 MHz Note 7, T_A = -40 to +85°C	V_{DD} = 3.0 V			40	250	
					V_{DD} = 2.0 V			40	250	
<R>			LV (low-voltage main) mode	f_{IH} = 3 MHz Note 4, T_A = -40 to +85°C	V_{DD} = 3.0 V			425	800	µA
					V_{DD} = 2.0 V			425	800	
			LP (low-power main) mode (MCSEL = 1)	f_{IH} = 1 MHz Note 4, T_A = -40 to +85°C	V_{DD} = 3.0 V			192	400	µA
					V_{DD} = 2.0 V			192	400	
<R>				f_{IM} = 1 MHz Note 7, T_A = -40 to +85°C	V_{DD} = 3.0 V			27	100	
					V_{DD} = 2.0 V			27	100	
			HS (high-speed main) mode	f_{MX} = 20 MHz Note 3, T_A = -40 to +85°C	V_{DD} = 3.0 V	Square wave input		0.20	1.55	mA
						Resonator connection		0.40	1.74	
				f_{MX} = 20 MHz Note 3, T_A = +85 to +105°C	V_{DD} = 3.0 V	Square wave input			2.45	
						Resonator connection			2.57	
				f_{MX} = 10 MHz Note 3, T_A = -40 to +85°C	V_{DD} = 3.0 V	Square wave input		0.15	0.86	
						Resonator connection		0.30	0.93	
				f_{MX} = 10 MHz Note 3, T_A = +85 to +105°C	V_{DD} = 3.0 V	Square wave input			1.28	
						Resonator connection			1.36	
			LS (low-speed main) mode (MCSEL = 0)	f_{MX} = 8 MHz Note 3, T_A = -40 to +85°C	V_{DD} = 3.0 V	Square wave input		68	550	µA
						Resonator connection		120	590	
				f_{MX} = 8 MHz Note 3, T_A = -40 to +85°C	V_{DD} = 2.0 V	Square wave input		68	550	
						Resonator connection		120	590	
			LS (low-speed main) mode (MCSEL = 1)	f_{MX} = 4 MHz Note 3, T_A = -40 to +85°C	V_{DD} = 3.0 V	Square wave input		23	128	µA
						Resonator connection		65	200	
				f_{MX} = 1 MHz Note 3, T_A = -40 to +85°C	V_{DD} = 2.0 V	Square wave input		23	128	
						Resonator connection		65	200	
			LP (low-power main) mode (MCSEL = 1)	f_{MX} = 4 MHz Note 3, T_A = -40 to +85°C	V_{DD} = 3.0 V	Square wave input		10	64	µA
						Resonator connection		48	150	
				f_{MX} = 1 MHz Note 3, T_A = -40 to +85°C	V_{DD} = 2.0 V	Square wave input		10	64	
						Resonator connection		48	150	
			Subsystem clock operation	f_{SX} = 32.768 kHz, T_A = -40°C Note 5		Square wave input		0.24	0.57	µA
						Resonator connection		0.42	0.76	
				f_{SX} = 32.768 kHz, T_A = +25°C Note 5		Square wave input		0.30	0.57	
						Resonator connection		0.54	0.76	
				f_{SX} = 32.768 kHz, T_A = +50°C Note 5		Square wave input		0.35	1.17	
						Resonator connection		0.60	1.36	
				f_{SX} = 32.768 kHz, T_A = +70°C Note 5		Square wave input		0.42	1.97	
						Resonator connection		0.70	2.16	
				f_{SX} = 32.768 kHz, T_A = +85°C Note 5		Square wave input		0.80	3.37	
						Resonator connection		0.95	3.56	
				f_{SX} = 32.768 kHz, T_A = +105°C Note 5		Square wave input		1.80	17.10	
						Resonator connection		2.20	17.50	
				f_{IL} = 15 kHz, T_A = -40°C Note 6				0.40	1.22	µA
				f_{IL} = 15 kHz, T_A = +25°C Note 6				0.47	1.22	
				f_{IL} = 15 kHz, T_A = +85°C Note 6				0.80	3.30	
				f_{IL} = 15 kHz, T_A = +105°C Note 6				2.00	17.30	

(**Notes** and **Remarks** are listed on the next page.)

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

(T_A = +85 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Self-programming operating current	I_{FSP} Notes 1, 3				2.0	12.20	mA
BGO current	I_{BGO} Notes 1, 2				2.0	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation AV_{REFP} = V_{DD} =3.0 V T_A = -40 to +85°C	The mode is performed Note 5		0.50	0.60	mA
			The A/D conversion operations are performed Note 1		0.60	0.75	mA
			The A/D conversion operations are performed Note 4		420	720	μA
		ADC operation AV_{REFP} = V_{DD} =3.0 V T_A = +85 to +105°C	The mode is performed Note 5		0.50	1.10	mA
			The A/D conversion operations are performed Note 1		0.60	1.34	mA
			The A/D conversion operations are performed Note 4		420	720	μA
		CSI/UART operation	T_A = -40 to +85°C		0.70	0.84	mA
			T_A = +85 to +105°C		0.70	1.54	mA

Note 1. Current flowing to V_{DD}.

Note 2. Current flowing during programming of the data flash.

Note 3. Current flowing during self-programming.

Note 4. Current flowing to AV_{DD}.

<R> **Note 5.** For shift time to the SNOOZE mode, see 23.3.3 SNOOZE mode in the RL78/I1D User's Manual.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. Temperature condition of the TYP. value is T_A = 25°C

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

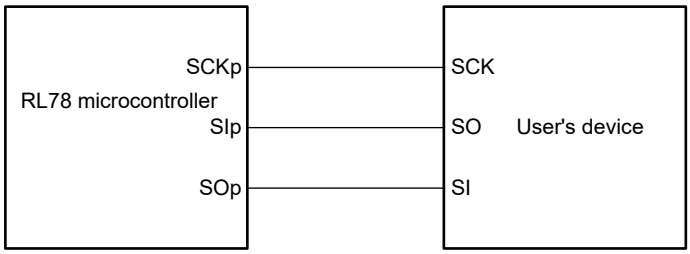
(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{SSI00}$ setup time	t_{SSIK}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 3.6 V	120		120		120		120		ns
			2.4 V ≤ V_{DD} < 2.7 V	200		200		200		200		
			1.8 V ≤ V_{DD} < 2.4 V	—								
			1.6 V ≤ V_{DD} < 1.8 V	—		—		—		400		
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 3.6 V	1/f_{MCK} + 120		1/f_{MCK} + 120		1/f_{MCK} + 120		1/f_{MCK} + 120		ns
			2.4 V ≤ V_{DD} < 2.7 V	1/f_{MCK} + 200		1/f_{MCK} + 200		1/f_{MCK} + 200		1/f_{MCK} + 200		
			1.8 V ≤ V_{DD} < 2.4 V	—								
			1.6 V ≤ V_{DD} < 1.8 V	—		—		—		1/f_{MCK} + 400		
$\overline{SSI00}$ hold time	t_{KSSI}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 3.6 V	1/f_{MCK} + 120		1/f_{MCK} + 120		1/f_{MCK} + 120		1/f_{MCK} + 120		ns
			2.4 V ≤ V_{DD} < 2.7 V	1/f_{MCK} + 200		1/f_{MCK} + 200		1/f_{MCK} + 200		1/f_{MCK} + 200		
			1.8 V ≤ V_{DD} < 2.4 V	—								
			1.6 V ≤ V_{DD} < 1.8 V	—		—		—		1/f_{MCK} + 400		
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 3.6 V	120		120		120		120		ns
			2.4 V ≤ V_{DD} < 2.7 V	200		200		200		200		
			1.8 V ≤ V_{DD} < 2.4 V	—								
			1.6 V ≤ V_{DD} < 1.8 V	—		—		—		400		

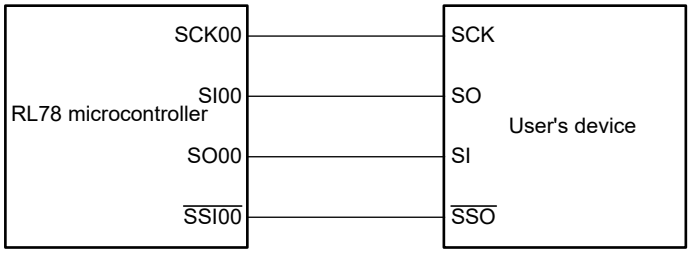
Caution **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

CSI mode connection diagram (during communication at same potential)



CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))



Remark 1. p: CSI number (p = 00, 01)
Remark 2. m: Unit number, n: Channel number (mn = 00, 01)

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

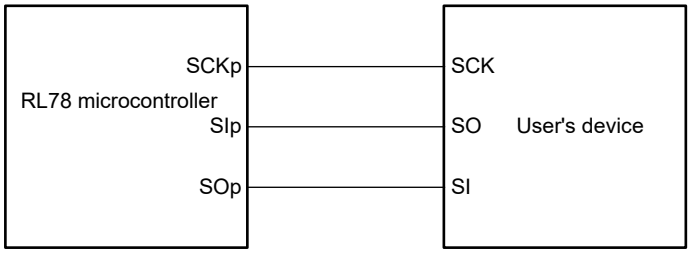
(T_A = +85 to +105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
$\overline{SSI00}$ setup time	t_{SSIK}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 3.6 V	240		ns
			2.4 V ≤ V_{DD} < 2.7 V	400		ns
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 3.6 V	1/f_{MCK} + 240		ns
			2.4 V ≤ V_{DD} < 2.7 V	1/f_{MCK} + 400		ns
$\overline{SSI00}$ hold time	t_{KSSI}	DAPmn = 0	2.7 V ≤ V_{DD} ≤ 3.6 V	1/f_{MCK} + 240		ns
			2.4 V ≤ V_{DD} < 2.7 V	1/f_{MCK} + 400		ns
		DAPmn = 1	2.7 V ≤ V_{DD} ≤ 3.6 V	240		ns
			2.4 V ≤ V_{DD} < 2.7 V	400		ns

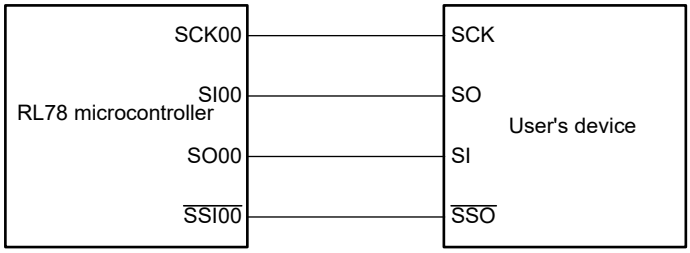
Caution **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

CSI mode connection diagram (during communication at same potential)

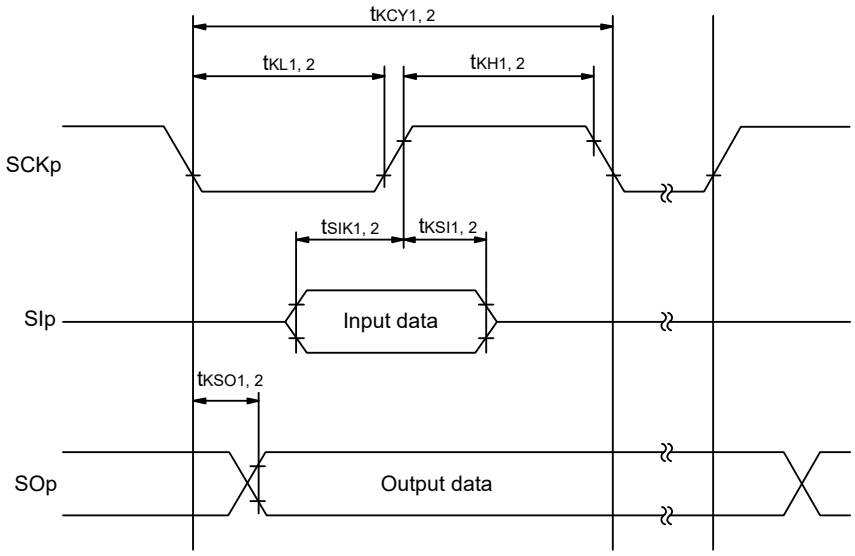


CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))

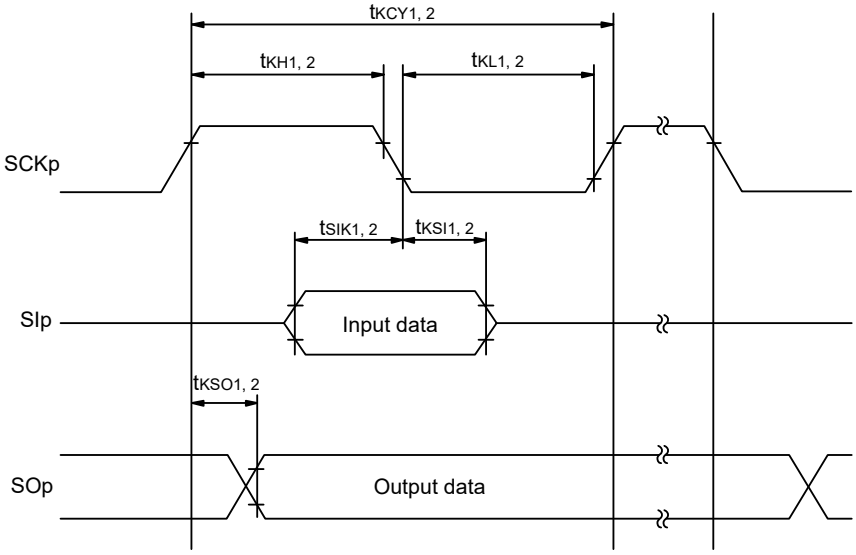


Remark 1. p: CSI number (p = 00, 01)
Remark 2. m: Unit number, n: Channel number (mn = 00, 01)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01)
Remark 2. m: Unit number, n: Channel number (mn = 00, 01)

(5) During communication at same potential (simplified I²C mode)

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1		250 Note 1		400 Note 1	kHz
		1.8 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ		—							
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		—		300 Note 1		250 Note 1		300 Note 1	
		1.7 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		—		—		—		250 Note 1	
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		—		—		—			
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		1150		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	—								
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	—		1550		1550		1550		
		1.7 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		—		—		1850		
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		—		—				
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		1150		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	—								
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	—		1550		1550		1550		
		1.7 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		—		—		1850		
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		—		—				
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85 Note 2		1/f_{MCK} + 145 Note 2		1/f_{MCK} + 145 Note 2		1/f_{MCK} + 145 Note 2		ns
		1.8 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	—								
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	—		1/f_{MCK} + 230 Note 2		1/f_{MCK} + 230 Note 2		1/f_{MCK} + 230 Note 2		
		1.7 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		—		—		1/f_{MCK} + 290 Note 2		
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		—		—				
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		1.8 V ≤ V_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	—	—		355		355		355	
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	—	—							
		1.7 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—	—	—	—	—	—		405	
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—	—	—	—	—	—			

(**Notes** and **Caution** are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = +85 to 105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	354		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	958		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	38		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		390	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		966	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	88		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	220		ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	38		ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		50	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. Use it with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

(9) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = +85 to 105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	32/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	28/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	24/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	20 MHz < f_{MCK} ≤ 24 MHz	72/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	64/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	52/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	32/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	20/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 36		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 - 100		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 40		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 428	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 1146	ns

(**Notes** and **Caution** are listed on the next page. **Remarks** are listed on the page after the next page.)

(10) Communication at different potential (1.8 V, 2.5 V) (simplified I²C mode)

(T_A = -40 to 85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
		2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ		300 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1550		1550		1550		ns
		2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150		1550		1550		1550		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1550		1550		1550		1550		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	200		610		610		610		ns
		2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600		610		610		610		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	610		610		610		610		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		1/f_{MCK} + 190 Note 2		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
		2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		2.7 V ≤ V_{DD} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	0	355	0	355	0	355	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	0	405	0	405	0	405	0	405	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.

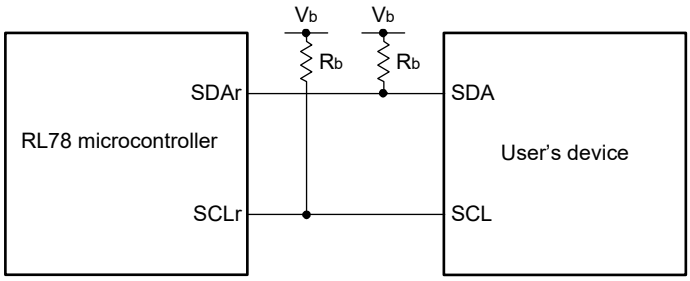
Note 2. Use it with V_{DD} ≥ V_b.

Note 3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

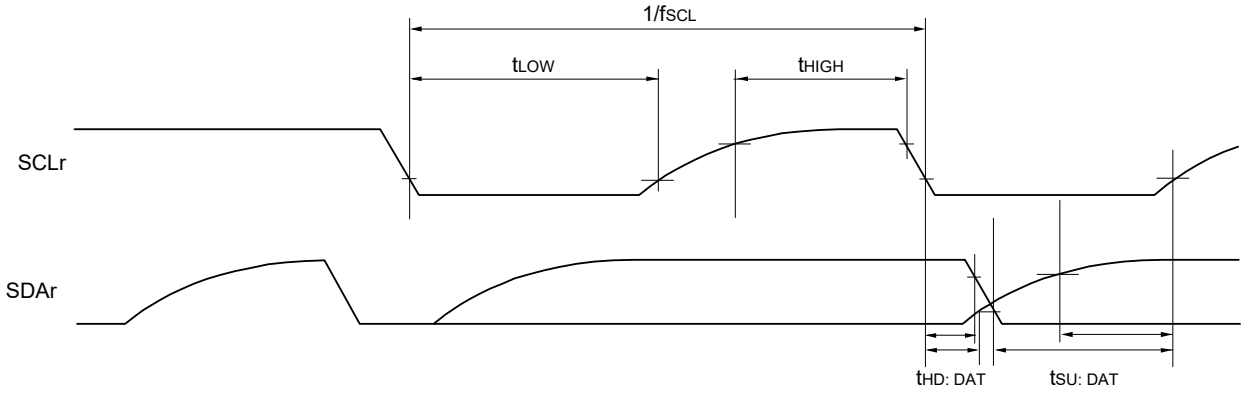
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)

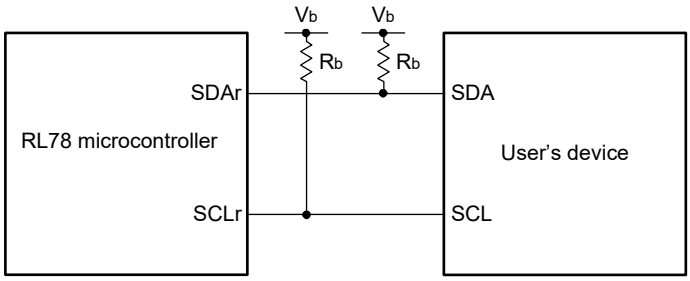


Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

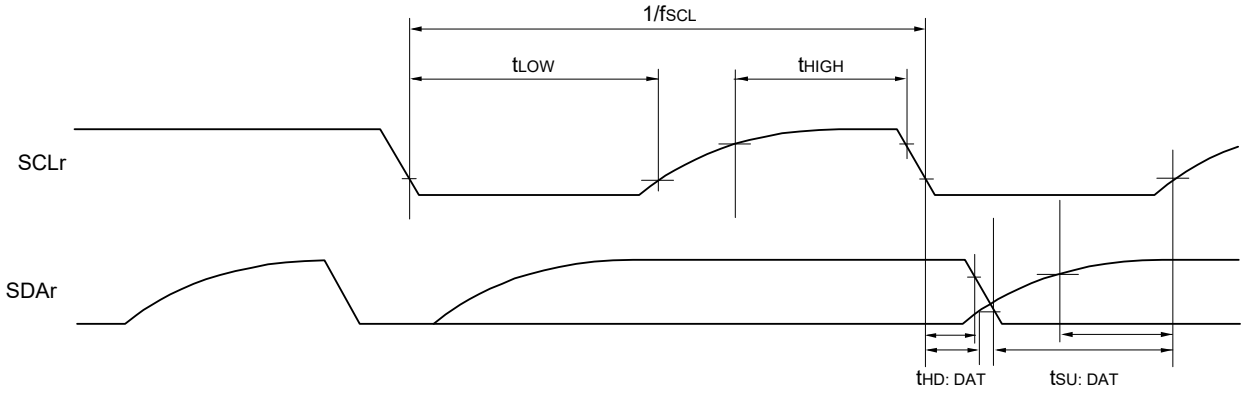
Remark 2. r: IIC number (r = 00, 01), g: PIM, POM number (g = 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01), g: PIM and POM numbers (g = 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01)

(1) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), conversion target: ANI2 to ANI13

(TA = -40 to +85°C, 1.6 V ≤ AVREFP ≤ AVDD = VDD ≤ 3.6 V, VSS = 0 V, AVSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	8		12	bit
			1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.5	
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	3.375			µs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	6.75			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	13.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	2.5625			
			1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	5.125			
			1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	10.25			
Zero-scale error Note 3	EZS	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±4.5	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±4.5	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.0	
Full-scale error Note 3	EFS	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±4.5	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±4.5	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.0	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±1.5	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±1.0	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±1.5	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±1.5	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±1.0	
Analog input voltage	VAIN			0		AVREFP	V

Note 1. Cannot be used for lower 2 bit of ADCR register

Note 2. Cannot be used for lower 4 bit of ADCR register

Note 3. Excludes quantization error (±1/2 LSB).

Caution Always use AVDD pin with the same potential as the VDD pin.

(3) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), conversion target: ANI16 to ANI18, internal reference voltage, temperature sensor output voltage

(TA = -40 to +85°C, 1.6 V ≤ VDD ≤ 3.6 V, 1.6 V ≤ AVREFP ≤ AVDD = VDD ≤ 3.6 V, VSS = 0 V, AVSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	8		12	bit
			1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±7.0	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±3.0	
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	4.125			µs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	3.3125			
			1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	7.875			
			1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	54.25			
Zero-scale error Note 3	EZS	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±5.0	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.5	
Full-scale error Note 3	EFS	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±5.0	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.5	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±3.0	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±1.5	
Analog input voltage	VAIN			0		AVREFP	V
		Internal reference voltage (1.8 V ≤ VDD ≤ 3.6 V)		VBGR Note 4			
		Temperature sensor output voltage (1.8 V ≤ VDD ≤ 3.6 V)		VTMP25 Note 4			

Note 1. Cannot be used for lower 2 bits of ADCR register

Note 2. Cannot be used for lower 4 bits of ADCR register

Note 3. Excludes quantization error (±1/2 LSB).

Note 4. Refer to **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

Caution Always use AVDD pin with the same potential as the VDD pin.

(7) When reference voltage (+) = AVDD (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = AVSS (ADREFM = 0), conversion target: ANI0 to ANI13

(T_A = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = 0 V, AVSS = 0 V, Reference voltage (+) = AVDD, Reference voltage (-) = AVSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AVDD ≤ 3.6 V	8		12	bit
Overall error Note	AINL	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±7.5	LSB
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V	3.375			µs
Zero-scale error Note	EZS	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±6.0	LSB
Full-scale error Note	EFS	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±6.0	LSB
Integral linearity error Note	ILE	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±3.0	LSB
Differential linearity error Note	DLE	12-bit resolution	2.4 V ≤ AVDD ≤ 3.6 V			±2.0	LSB
Analog input voltage	VAIN			0		AVDD	V

Note Excludes quantization error (±1/2 LSB).

Caution Always use AVDD pin with the same potential as the VDD pin.

(10) When reference voltage (+) = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVSS (ADREFM = 0), conversion target: ANI0 to ANI13, ANI16 to ANI18

(T_A = +85 to +105°C, 2.4 V ≤ V_{DD}, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = internal reference voltage, Reference voltage (-) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES			8		bit
Conversion time	tCONV	8-bit resolution	16.0			µs
Zero-scale error Note	EZS	8-bit resolution			±4.0	LSB
Integral linearity error Note	ILE	8-bit resolution			±2.0	LSB
Differential linearity error Note	DLE	8-bit resolution			±2.5	LSB
Analog input voltage	VAIN		0		V_{BGR}	V

Note Excludes quantization error (±1/2 LSB).

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

2.6.2 Temperature sensor, internal reference voltage output characteristics

(T_A = -40 to 85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)
(T_A = +85 to 105°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 3.6 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.50	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tAMP	2.4 V ≤ V_{DD} ≤ 3.6 V	5			µs
		1.8 V ≤ V_{DD} < 2.4 V	10			

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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