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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	33
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f117gagfb-30

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/I1D				
			20 pins	24 pins	30 pins	32 pins	48 pins
32 KB	2 KB	3 KB Note	—	—	R5F117AC	R5F117BC	R5F117GC
16 KB	2 KB	2 KB	R5F1176A	R5F1177A	R5F117AA	R5F117BA	R5F117GA
8 KB	2 KB	0.7 KB	R5F11768	R5F11778	R5F117A8	—	—

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.

R5F117xC (x = A, B, G): Start address FF300H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

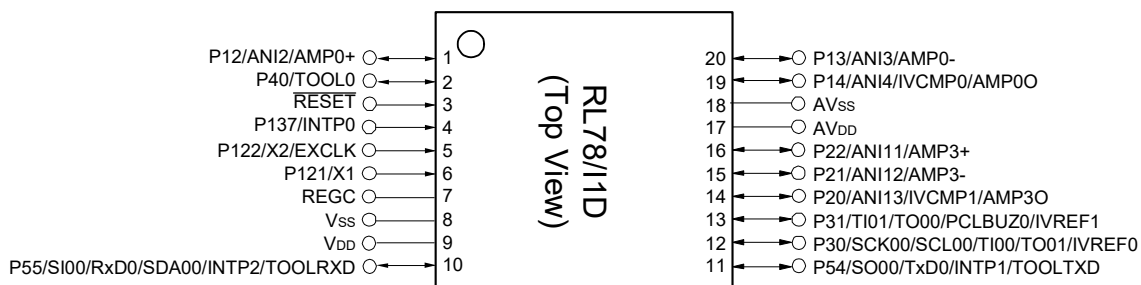
Pin count	Package	Ordering Part Number
20 pins	20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)	R5F11768GSP#30, R5F1176AGSP#30, R5F11768GSP#50, R5F1176AGSP#50
24 pins	24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)	R5F11778GNA#U0, R5F1177AGNA#U0, R5F11778GNA#W0, R5F1177AGNA#W0
30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	R5F117A8GSP#30, R5F117AAGSP#30, R5F117ACGSP#30, R5F117A8GSP#50, R5F117AAGSP#50, R5F117ACGSP#50
32 pins	32-pin plastic HVQFN (5 × 5 mm, 0.5 mm pitch)	R5F117BAGNA#20, R5F117BCGNA#20, R5F117BAGNA#40, R5F117BCGNA#40
	32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)	R5F117BAGFP#30, R5F117BCGFP#30, R5F117BAGFP#50, R5F117BCGFP#50
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	R5F117GAGFB#30, R5F117GCGFB#30, R5F117GAGFB#50, R5F117GCGFB#50

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 20-pin products

<R> • 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65 mm pitch)



Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

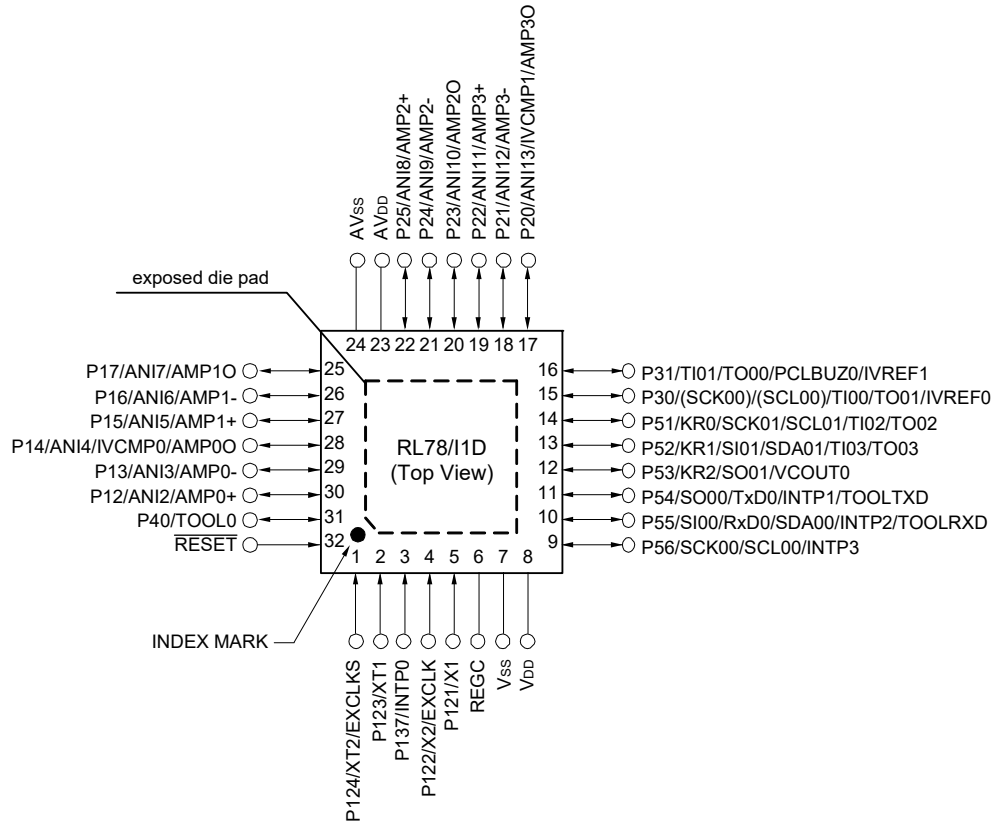
Caution 2. Make AVss pin the same potential as Vss pin.

Caution 3. Make AVDD pin the same potential as VDD pin.

Remark For pin identification, see 1.4 Pin Identification.

1.3.4 32-pin products

- <R> • 32-pin plastic HVQFN (5 × 5 mm, 0.5 mm pitch)



Caution 1. Connect the REGC pin to V_{ss} pin via a capacitor (0.47 to 1 μF).

Caution 2. Make AV_{SS} pin the same potential as V_{ss} pin.

Caution 3. Make AV_{DD} pin the same potential as V_{DD} pin.

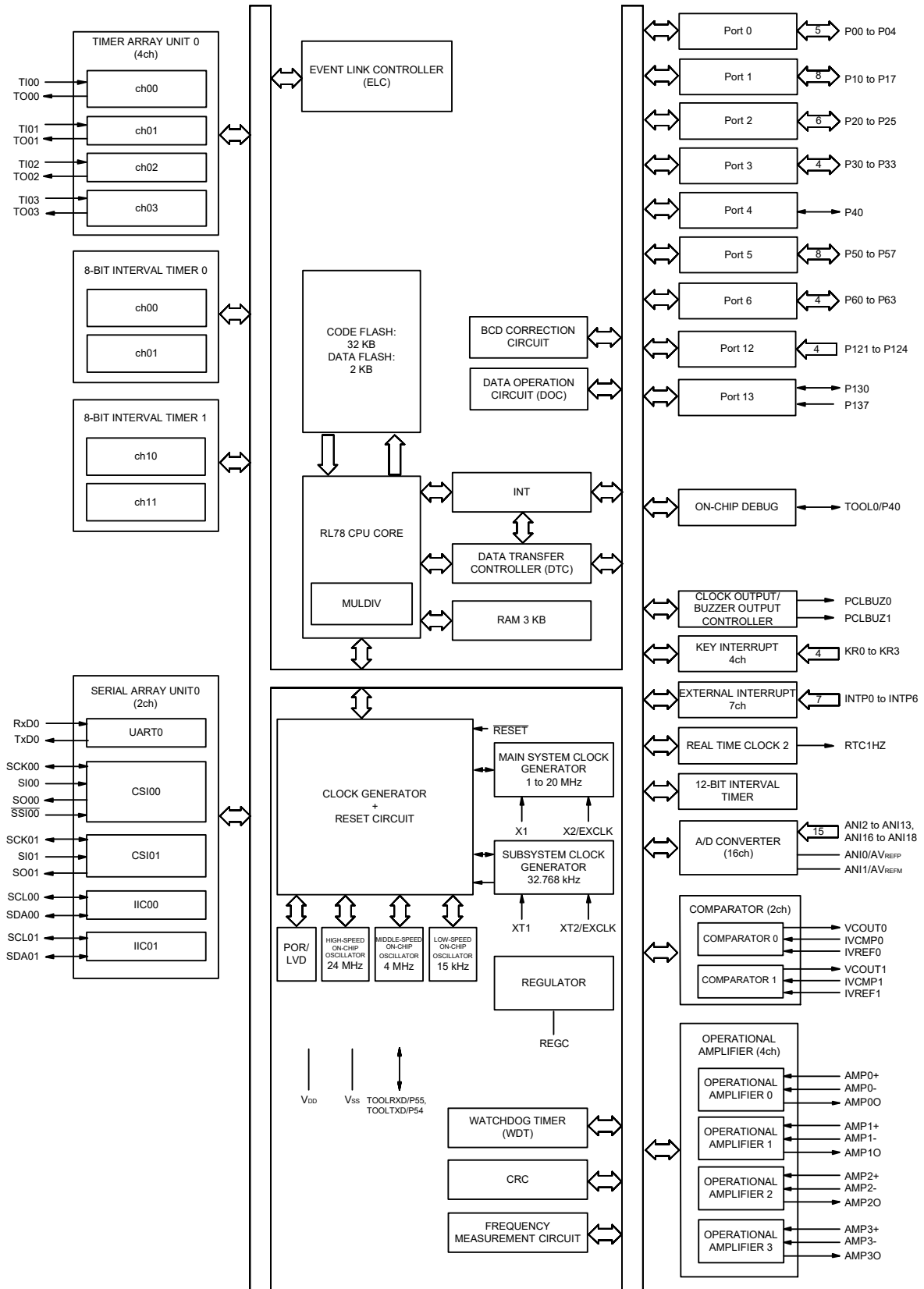
Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

Remark 3. It is recommended to connect an exposed die pad to V_{ss}.

1.5 Block Diagram

1.5.1 48-pin products



($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

($T_A = +85$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

(4/5)

<R>

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output voltage, high	VOH1	P00 to P04, P30 to P33, P40, P50 to P57, P130	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -2.0\text{ mA}$			$V_{DD} - 0.6$	V
			$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ Note 3, $I_{OH} = -1.5\text{ mA}$			$V_{DD} - 0.5$	V
			$1.6\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ Note 1, $I_{OH} = -1.0\text{ mA}$			$V_{DD} - 0.5$	V
	VOH2	P10 to P17, P20 to P25	$1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ Note 2, $I_{OH} = -100\text{ }\mu\text{A}$			$AV_{DD} - 0.5$	V
Output voltage, low	VOL1	P00 to P04, P30 to P33, P40, P50 to P57, P130	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 3.0\text{ mA}$			0.6	V
			$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 1.5\text{ mA}$			0.4	V
			$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ Note 3, $I_{OL} = 0.6\text{ mA}$			0.4	V
			$1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ Note 1, $I_{OL} = 0.3\text{ mA}$			0.4	V
	VOL2	P10 to P17, P20 to P25	$1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ Note 2, $I_{OL} = 400\text{ }\mu\text{A}$			0.4	V
	VOL3	P60 to P63	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 3.0\text{ mA}$			0.4	V
			$1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ Note 3, $I_{OL} = 2.0\text{ mA}$			0.4	V
			$1.6\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ Note 1, $I_{OL} = 1.0\text{ mA}$			0.4	V

Note 1. Only $T_A = -40$ to $+85^\circ\text{C}$ is guaranteed.

Note 2. The condition that $2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$ is guaranteed when $+85^\circ\text{C} < T_A \leq +105^\circ\text{C}$.

Note 3. The condition that $2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ is guaranteed when $+85^\circ\text{C} < T_A \leq +105^\circ\text{C}$.

Caution P30 and P51 to P56 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.4 AC Characteristics

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

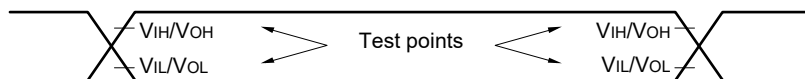
(1/2)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	TCY	Main system clock (fMAIN) operation	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 3.6 V	0.04167		1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 3.6 V PMMC. MCSEL = 0	0.125		1	μs
				1.8 V ≤ VDD ≤ 3.6 V PMMC. MCSEL = 1	0.25		1	μs
			LP (low-power main) mode	1.8 V ≤ VDD ≤ 3.6 V	1			μs
			LV (low-voltage main) mode	1.8 V ≤ VDD ≤ 3.6 V	0.25		1	μs
		1.6 V ≤ VDD < 1.8 V		0.34		1	μs	
		Subsystem clock (fSUB) operation	fsx	1.8 V ≤ VDD ≤ 3.6 V	28.5	30.5	31.3	μs
			fil	1.8 V ≤ VDD ≤ 3.6 V		66.7		μs
		In the self- programming mode	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 3.6 V	0.04167		1	μs
2.4 V ≤ VDD < 2.7 V	0.0625				1	μs		
LS (low-speed main) mode	1.8 V ≤ VDD ≤ 3.6 V		0.125		1	μs		
LV (low-voltage main) mode	1.8 V ≤ VDD ≤ 3.6 V		0.25		1	μs		
External system clock frequency	fEX	2.7 V ≤ VDD ≤ 3.6 V		1.0		20.0	MHz	
		2.4 V ≤ VDD < 2.7 V		1.0		16.0	MHz	
		1.8 V ≤ VDD < 2.4 V		1		8	MHz	
		1.6 V ≤ VDD < 1.8 V		1		4	MHz	
	fEXS			32		35	kHz	
External system clock input high-level width, low-level width	tEXH, tEXL	2.7 V ≤ VDD ≤ 3.6 V		24			ns	
		2.4 V ≤ VDD < 2.7 V		30			ns	
		1.8 V ≤ VDD < 2.4 V		60			ns	
		1.6 V ≤ VDD < 1.8 V		120			ns	
	tEXHS, tEXLS			13.7			μs	
Ti00 to Ti03 input high-level width, low-level width	tTIH, tTIL			1/fMCK + 10			ns	

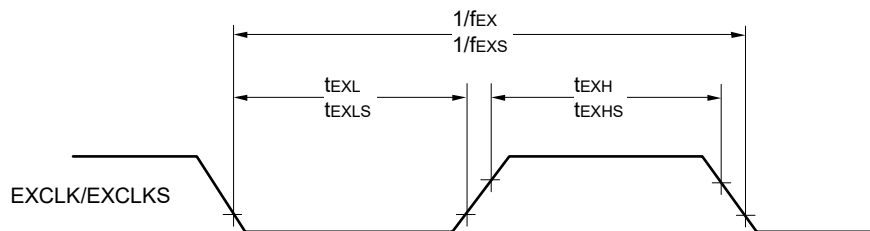
Remark fMCK: Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3))

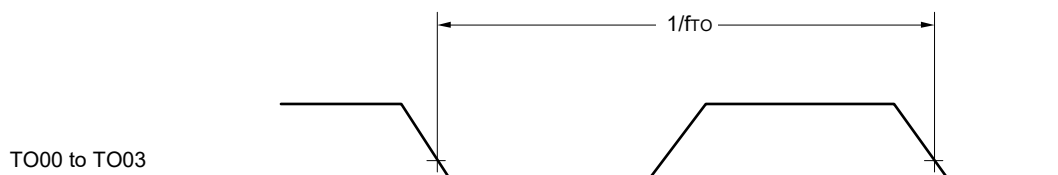
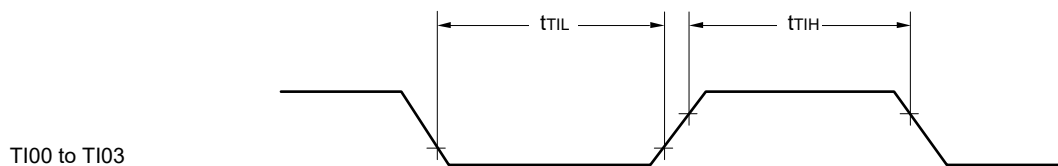
AC Timing Test Points



External System Clock Timing



TI/TO Timing



(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**(TA = +85 to +105°C, 2.7 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	tkCY1	tkCY1 ≥ fCLK/4 2.7 V ≤ VDD ≤ 3.6 V	250		ns
			500		ns
SCKp high-/low-level width	tkH1, tkL1	2.7 V ≤ VDD ≤ 3.6 V	tkCY1/2 - 36		ns
		2.4 V ≤ VDD ≤ 3.6 V	tkCY1/2 - 76		ns
Slp setup time (to SCKp↑) Note 1	tSIK1	2.7 V ≤ VDD ≤ 3.6 V	66		ns
		2.4 V ≤ VDD ≤ 3.6 V	133		ns
Slp hold time (from SCKp↑) Note 2	tKSI1		38		ns
Delay time from SCKp↓ to SOp output Note 3	tKSO1	C = 30 pF Note 4		50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

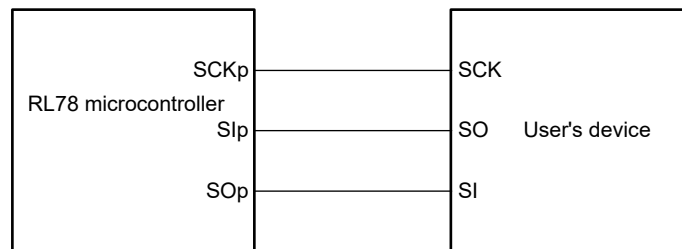
(2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SSi00 setup time	tssik	DAPmn = 0	2.7 V ≤ VDD ≤ 3.6 V	120		120		120		120	ns
			2.4 V ≤ VDD < 2.7 V	200		200		200		200	
			1.8 V ≤ VDD < 2.4 V	—		—		—		—	
			1.6 V ≤ VDD < 1.8 V	—		—		—		400	
		DAPmn = 1	2.7 V ≤ VDD ≤ 3.6 V	1/fMCK + 120		1/fMCK + 120		1/fMCK + 120		1/fMCK + 120	ns
			2.4 V ≤ VDD < 2.7 V	1/fMCK + 200		1/fMCK + 200		1/fMCK + 200		1/fMCK + 200	
			1.8 V ≤ VDD < 2.4 V	—		—		—		—	
			1.6 V ≤ VDD < 1.8 V	—		—		—		1/fMCK + 400	
SSi00 hold time	tkssi	DAPmn = 0	2.7 V ≤ VDD ≤ 3.6 V	1/fMCK + 120		1/fMCK + 120		1/fMCK + 120		1/fMCK + 120	ns
			2.4 V ≤ VDD < 2.7 V	1/fMCK + 200		1/fMCK + 200		1/fMCK + 200		1/fMCK + 200	
			1.8 V ≤ VDD < 2.4 V	—		—		—		—	
			1.6 V ≤ VDD < 1.8 V	—		—		—		1/fMCK + 400	
		DAPmn = 1	2.7 V ≤ VDD ≤ 3.6 V	120		120		120		120	ns
			2.4 V ≤ VDD < 2.7 V	200		200		200		200	
			1.8 V ≤ VDD < 2.4 V	—		—		—		—	
			1.6 V ≤ VDD < 1.8 V	—		—		—		400	

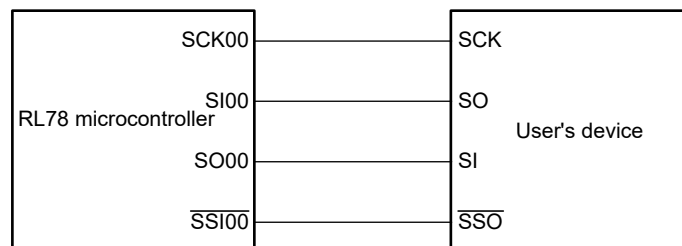
Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

CSI mode connection diagram (during communication at same potential)



**CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))**



Remark 1. p: CSI number (p = 00, 01)

Remark 2. m: Unit number, n: Channel number (mn = 00, 01)

(6) Communication at different potential (1.8 V, 2.5V) (UART mode) (dedicated baud rate generator output)**(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Transfer rate Note 2		Transmission	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V			Note 1		Note 1		Note 1	Note 1	bps	
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V			1.2 Note 2		1.2 Note 2		1.2 Note 2		1.2 Note 2	Mbps
			1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V			Notes 3, 4		Notes 3, 4		Notes 3, 4		Notes 3, 4	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V			0.43 Note 5		0.43 Note 5		0.43 Note 5		0.43 Note 5	Mbps

Note 1. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ and $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}} \times 3 \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

Note 3. Use it with $V_{DD} \geq V_b$.

Note 4. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when $1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}} \times 3 \quad [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 5. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(8) Communication at different potential (1.8 V, 2.5 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 3.6 V, Vss = AVss = 0 V)****(2/2)**

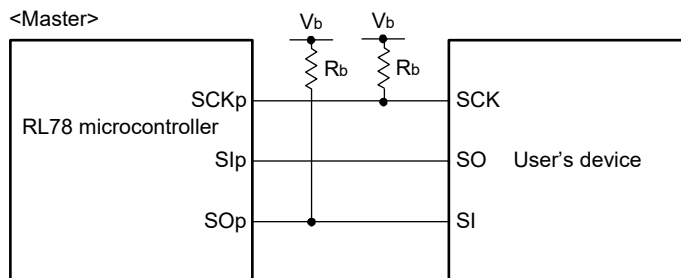
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) Note 1	tsIK1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		479		479		479		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	479		479		479		479		ns
Slp hold time (from SCKp↓) Note 1	tkSH1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		19		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		19		ns
Delay time from SCKp↓ to SOp output Note 1	tkSO1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195		195		195	ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ		483		483		483		483	ns
Slp setup time (to SCKp↓) Note 2	tsIK1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	44		110		110		110		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	110		110		110		110		ns
Slp hold time (from SCKp↓) Note 2	tkSH1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		19		ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		19		ns
Delay time from SCKp↑ to SOp output Note 2	tkSO1	2.7 V ≤ VDD ≤ 3.6 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		25		25		25		25	ns
		1.8 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ		25		25		25		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**Note 3.** Use it with VDD ≥ Vb.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

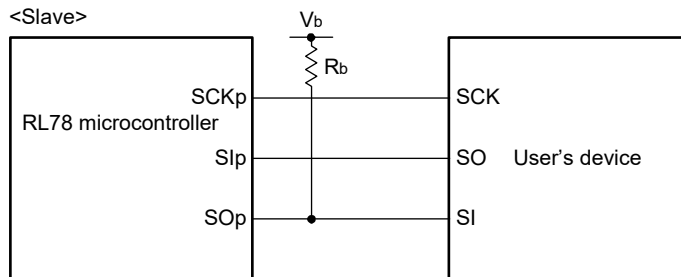


Remark 1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)

Remark 3. f_{mck} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

CSI mode connection diagram (during communication at different potential)



Remark 1. $R_b[\Omega]$: Communication line (SO_p) pull-up resistance, $C_b[F]$: Communication line (SO_p) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(10) Communication at different potential (1.8 V, 2.5 V) (simplified I²C mode)**(TA = -40 to 85°C, 1.8 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)**

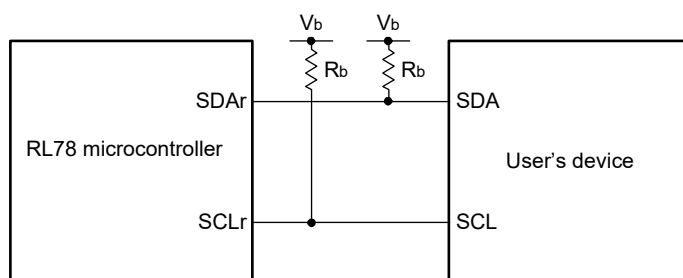
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
		2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		400 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ		300 Note 1		300 Note 1		250 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1550		1550		1550		ns
		2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1150		1550		1550		1550		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ	1550		1550		1550		1550		ns
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	200		610		610		610		ns
		2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	600		610		610		610		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ	610		610		610		610		ns
Data setup time (reception)	t _{SU-DAT}	2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 Note 3		1/f _{MCK} + 190 Note 2		1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		ns
		2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		ns
Data hold time (transmission)	t _{HD-DAT}	2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		2.7 V ≤ V _{DD} ≤ 3.6 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	355	0	355	0	355	0	355	ns
		1.8 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ	0	405	0	405	0	405	0	405	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.**Note 2.** Use it with V_{DD} ≥ V_b.**Note 3.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

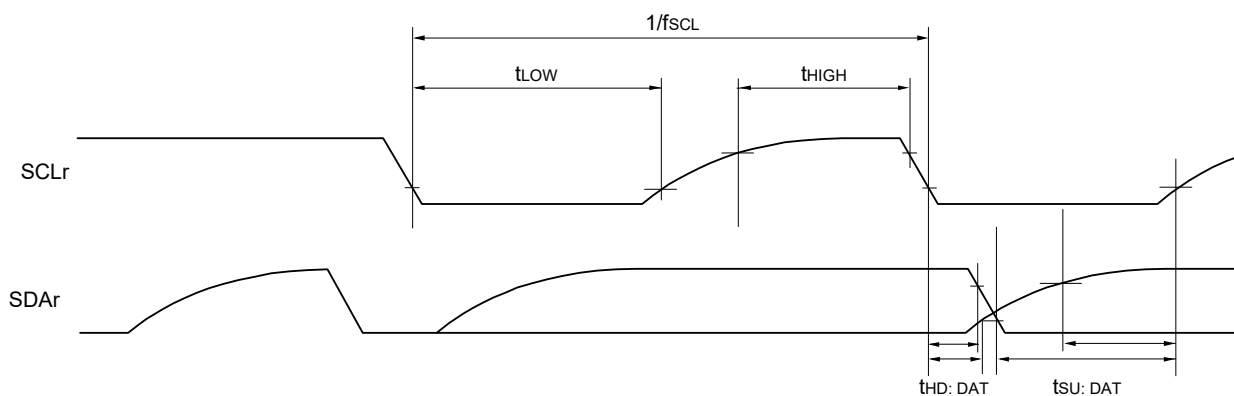
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



- Remark 1.** $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
- Remark 2.** r: IIC number (r = 00, 01), g: PIM and POM numbers (g = 5)
- Remark 3.** f_{mck} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0, 1), mn = 00, 01)

2.6.4 Operational amplifier characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

($T_A = +85$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Common mode input range	Vicm1	Low-power consumption mode		0.2		$AV_{DD} - 0.5$	V
	Vicm2	High-speed mode		0.3		$AV_{DD} - 0.6$	V
Output voltage range	Vo1	Low-power consumption mode		0.1		$AV_{DD} - 0.1$	V
	Vo2	High-speed mode		0.1		$AV_{DD} - 0.1$	V
Input offset voltage	Vioff			-10		10	mV
Open gain	Av			60	120		dB
Gain-bandwidth (GB) product	GBW1	Low-power consumption mode			0.04		MHz
	GBW2	High-speed mode			1.7		MHz
Phase margin	PM	CL = 20 pF		50			deg
Gain margin	GM	CL = 20 pF		10			dB
Equivalent input noise	Vnoise1	f = 1 kHz	Low-power consumption mode		230		nV/ $\sqrt{\text{Hz}}$
	Vnoise2	f = 10 kHz			200		nV/ $\sqrt{\text{Hz}}$
	Vnoise3	f = 1 kHz	High-speed mode		90		nV/ $\sqrt{\text{Hz}}$
	Vnoise4	f = 2 kHz			70		nV/ $\sqrt{\text{Hz}}$
Power supply reduction ratio	PSRR				90		dB
Common mode signal reduction ratio	CMRR				90		dB
Operation stabilization wait time	Tstd1	CL = 20 pF Only operational amplifier is activated ^{Note}	Low-power consumption mode	650			μs
	Tstd2		High-speed mode	13			μs
	Tstd3	CL = 20 pF Operational amplifier and reference current circuit are activated simultaneously	Low-power consumption mode	650			μs
	Tstd4		High-speed mode	13			μs
Settling time	Tset1	CL = 20 pF	Low-power consumption mode			750	μs
	Tset2		High-speed mode			13	μs
Slew rate	Tslew1	CL = 20 pF	Low-power consumption mode		0.02		V/ μs
	Tslew2		High-speed mode		1.1		V/ μs
Load current	Iload1	Low-power consumption mode		-100		100	μA
	Iload2	High-speed mode		-100		100	μA
Load capacitance	CL					20	pF

Note When the operational amplifier reference current circuit is activated in advance.

(2) LVD Detection Voltage of Interrupt & Reset Mode

(TA = -40 to +85°C, VPDR ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Interrupt and reset mode	VLVDA0	VPOC0, VPOC1, VPOC2 = 0, 0, 0, falling reset voltage	1.60	1.63	1.66	V	
	VLVDA1	LVISO, LVIS1 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	VLVDA2	LVISO, LVIS1 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	VLVDA3	LVISO, LVIS1 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDB0	VPOC0, VPOC1, VPOC2 = 0, 0, 1, falling reset voltage	1.80	1.84	1.87	V	
	VLVDB1	LVISO, LVIS1 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	VLVDB2	LVISO, LVIS1 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	VLVDB3	LVISO, LVIS1 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	VLVDC0	VPOC0, VPOC1, VPOC2 = 0, 1, 0, falling reset voltage	2.40	2.45	2.50	V	
	VLVDC1	LVISO, LVIS1 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	VLVDC2	LVISO, LVIS1 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	VLVDD0	VPOC0, VPOC1, VPOC2 = 0, 1, 1, falling reset voltage	2.70	2.75	2.81	V	
VLVDD1	LVISO, LVIS1 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V	
		Falling interrupt voltage	2.80	2.86	2.91	V	
VLVDD2	LVISO, LVIS1 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V	
		Falling interrupt voltage	2.90	2.96	3.02	V	

(TA = +85 to +105°C, VPDR ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Interrupt and reset mode	VLVDD0	VPOC0, VPOC1, VPOC2 = 0, 1, 1, falling reset voltage	2.64	2.75	2.86	V	
	VLVDD1	LVISO, LVIS1 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	VLVDD2	LVISO, LVIS1 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V

2.6.7 Power supply voltage rising slope characteristics

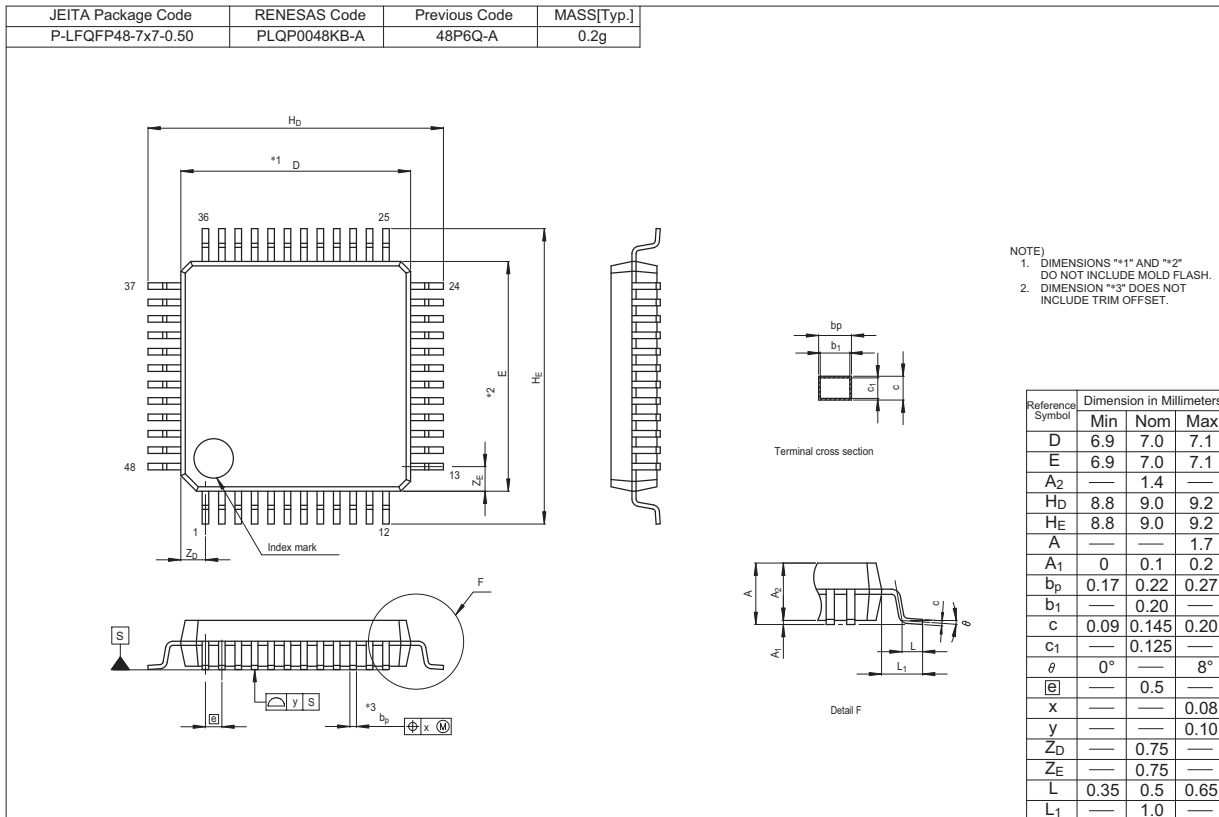
(TA = -40 to +105°C, VSS = AVSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until VDD reaches the operating voltage range shown in 2.4 AC Characteristics.

3.5 48-pin products

<R> R5F117GCGFB, R5F117GAGFB



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