



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

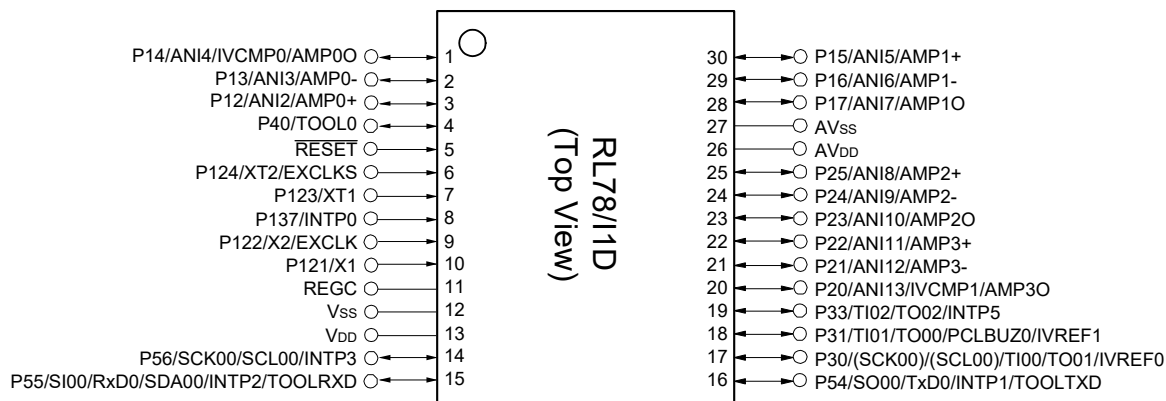
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	33
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 17x8/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f117gagfb-50

1.3.3 30-pin products

<R> • 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

Caution 2. Make AVss pin the same potential as Vss pin.

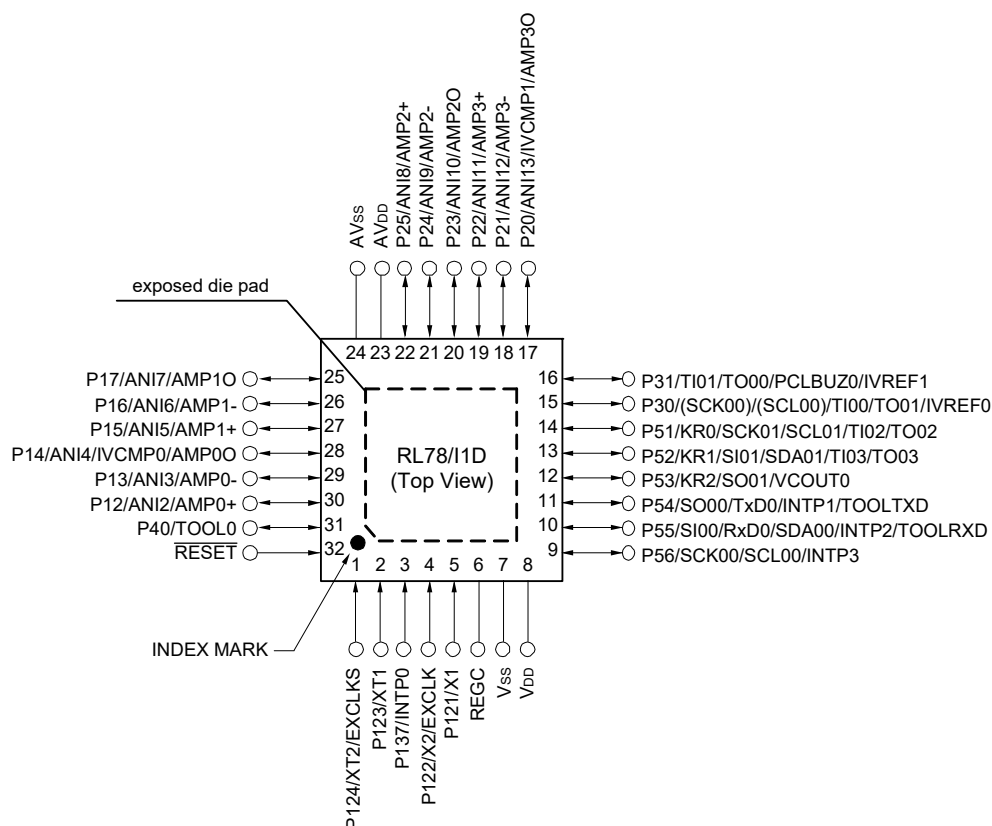
Caution 3. Make AVDD pin the same potential as VDD pin.

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

1.3.4 32-pin products

<R> • 32-pin plastic HVQFN (5 × 5 mm, 0.5 mm pitch)



Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

Caution 2. Make AVss pin the same potential as Vss pin.

Caution 3. Make AVdd pin the same potential as Vdd pin.

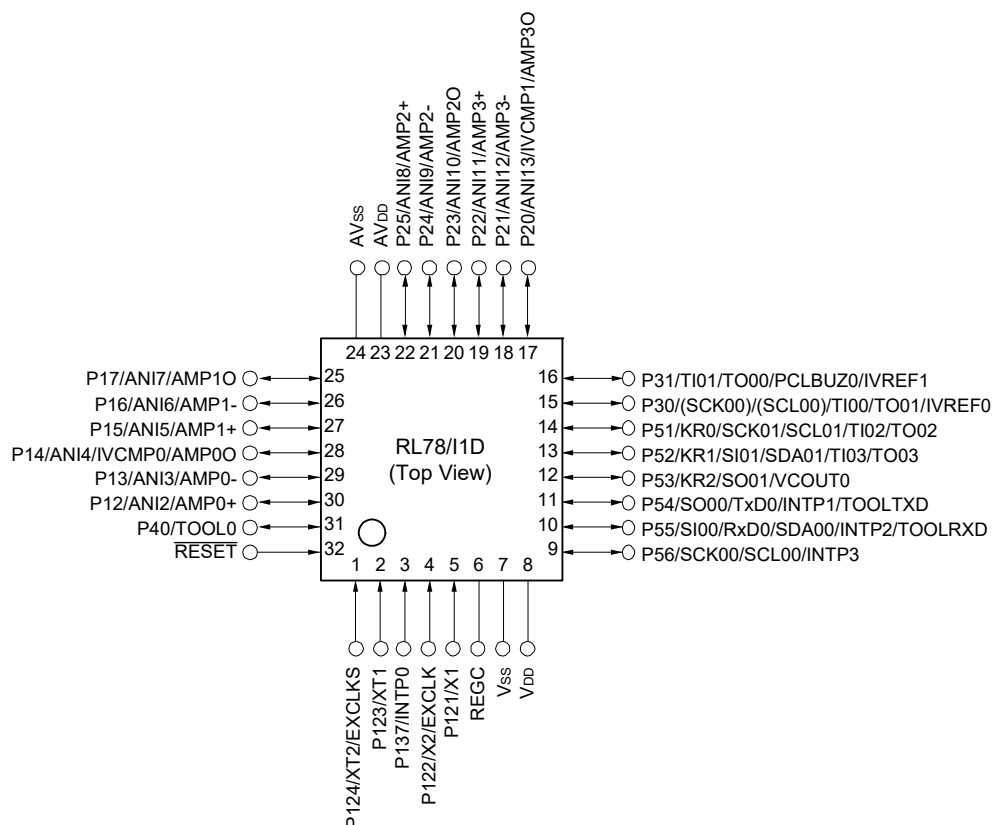
Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

Remark 3. It is recommended to connect an exposed die pad to Vss.

<R>

- 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)



Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μ F).

Caution 2. Make AVss pin the same potential as Vss pin.

Caution 3. Make AVdd pin the same potential as Vdd pin.

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

1.4 Pin Identification

ANI0 to ANI13,	: Analog input	PCLBUZ0, PCLBUZ1	: Programmable clock output/buzzer output
ANI16 to ANI18			
AVDD	: Analog power supply	REGC	: Regulator capacitance
AVREFM	: A/D converter reference potential (- side) input	$\overline{\text{RESET}}$	: Reset
AVREFP	: A/D converter reference potential (+ side) input	RTC1HZ	: Real-time clock correction clock (1 Hz) output
AVss	: Analog ground	RxD0	: Receive data
EXCLK	: External clock input (main system clock)	SCK00, SCK01	: Serial clock input/output
EXCLKS	: External clock input (subsystem clock)	SCL00, SCL01	: Serial clock input/output
INTP0 to INTP6	: External interrupt input	SDA00, SDA01	: Serial data input/output
IVCMP0, IVCMP1	: Comparator input	SI00, SI01	: Serial data input
IVREF0, IVREF1	: Comparator reference input	SO00, SO01	: Serial data output
KR0 to KR3	: Key return	$\overline{\text{SSI00}}$	: Serial interface chip select input
P00 to P04	: Port 0	TI00 to TI03	: Timer input
P10 to P17	: Port 1	TO00 to TO03	: Timer output
P20 to P25	: Port 2	TOOL0	: Data input/output for tool
P30 to P33	: Port 3	TOOLRXD, TOOLTXD	: Data input/output for external device
P40	: Port 4	TxD0	: Transmit data
P50 to P57	: Port 5	VCOU0, VCOU1	: Comparator output
P60 to P63	: Port 6	AMP0+, AMP1+,	: Operational amplifier (+side) input
P121 to P124	: Port 12	AMP2+, AMP3+	
P130, P137	: Port 13	AMP0-, AMP1-,	: Operational amplifier (-side) input
		AMP2-, AMP3-	
		AMP0O, AMP1O,	: Operational amplifier output
		AMP2O, AMP3O	
		VDD	: Power supply
		Vss	: Ground
		X1, X2	: Crystal oscillator (main system clock)
		XT1, XT2	: Crystal oscillator (subsystem clock)

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low Note 1	IOL1	Per pin for P00 to P04, P30 to P33, P40, P50 to P57, P130	TA = -40 to +85°C		20.0 Note 2	mA
			TA = +85 to +105°C		8.5 Note 2	mA
		Per pin for P60 to P63			15.0 Note 2	mA
		Total of P00 to P04, P40, P130 (When duty ≤ 70% Note 3)	2.7 V ≤ VDD ≤ 3.6 V		15.0	mA
			1.8 V ≤ VDD < 2.7 V		9.0	mA
			1.6 V ≤ VDD < 1.8 V		4.5	mA
		Total of P30 to P33, P50 to P57, P60 to P63 (When duty ≤ 70% Note 3)	2.7 V ≤ VDD ≤ 3.6 V		35.0	mA
			1.8 V ≤ VDD < 2.7 V		20.0	mA
			1.6 V ≤ VDD < 1.8 V		10.0	mA
		Total of all pins (When duty ≤ 70% Note 3)			50.0	mA
	IOL2	Per pin for P10 to P17, P20 to P25			0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.6 V ≤ VDD ≤ 3.6 V		5.6	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the Vss pin.**Note 2.** Do not exceed the total current value.**Note 3.** Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(3/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	VIH1	P00 to P04, P30 to P33, P40, P50 to P57, P130	Normal input buffer	0.8 VDD		VDD	V
	VIH2	P30, P32, P33, P51, P52, P54 to P57	TTL input buffer 3.3 V ≤ VDD ≤ 3.6 V	2.0		VDD	V
			TTL input buffer 1.6 V ≤ VDD < 3.3 V	1.5		VDD	V
	VIH3	P10 to P17, P20 to P25		0.7 AVDD		AVDD	V
	VIH4	P60 to P63		0.7 VDD		6.0	V
	VIH5	P121 to P124, P137, EXCLK, EXCLKS, RESET		0.8 VDD		VDD	V
Input voltage, low	VIL1	P00 to P04, P30 to P33, P40, P50 to P57, P130	Normal input buffer	0		0.2 VDD	V
	VIL2	P30, P32, P33, P51, P52, P54 to P57	TTL input buffer 3.3 V ≤ VDD ≤ 3.6 V	0		0.5	V
			TTL input buffer 1.6 V ≤ VDD < 3.3 V	0		0.32	V
	VIL3	P10 to P17, P20 to P25		0		0.3 AVDD	V
	VIL4	P60 to P63		0		0.3 VDD	V
	VIL5	P121 to P124, P137, EXCLK, EXCLKS, RESET		0		0.2 VDD	V

Caution The maximum value of VIH of pins P30 and P51 to P56 is VDD, even in the N-ch open-drain mode.**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

(2/2)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TO00 to TO03 output frequency	fro	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 3.6 V		8	MHz
			2.4 V ≤ VDD < 2.7 V		4	
		LS (low-speed main) mode	1.8 V ≤ VDD ≤ 3.6 V		4	
		LP (low-power main) mode	1.8 V ≤ VDD ≤ 3.6 V		0.5	
		LV (low-voltage main) mode	1.6 V ≤ VDD ≤ 3.6 V		2	
PCLBUZ0, PCLBUZ1 output frequency	fpCL	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 3.6 V		8	MHz
			2.4 V ≤ VDD < 2.7 V		4	
		LS (low-speed main) mode	1.8 V ≤ VDD ≤ 3.6 V		4	
		LP (low-power main) mode	1.8 V ≤ VDD ≤ 3.6 V		1	
		LV (low-voltage main) mode	1.8 V ≤ VDD ≤ 3.6 V		4	
			1.6 V ≤ VDD < 1.8 V		2	
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0 to INTP6	1.6 V ≤ VDD ≤ 3.6 V	1		μs
Key interrupt input low-level width	tKR	KR0 to KR3	1.8 V ≤ VDD ≤ 3.6 V	250		ns
			1.6 V ≤ VDD < 1.8 V	1		μs
RESET low-level width	tRSL			10		μs

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**(TA = +85 to +105°C, 2.4 V ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)****(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 5	tkCY2	2.7 V ≤ VDD < 3.6 V	fMCK > 16 MHz	16/fMCK		ns
			fMCK ≤ 16 MHz	12/fMCK		ns
		2.4 V ≤ VDD < 2.7 V		12/fMCK and 1000		ns
SCKp high-/low-level width	tkH2, tkL2	2.7 V ≤ VDD ≤ 3.6 V		tkCY2/2 - 16		ns
		2.4 V ≤ VDD < 2.7 V		tkCY2/2 - 36		ns
Slp setup time (to SCKp↑) Note 1	tsIK2	2.7 V ≤ VDD ≤ 3.6 V		1/fMCK + 40		ns
		2.4 V ≤ VDD < 2.7 V		1/fMCK + 60		ns
Slp hold time (from SCKp↑) Note 2	tkSI2			1/fMCK + 62		ns
Delay time from SCKp↓ to SOp output Note 3	tkSO2	C = 30 pF Note 4	2.7 V ≤ VDD ≤ 3.6 V		2/fMCK + 66	ns
			2.4 V ≤ VDD < 2.7 V		2/fMCK + 113	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

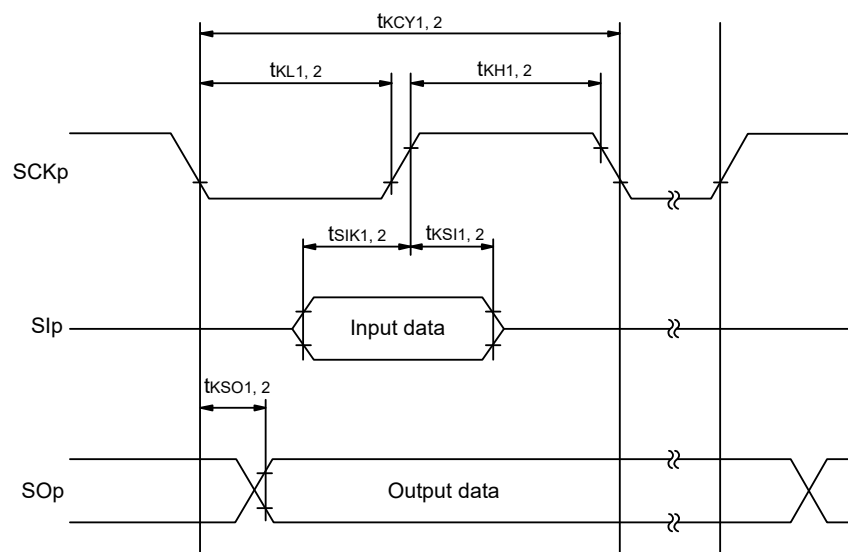
Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

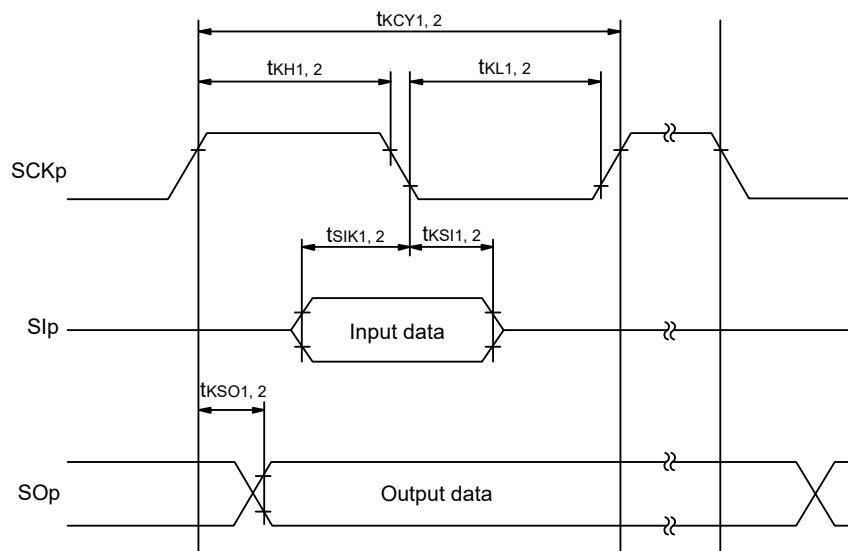
Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 01))

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

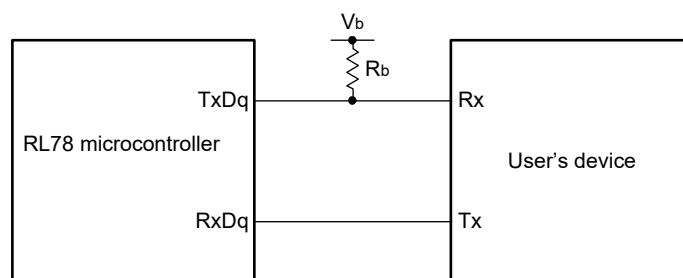
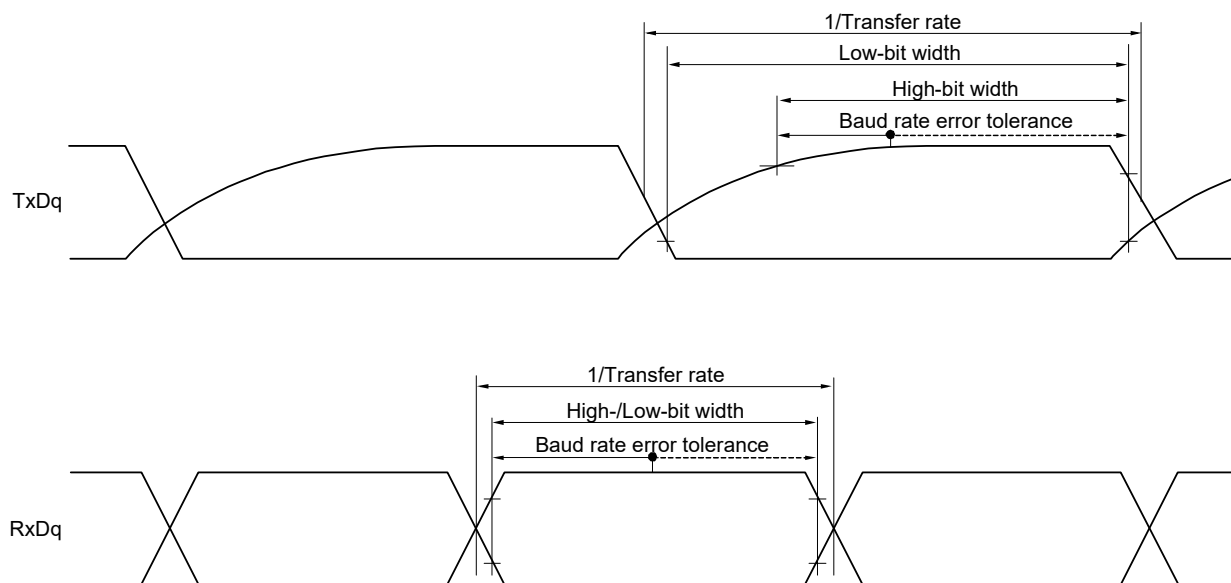


CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01)

Remark 2. m: Unit number, n: Channel number (mn = 00, 01)

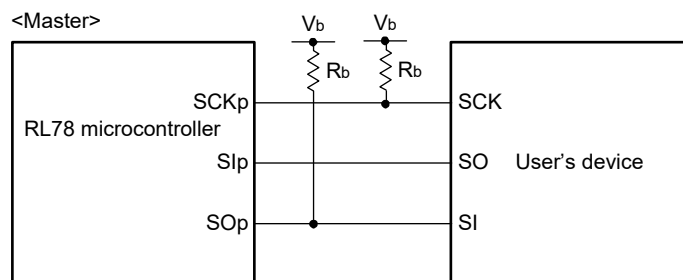
UART mode connection diagram (during communication at different potential)**UART mode bit width (during communication at different potential) (reference)**

Remark 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. q: UART number (q = 0), g: PIM and POM number (g = 5)

Remark 3. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

CSI mode connection diagram (during communication at different potential)

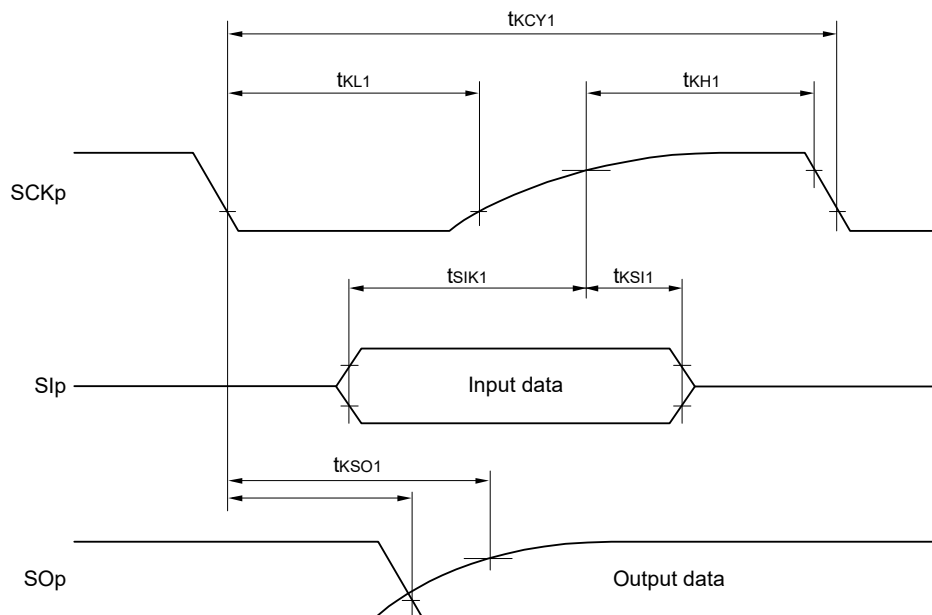
Remark 1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)

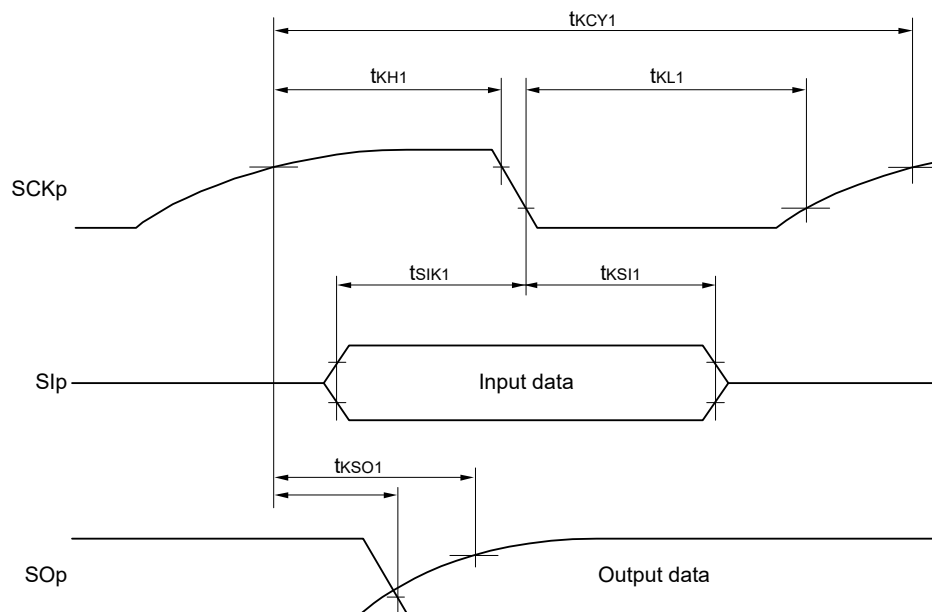
Remark 3. f_{mck} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

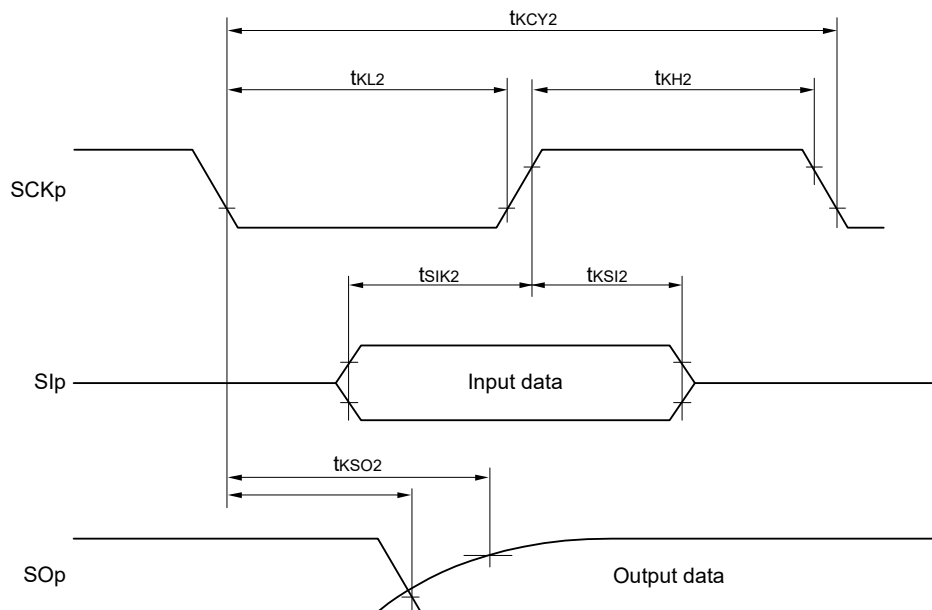


CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

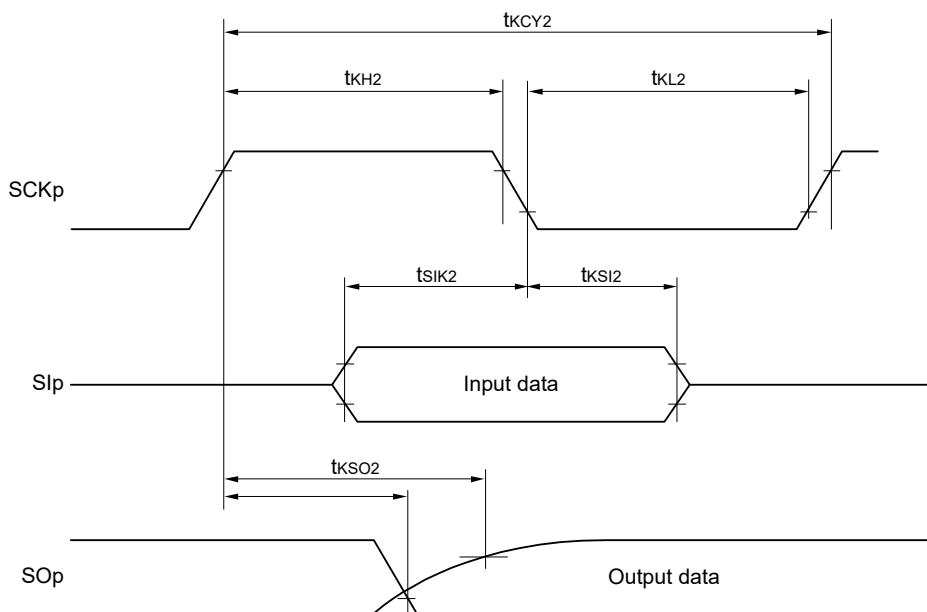


Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 5)

- (8) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), conversion target $ANI16$ to $ANI18$, internal reference voltage, temperature sensor output voltage

($T_A = +85$ to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$, $V_{SS} = 0\text{ V}$, $AV_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	8		12	bit
Overall error ^{Note 1}	AINL	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±7.0	LSB
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V	4.125			μs
Zero-scale error ^{Note 1}	Ezs	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±5.0	LSB
Full-scale error ^{Note 1}	EFS	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±5.0	LSB
Integral linearity error ^{Note 1}	ILE	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±3.0	LSB
Differential linearity error ^{Note 1}	DLE	12-bit resolution	2.4 V ≤ AVREFP ≤ AVDD ≤ 3.6 V			±2.0	LSB
Analog input voltage	VAIN			0		AVREFP	V
		Internal reference voltage (2.4 V ≤ VDD ≤ 3.6 V)		VBGR ^{Note 2}			
		Temperature sensor output voltage (2.4 V ≤ VDD ≤ 3.6 V)		VTMP25 ^{Note 2}			

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. Refer to **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

(9) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = AV_{SS} (ADREFM = 0), conversion target: ANI16 to ANI18, internal reference voltage, temperature sensor output voltage

($T_A = +85$ to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$, $V_{SS} = 0\text{ V}$, $AV_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{DD} , Reference voltage (-) = $AV_{SS} = 0$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$	8		12	bit
Overall error Note 1	AINL	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			± 8.5	LSB
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$	4.125			μs
Zero-scale error Note 1	Ezs	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			± 8.0	LSB
Full-scale error Note 1	Efs	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			± 8.0	LSB
Integral linearity error Note 1	ILE	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			± 3.5	LSB
Differential linearity error Note 1	DLE	12-bit resolution	$2.4\text{ V} \leq AV_{DD} \leq 3.6\text{ V}$			± 2.5	LSB
Analog input voltage	VAIN			0		AV_{DD}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$)		V_{BGR} Note 2			
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$)		V_{TMP25} Note 2			

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. Refer to **2.6.2 Temperature sensor, internal reference voltage output characteristics**.

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

2.6.4 Operational amplifier characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

($T_A = +85$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{DD} = V_{DD} \leq 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Common mode input range	Vicm1	Low-power consumption mode		0.2		AVDD - 0.5	V
	Vicm2	High-speed mode		0.3		AVDD - 0.6	V
Output voltage range	Vo1	Low-power consumption mode		0.1		AVDD - 0.1	V
	Vo2	High-speed mode		0.1		AVDD - 0.1	V
Input offset voltage	Vioff			-10		10	mV
Open gain	Av			60	120		dB
Gain-bandwidth (GB) product	GBW1	Low-power consumption mode			0.04		MHz
	GBW2	High-speed mode			1.7		MHz
Phase margin	PM	CL = 20 pF		50			deg
Gain margin	GM	CL = 20 pF		10			dB
Equivalent input noise	Vnoise1	f = 1 kHz	Low-power consumption mode		230		nV/√Hz
	Vnoise2	f = 10 kHz			200		nV/√Hz
	Vnoise3	f = 1 kHz	High-speed mode		90		nV/√Hz
	Vnoise4	f = 2 kHz			70		nV/√Hz
Power supply reduction ratio	PSRR				90		dB
Common mode signal reduction ratio	CMRR				90		dB
Operation stabilization wait time	Tstd1	CL = 20 pF Only operational amplifier is activated ^{Note}	Low-power consumption mode	650			μs
	Tstd2		High-speed mode	13			μs
	Tstd3	CL = 20 pF Operational amplifier and reference current circuit are activated simultaneously	Low-power consumption mode	650			μs
	Tstd4		High-speed mode	13			μs
Settling time	Tset1	CL = 20 pF	Low-power consumption mode			750	μs
	Tset2		High-speed mode			13	μs
Slew rate	Tslew1	CL = 20 pF	Low-power consumption mode		0.02		V/μs
	Tslew2		High-speed mode		1.1		V/μs
Load current	Iload1	Low-power consumption mode		-100		100	μA
	Iload2	High-speed mode		-100		100	μA
Load capacitance	CL					20	pF

Note When the operational amplifier reference current circuit is activated in advance.

2.6.6 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(TA = -40 to +85°C, VPDR ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	VLVD2	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		VLVD3	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		VLVD4	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		VLVD5	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		VLVD6	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		VLVD7	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		VLVD8	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		VLVD9	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		VLVD10	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		VLVD11	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		VLVD12	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		VLVD13	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		tLW		300			μs
Detection delay time						300	μs

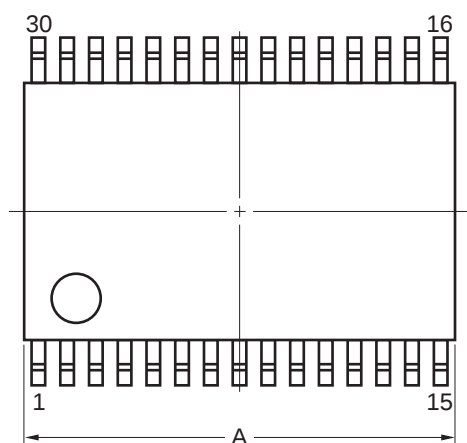
(TA = +85 to +105°C, VPDR ≤ AVDD = VDD ≤ 3.6 V, VSS = AVSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	VLVD2	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		VLVD3	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		VLVD4	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		VLVD5	Power supply rise time	2.71	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		VLVD6	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		VLVD7	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		tLW		300			μs
Detection delay time						300	μs

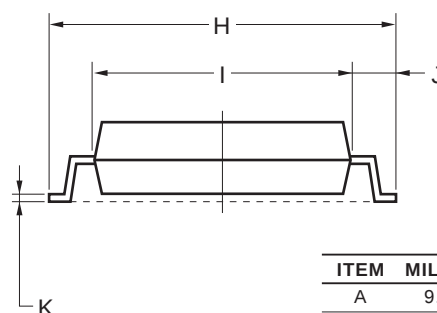
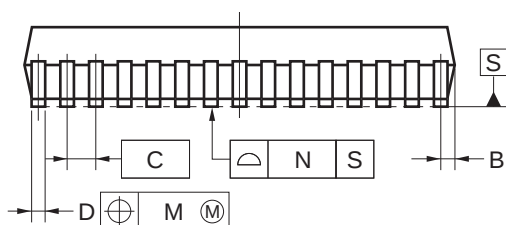
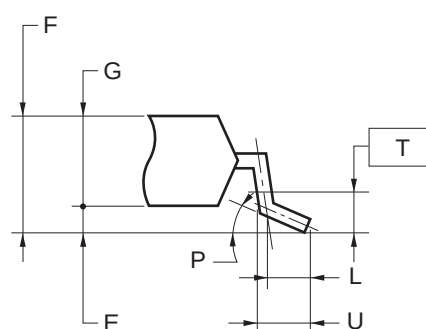
3.3 30-pin products

R5F117ACGSP, R5F117AAGSP, R5F117A8GSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



detail of lead end



NOTE

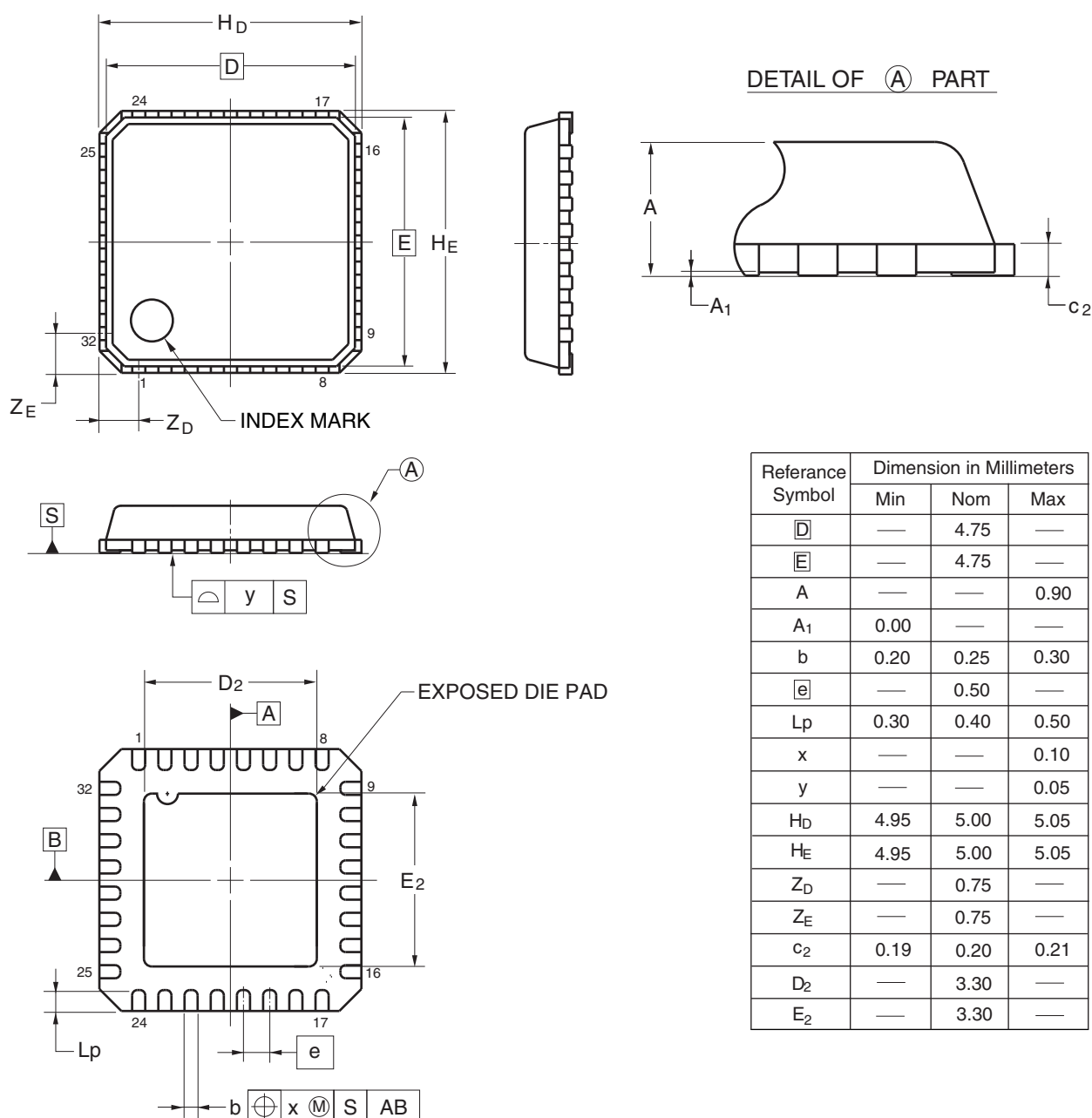
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 ^{+0.08} _{-0.07}
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25
U	0.6±0.15

3.4 32-pin products

R5F117BCGNA, R5F117BAGNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HVQFN32-5x5-0.50	PVQN0032KE-A	P32K9-50B-BAH	0.058



REVISION HISTORY	RL78/I1D Datasheet
------------------	--------------------

Rev.	Date	Description	
		Page	Summary
1.00	Aug 29, 2014	—	First Edition issued
2.00	Jan 16, 2015	24, 25, 27	Addition of note 7 in 2.3.2 Supply current characteristics
		24, 26	Addition of description in 2.3.2 Supply current characteristics
		26, 28	Modification of description in 2.3.2 Supply current characteristics
		28	Correction of error in 2.3.2 Supply current characteristics
		95	Modification of package drawing in 3.2 24-pin products
2.20	Feb 20, 2017	ALL	The function name changed from real-time clock to real-time clock 2
		5	Addition of product name in 1.3.1 20-pin products
		6	Addition of product name in 1.3.2 24-pin products
		7	Addition of product name in 1.3.3 30-pin products
		8	Addition of product name in 1.3.4 32-pin products
		9	Change of description and addition of product name in 1.3.4 32-pin products
		10	Addition of product name in 1.3.5 48-pin products
		13, 14	Change of description in 1.6 Outline of Functions
		16	Change of 2.1 Absolute Maximum Ratings
		22	Change of 2.3.1 Pin characteristics
		24	Change of conditions in 2.3.2 Supply current characteristics
		25, 27, 28	Change of note 1 in 2.3.2 Supply current characteristics
		26	Change of conditions and unit in 2.3.2 Supply current characteristics
		30	Change of note 3 in 2.3.2 Supply current characteristics
		31	Addition of note 5 in 2.3.2 Supply current characteristics
		92	Change of table in 2.8 Flash Memory Programming Characteristics
		92	Addition of note 4 in 2.8 Flash Memory Programming Characteristics
		99	Change of package drawing in 3.5 48-pin products

SuperFlash is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

All trademarks and registered trademarks are the property of their respective owners.