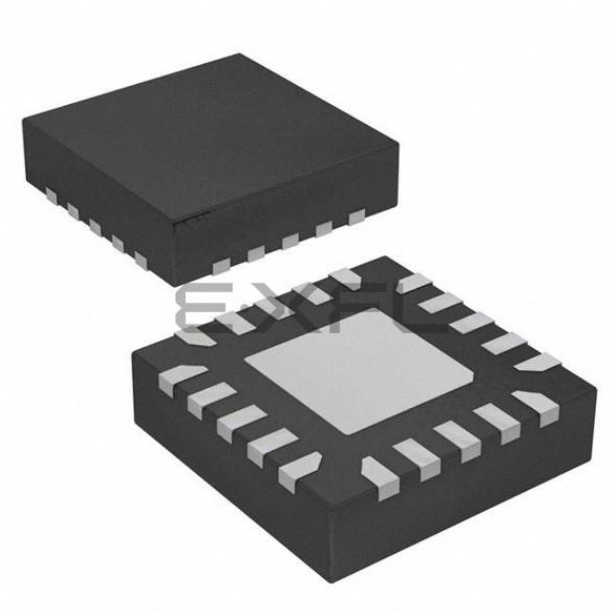

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | AVR |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 18 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 20x10b; D/A 3x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-VFQFN Exposed Pad |
| Supplier Device Package | 20-VQFN (3x3) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/attiny1616-mfr |

#### 6.10.4.3 Oscillator Configuration

**Name:** OSCCFG
**Offset:** 0x02
**Reset:** -
**Property:** -

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | OSCLOCK | | | | | | FREQSEL[1:0] | |
| Access | R | | | | | | R | R |
| Reset | 0 | | | | | | 1 | 0 |

**Bit 7 – OSCLOCK** Oscillator Lock
This fuse bit is loaded to LOCK in CLKCTRL.OSC20MCALIBB during Reset.

| Value | Description |
|---|---|
| 0 | Calibration registers of the 20 MHz oscillator are accessible |
| 1 | Calibration registers of the 20 MHz oscillator are locked |

**Bits 1:0 – FREQSEL[1:0]** Frequency Select
These bits select the operation frequency of the 16/20 MHz internal oscillator (OSC20M) and determine the respective factory calibration values to be written to CAL20M in CLKCTRL.OSC20MCALIBA and TEMPCAL20M in CLKCTRL.OSC20MCALIBB.

| Value | Description |
|---|---|
| 0x1 | Run at 16 MHz with corresponding factory calibration |
| 0x2 | Run at 20 MHz with corresponding factory calibration |
| Other | Reserved |

### 6.10.4.5 System Configuration 0

**Name:** SYSCFG0
**Offset:** 0x05
**Reset:** -
**Property:** -

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CRCBOOTDIS | CRCAPPDIS | RESERVED | TOUTDIS | RSTPINCFG[1:0] | | RESERVED | EESAVE |
| Access | R | R | R | R | R | R | R | R |
| Reset | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

**Bit 7 – CRCBOOTDIS** CRC of Boot Section in Reset Disable
See CRC description for more information about the functionality.

| Value | Description |
|---|---|
| 0 | Boot section undergoing a CRC before Reset releases |
| 1 | No CRC of the boot section before Reset releases |

**Bit 6 – CRCAPPDIS** CRC of Application Code Section in Reset Disable
See CRC description for more information about the functionality.

| Value | Description |
|---|---|
| 0 | Application code section undergoing a CRC before Reset releases |
| 1 | No CRC of the application code section before Reset releases |

**Bit 5 – RESERVED**

**Bit 4 – TOUTDIS** Time Out Disable
This bit can disable the blocking of NVM writes after POR
The NVM write block is only there the first 16ms -31ms after POR if the PDI/RST/GPIO pin (PA0) is fused to be GPIO or reset. The user should check the NVM busy status or the ready flag before the page buffer can be filled or NVM commands can be issued.

The PA0 output enable a block the first 16ms-31ms after POR if the PDI/RST/GPIO pin (PA0) is fused to be GPIO. This should be added to the documentation at a suitable place.

**Bits 3:2 – RSTPINCFG[1:0]** Reset Pin Configuration
These bits select the Reset/UPDI pin configuration.

| Value | Description |
|---|---|
| 0x0 | GPIO |
| 0x1 | UPDI |
| 0x2 | RESET |
| 0x3 | reserved |

**Bit 1 – RESERVED**

**Bit 0 – EESAVE** EEPROM Save during chip erase
**Note:** If the device is locked the EEPROM is always erased by a chip erase, regardless of this bit.

### 10.5.2 Main Clock Control B

**Name:** MCLKCTRLB
**Offset:** 0x01
**Reset:** 0x11
**Property:** Configuration Change Protection

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | PDIV[3:0] | | | | PEN |
| Access | | | | R/W | R/W | R/W | R/W | R/W |
| Reset | | | | 1 | 0 | 0 | 0 | 1 |

**Bits 4:1 – PDIV[3:0]** Prescaler Division
If the Prescaler Enable (PEN) bit is written to ‘1’, these bits define the division ratio of the main clock prescaler.

These bits can be written during run-time to vary the clock frequency of the system to suit the application requirements.

The user software must ensure a correct configuration of input frequency (CLK_MAIN) and prescaler settings, such that the resulting frequency of CLK_PER never exceeds the allowed maximum (see Electrical Characteristics).

| Value | Description |
|---|---|
| Value | Division |
| 0x0 | 2 |
| 0x1 | 4 |
| 0x2 | 8 |
| 0x3 | 16 |
| 0x4 | 32 |
| 0x5 | 64 |
| 0x8 | 6 |
| 0x9 | 10 |
| 0xA | 12 |
| 0xB | 24 |
| 0xC | 48 |
| other | Reserved |

**Bit 0 – PEN** Prescaler Enable
This bit must be written '1' to enable the prescaler. When enabled, the division ratio is selected by the PDIV bit field.

When this bit is written to '0', the main clock will pass through undivided (CLK_PER=CLK_MAIN), regardless of the value of PDIV.

# 17. BOD - Brown-out Detector

## 17.1 Features

- Brown-out Detection monitors the power supply to avoid operation below a programmable level
- There are three modes:
  - Enabled
  - Sampled
  - Disabled
- Separate selection of mode for Active and Sleep modes
- Voltage Level Monitor (VLM) with Interrupt
- Programmable VLM Level Relative to the BOD Level

## 17.2 Overview

The Brown-out Detector (BOD) peripheral monitors the power supply and compares the voltage with two programmable threshold levels: The brown-out threshold level defines when to generate a Reset. A Voltage Level Monitor (VLM) monitors the power supply and compares it to a threshold higher than the BOD threshold. The VLM can then generate an interrupt request as an "early warning" when the supply voltage is about to drop below the VLM threshold. The VLM threshold level is expressed as a percentage above the BOD threshold level.

The BOD is mainly controlled by fuses. The mode used in Standby Sleep mode and Power-Down Sleep mode can be altered in normal program execution. The VLM part of the BOD is controlled by I/O registers as well.

When activated, the BOD can operate in Enabled mode, where the BOD is continuously active, and in Sampled mode, where the BOD is activated briefly at a given period to check the supply voltage level.

### 17.5.2 Control B

**Name:** CTRLB
**Offset:** 0x01
**Reset:** Loaded from fuse
**Property:** -

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | LVL[2:0] | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | x | x | x |

**Bits 2:0 – LVL[2:0]** BOD Level
These bits select the BOD threshold level.

The Reset value is loaded from the BOD Level bits (LVL) in the BOD Configuration Fuse (FUSE.BODCFG).

| Value | Name | Description |
|---|---|---|
| 0x0 | BODLEVEL0 | 1.8V |
| 0x1 | BODLEVEL1 | 2.15V |
| 0x2 | BODLEVEL2 | 2.60V |
| 0x3 | BODLEVEL3 | 2.95V |
| 0x4 | BODLEVEL4 | 3.30V |
| 0x5 | BODLEVEL5 | 3.70V |
| 0x6 | BODLEVEL6 | 4.00V |
| 0x7 | BODLEVEL7 | 4.30V |

### 20.5.6 Control Register E Set - Normal Mode

**Name:** CTRLESET
**Offset:** 0x05
**Reset:** 0x00
**Property:** -

The individual Status bit can be set by writing a '1' to its bit location. This allows each bit to be set without the use of a read-modify-write operation on a single register.
Each Status bit can be read out either by reading TCAn.CTRLESET or TCAn.CTRLECLR.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | CMD[1:0] | | LUPD | DIR |
| Access | | | | | R/W | R/W | R/W | R/W |
| Reset | | | | | 0 | 0 | 0 | 0 |

**Bits 3:2 – CMD[1:0]** Command
These bits are used for software control of update, restart, and reset the timer/counter. The command bits are always read as '0'.

| Value | Name | Description |
|---|---|---|
| 0x0 | NONE | No command |
| 0x1 | UPDATE | Force update |
| 0x2 | RESTART | Force restart |
| 0x3 | RESET | Force hard Reset (ignored if TC is enabled) |

**Bit 1 – LUPD** Lock Update
Locking the update ensures that all buffers are valid before an update is performed.

| Value | Description |
|---|---|
| 0 | The buffered registers are updated as soon as an UPDATE condition has occurred. |
| 1 | No update of the buffered registers is performed, even though an UPDATE condition has occurred. |

**Bit 0 – DIR** Counter Direction
Normally this bit is controlled in hardware by the Waveform Generation mode or by event actions, but this bit can also be changed from software.

| Value | Description |
|---|---|
| 0 | The counter is counting up (incrementing) |
| 1 | The counter is counting down (decrementing) |

### 20.5.7 Control Register F Clear

**Name:** CTRLFCLR
**Offset:** 0x06
**Reset:** 0x00
**Property:** -

The individual Status bit can be cleared by writing a '1' to its bit location. This allows each bit to be cleared without the use of a read-modify-write operation on a single register.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | CMP2BV | CMP1BV | CMP0BV | PERBV |
| Access | | | | | R/W | R/W | R/W | R/W |
| Reset | | | | | 0 | 0 | 0 | 0 |

**Bit 3 – CMP2BV** Compare 2 Buffer Valid
See CMP0BV.

**Bit 2 – CMP1BV** Compare 1 Buffer Valid
See CMP0BV.

**Bit 1 – CMP0BV** Compare 0 Buffer Valid
The CMPnBV bits are set when a new value is written to the corresponding TCAn.CMPnBUF register. These bits are automatically cleared on an UPDATE condition.

**Bit 0 – PERBV** Period Buffer Valid
This bit is set when a new value is written to the TCAn.PERBUF register. This bit is automatically cleared on an UPDATE condition.

### 20.5.9 Event Control

**Name:** EVCTRL
**Offset:** 0x09
**Reset:** 0x00
**Property:** -

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | EVACT[1:0] | | CNTEI |
| Access | | | | | | R/W | R/W | R/W |
| Reset | | | | | | 0 | 0 | 0 |

**Bits 2:1 – EVACT[1:0]** Event Action
These bits define what type of event action the counter will increment or decrement.

| Value | Name | Description |
|---|---|---|
| 0x0 | EVACT_POSEDGE | Count on positive edge event |
| 0x1 | EVACT_ANYEDGE | Count on any edge event |
| 0x2 | EVACT_HIGHLVL | Count on prescaled clock while event line is 1. |
| 0x3 | EVACT_UPDOWN | Count on prescaled clock. The Event controls the count direction. Up-counting when the event line is 0, down-counting when the event line is 1. |

**Bit 0 – CNTEI** Enable Count on Event Input

| Value | Description |
|---|---|
| 0 | Counting on Event input is disabled |
| 1 | Counting on Event input is enabled according to EVACT bit field |

### 20.5.15 Period Register - Normal Mode

**Name:** PER
**Offset:** 0x26
**Reset:** 0xFFFF
**Property:** -

TCAn.PER contains the 16-bit TOP value in the timer/counter.

The TCAn.PERL and TCAn.PERH register pair represents the 16-bit value, TCAn.PER. The low byte [7:0] (suffix L) is accessible at the original offset. The high byte [15:8] (suffix H) can be accessed at offset + 0x01.

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | PER[15:8] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | PER[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Bits 15:8 – PER[15:8]** Periodic High Byte
These bits hold the MSB of the 16-bit period register.

**Bits 7:0 – PER[7:0]** Periodic Low Byte
These bits hold the LSB of the 16-bit period register.

### 20.5.18 Compare n Buffer Register

**Name:** CMPBUF
**Offset:** 0x38 + n*0x02 [n=0..2]
**Reset:** 0x00
**Property:** -

This register serves as the buffer for the associated compare registers (TCAn.CMPn). Accessing any of these registers using the CPU or UPDI will affect the corresponding CMPnBV status bit.

The TCAn.CMPnBUFL and TCAn.CMPnBUFH register pair represents the 16-bit value, TCAn.CMPnBUF. The low byte [7:0] (suffix L) is accessible at the original offset. The high byte [15:8] (suffix H) can be accessed at offset + 0x01.

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | CMPBUF[15:8] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CMPBUF[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 15:8 – CMPBUF[15:8]** Compare High Byte
These bits hold the MSB of the 16-bit compare buffer register.

**Bits 7:0 – CMPBUF[7:0]** Compare Low Byte
These bits hold the LSB of the 16-bit compare buffer register.

### 21.5.7 Debug Control

**Name:** DBGCTRL
**Offset:** 0x08
**Reset:** 0x00
**Property:** -

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DBGRUN |
| Access | | | | | | | | R/W |
| Reset | | | | | | | | 0 |

**Bit 0 – DBGRUN** Debug Run

| Value | Description |
|---|---|
| 0 | The peripheral is halted in Break Debug mode and ignores events |
| 1 | The peripheral will continue to run in Break Debug mode when the CPU is halted |

### 22.3.3 Events

The TCD can generate the following output events:

- TCD counter matches CMPBCLR
- TCD counter matches CMPASET
- TCD counter matches CMPBSET
- Programmable TCD output event. The user can select the trigger and all the different compare matches. In addition, it is possible to delay the output event from 0 to 256 TCD delay cycles.

The three events based on the counter match directly generate event strobes that last one clock cycle on the TCD counter clock. The programmable output event generates an event strobe that last one clock cycle on the TCD synchronizer clock.

The TCD has the possibility to receive these input events:

- Input A
- Input B

**Related Links**

22.3.2.4 TCD Inputs
14. EVSYS - Event System

#### 22.3.3.1 Programmable Output Events

Programmable output event uses the same logic as the input blanking for trigger selection and delay. It is therefore not possible to configure the functionalities independently. If the input blanking functionality is used, the output event cannot be delayed and the trigger used for input blanking will also be used for the output event.

The programmable output events are controlled by the TCDn.DLYCTRL and TCDn.DLYVAL registers. It is possible to delay the output event by 0 to 256 TCD delay clock cycles if the DLYTRIG bits in TCDn.DLYCTRL is set to 0x2. The delayed output event functionality uses the TCD delay clock and counts until the DLYVAL value is reached before the trigger is sent out as an event. The TCD delay clock is a prescaled version of the TCD synchronization clock and the division factor is set by the DLYPRESC bits in the TCDn.DLYCTRL register. The output event will be delayed by TCD clock period x DLYPRESC division factor x DLYVAL.

### 22.3.4 Interrupts

**Table 22-8. Available Interrupt Vectors and Sources**

| Offset | Name | Vector Description | Conditions |
|---|---|---|---|
| 0x00 | OVF | Overflow interrupt | The TCD is done with one TCD cycle. |
| 0x02 | TRIG | Trigger interrupt | • TRIGA: Counter is entering On-Time A<br>• TRIGB: Counter is entering On-Time B |

When an interrupt condition occurs, the corresponding interrupt flag is set in the Interrupt Flags register of the peripheral (*peripheral*.INTFLAGS).

An interrupt source is enabled or disabled by writing to the corresponding enable bit in the peripheral's Interrupt Control register (*peripheral*.INTCTRL).

### 24.5.7 Control B

**Name:** CTRLB
**Offset:** 0x06
**Reset:** 0x00
**Property:** -

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | RXEN | TXEN | | SFDEN | ODME | RXMODE[1:0] | | MPCM |
| Access | R/W | R/W | | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | | 0 | 0 | 0 | 0 | 0 |

**Bit 7 – RXEN** Receiver Enable
Writing this bit to ‘1’ enables the USART receiver. The receiver will override normal port operation for the RxD pin when enabled. Disabling the receiver will flush the receive buffer invalidating the FERR, BUFOVF, and PERR flags. In GENAUTO and LINAUTO mode, disabling the receiver will reset the auto-baud detection logic.

**Bit 6 – TXEN** Transmitter Enable
Writing this bit to ‘1’ enables the USART transmitter. The transmitter will override normal port operation for the TxD pin when enabled. Disabling the transmitter (writing TXEN to '0') will not become effective until ongoing and pending transmissions are completed (i.e. when the Transmit Shift register and Transmit Buffer register does not contain data to be transmitted). When the transmitter is disabled, it will no longer override the TxDn pin, and the pin direction is set as input automatically by hardware, even if it was configured as output by the user.

**Bit 4 – SFDEN** Start Frame Detection Enable
Writing this bit to ‘1’ enables the USART Start Frame Detection mode. The Start Frame detector is able to wake up the system from Idle or Standby Sleep modes when a high (IDLE) to low (START) transition is detected on the RxD line.

**Bit 3 – ODME** Open Drain Mode Enable
Writing this bit to ‘1’ makes the TxD pin to have open-drain functionality. A pull-up resistor is needed to prevent the line from floating when a logic '1' is output to the TxD pin.

**Bits 2:1 – RXMODE[1:0]** Receiver Mode
In CLK2X mode, the divisor of the baud rate divider will be reduced from 16 to 8 effectively doubling the transfer rate for asynchronous communication modes. For synchronous operation, the CLK2X mode has no effect and RXMODE should always be written to '0'. RXMODE must be '0' when the USART Communication mode is configured to IRCOM. Setting RXMODE to GENAUTO enables generic auto-baud where the SYNC character is valid when eight low and high bits have been registered. In this mode, any SYNC character that gives a valid BAUD rate will be accepted. In LINAUTO mode the SYNC character is constrained and found valid if every two bits falls within 32 ±6 baud samples of the internal baud rate and match data value 0x55. The GENAUTO and LINAUTO mode is only supported for USART operated in Asynchronous Slave mode.

| Value | Name | Description |
|---|---|---|
| 0x0 | NORMAL | Normal USART mode, Standard Transmission Speed |
| 0x1 | CLK2X | Normal USART mode, Double Transmission Speed |

## 25.4 Register Summary - SPI

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | CTRLA | 7:0 | | DORD | MASTER | CLK2X | | PRESC[1:0] | | ENABLE |
| 0x01 | CTRLB | 7:0 | BUFEN | BUFWR | | | | SSD | MODE[1:0] | |
| 0x02 | INTCTRL | 7:0 | RXCIE | TXCIE | DREIE | SSIE | | | | IE |
| 0x03 | INTFLAGS | 7:0 | RXCIF/IF | TXCIF/ WRCOL | DREIF | SSIF | | | | BUFOVF |
| 0x04 | DATA | 7:0 | DATA[7:0] | | | | | | | |

## 25.5 Register Description

## 27.4 Register Summary - CRCSCAN

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | CTRLA | 7:0 | RESET | | | | | | NMIEN | ENABLE |
| 0x01 | CTRLB | 7:0 | | | | | | | SRC[1:0] | |
| 0x02 | STATUS | 7:0 | | | | | | | OK | BUSY |

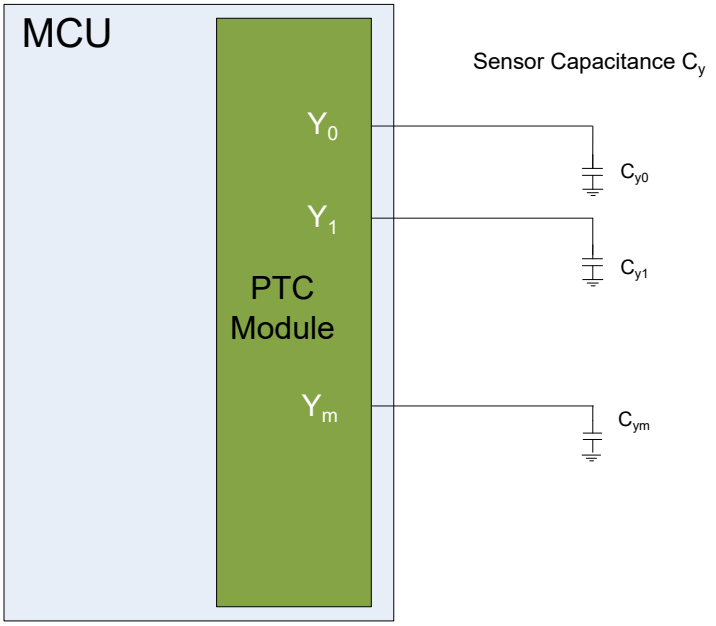
## 27.5 Register Description

## 30.4 Register Summary - ADCn

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | CTRLA | 7:0 | RUNSTBY | | | | | RESSEL | FREERUN | ENABLE |
| 0x01 | CTRLB | 7:0 | | | | | | SAMPNUM[2:0] | | |
| 0x02 | CTRLC | 7:0 | | SAMPCAP | REFSEL[1:0] | | | PRESC[2:0] | | |
| 0x03 | CTRLD | 7:0 | INITDLY[2:0] | | | ASDV | SAMPDLY[3:0] | | | |
| 0x04 | CTRLE | 7:0 | | | | | | WINCM[2:0] | | |
| 0x05 | SAMPCTRL | 7:0 | | | | SAMPLEN[4:0] | | | | |
| 0x06 | MUXPOS | 7:0 | | | | MUXPOS[4:0] | | | | |
| 0x07 | Reserved | | | | | | | | | |
| 0x08 | COMMAND | 7:0 | | | | | | | | STCONV |
| 0x09 | EVCTRL | 7:0 | | | | | | | | STARTEI |
| 0x0A | INTCTRL | 7:0 | | | | | | | WCOMP | RESRDY |
| 0x0B | INTFLAGS | 7:0 | | | | | | | WCOMP | RESRDY |
| 0x0C | DBGCTRL | 7:0 | | | | | | | | DBGRUN |
| 0x0D | TEMP | 7:0 | TEMP[7:0] | | | | | | | |
| 0x0E ... 0x0F | Reserved | | | | | | | | | |
| 0x10 | RES | 7:0 | RES[7:0] | | | | | | | |
| | | 15:8 | RES[15:8] | | | | | | | |
| 0x12 | WINLT | 7:0 | WINLT[7:0] | | | | | | | |
| | | 15:8 | WINLT[15:8] | | | | | | | |
| 0x14 | WINHT | 7:0 | WINHT[7:0] | | | | | | | |
| | | 15:8 | WINHT[15:8] | | | | | | | |
| 0x16 | CALIB | 7:0 | | | | | | | | DUTYCYC |

## 30.5 Register Description

**Figure 32-4. Self-Capacitance Sensor Arrangement**




For more information about designing the touch sensor, refer to Buttons, Sliders and Wheels Touch Sensor Design Guide.

### 32.5.2 Clocks

The PTC is clocked by the CLK_PER clock. See the Related Links for details on configuring CLK_PER.

**Related Links**

10. CLKCTRL - Clock Controller

### 32.5.3 Analog-Digital Converter (ADC)

The PTC is using the ADC for signal conversion and acquisition. The ADC must be enabled and configured appropriately to allow correct behavior of the PTC.

**Related Links**

30. ADC - Analog-to-Digital Converter

## 32.6 Functional Description

In order to access the PTC, the user must use the Atmel Start QTouch® Configurator to configure and link the QTouch Library firmware with the application software. QTouch Library can be used to implement buttons, sliders, and wheels in a variety of combinations on a single interface.

**Figure 32-5. QTouch Library Usage**

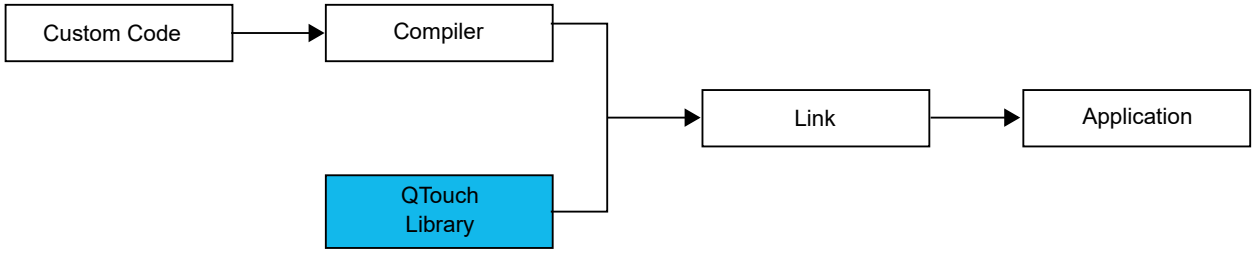
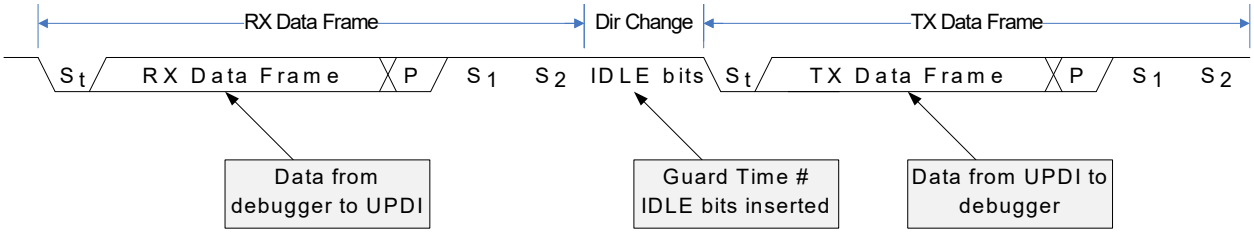


**Figure 33-7. UPDI Direction Change by Inserting IDLE Bits**

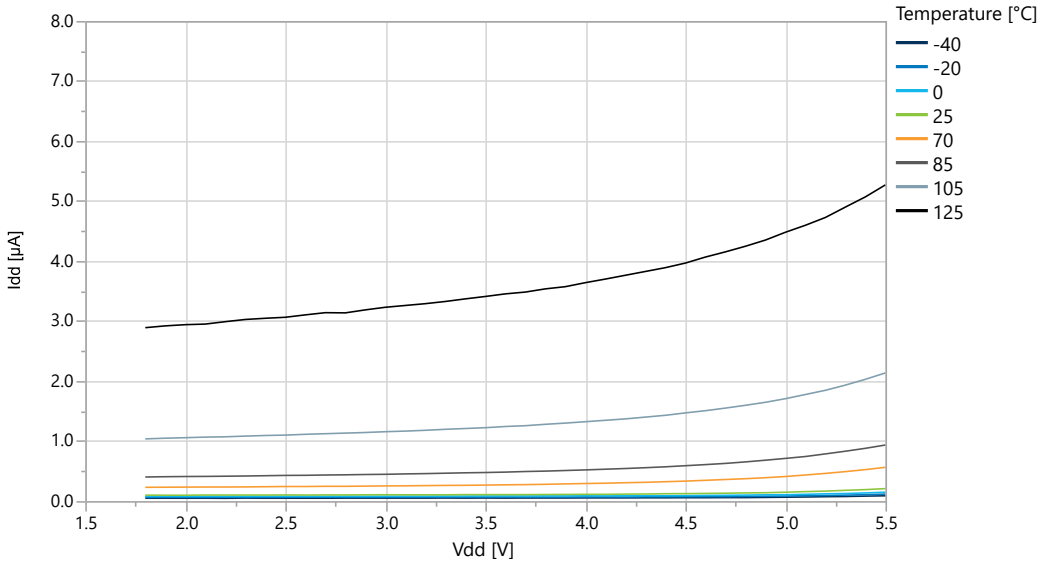



The UPDI Guard Time is the minimum IDLE time that the connected debugger will experience when waiting for data from the UPDI. Because of the asynchronous interface to the system, as presented in 33.2.2.1 Clocks, the ratio between the UPDI clock and the system clock will affect the synchronization time, and how long it takes before the UPDI can transmit data. In the cases where the synchronization delay is shorter than the current Guard Time setting, the Guard Time will be given by GTVAL directly.

### 33.3.3 UPDI Instruction Set

Communication through the UPDI is based on a small instruction set. The instructions are used to access the internal UPDI and ASI Control and Status (CS) space, as well as the memory mapped system space. All instructions are byte instructions and must be preceded by a SYNCH character to determine the baud rate for the communication. See 33.3.1.1 UPDI UART for information about setting the baud rate for the transmission. The following figure gives an overview of the UPDI instruction set.

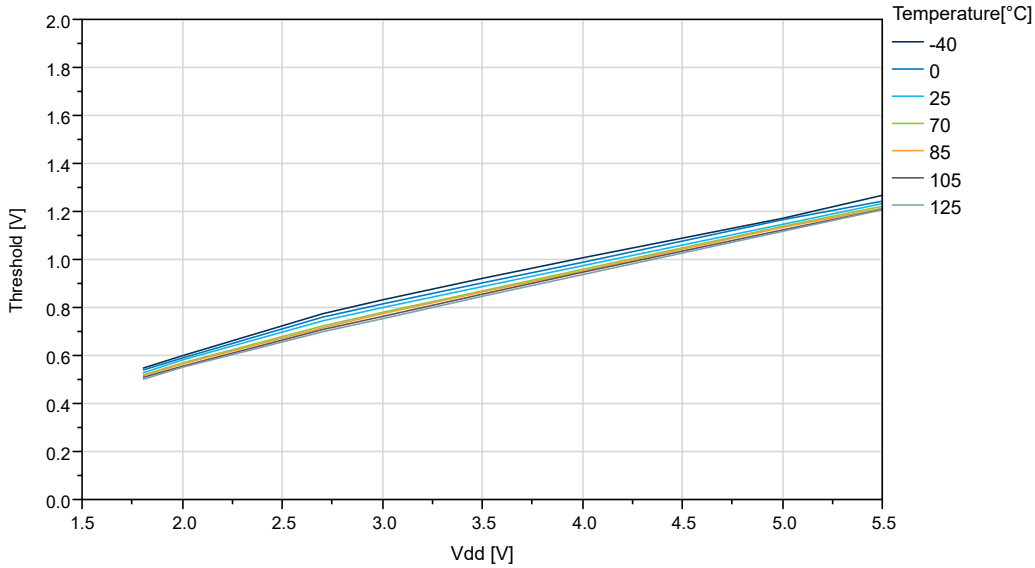
**Figure 38-29. ATtiny3216 Power-Down Mode Supply Current vs. $V_{DD}$ (all functions disabled)**




## 38.2 GPIO

### GPIO Input Characteristics

**Figure 38-30. I/O Pin Input Hysteresis vs. $V_{DD}$**



## 38.5 ADC Characteristics

**Figure 38-55. Absolute Accuracy vs. $V_{DD}$ ($f_{ADC}$=115 ksps) at T=25°C, REFSEL = Internal Reference**

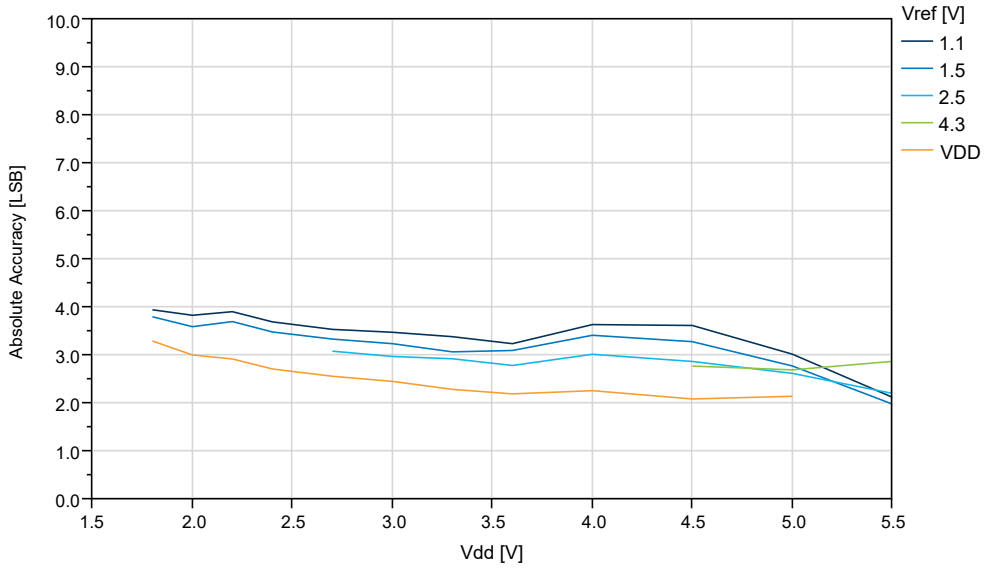



**Figure 38-56. Absolute Accuracy vs. $V_{ref}$ ($V_{DD}$=5.0V, $f_{ADC}$=115 ksps), REFSEL = Internal Reference**