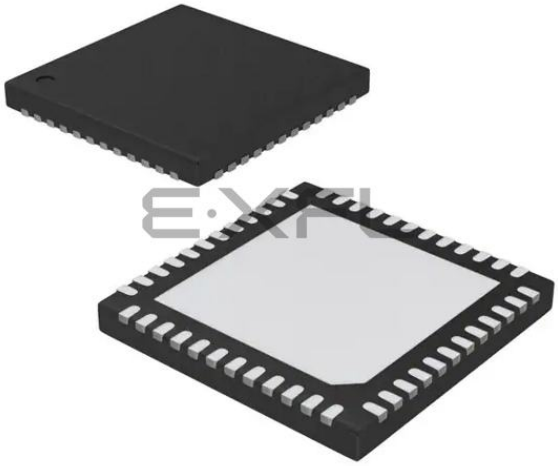
Toshiba Semiconductor and Storage - TMPM3H2FSQG,A,EL Datasheet



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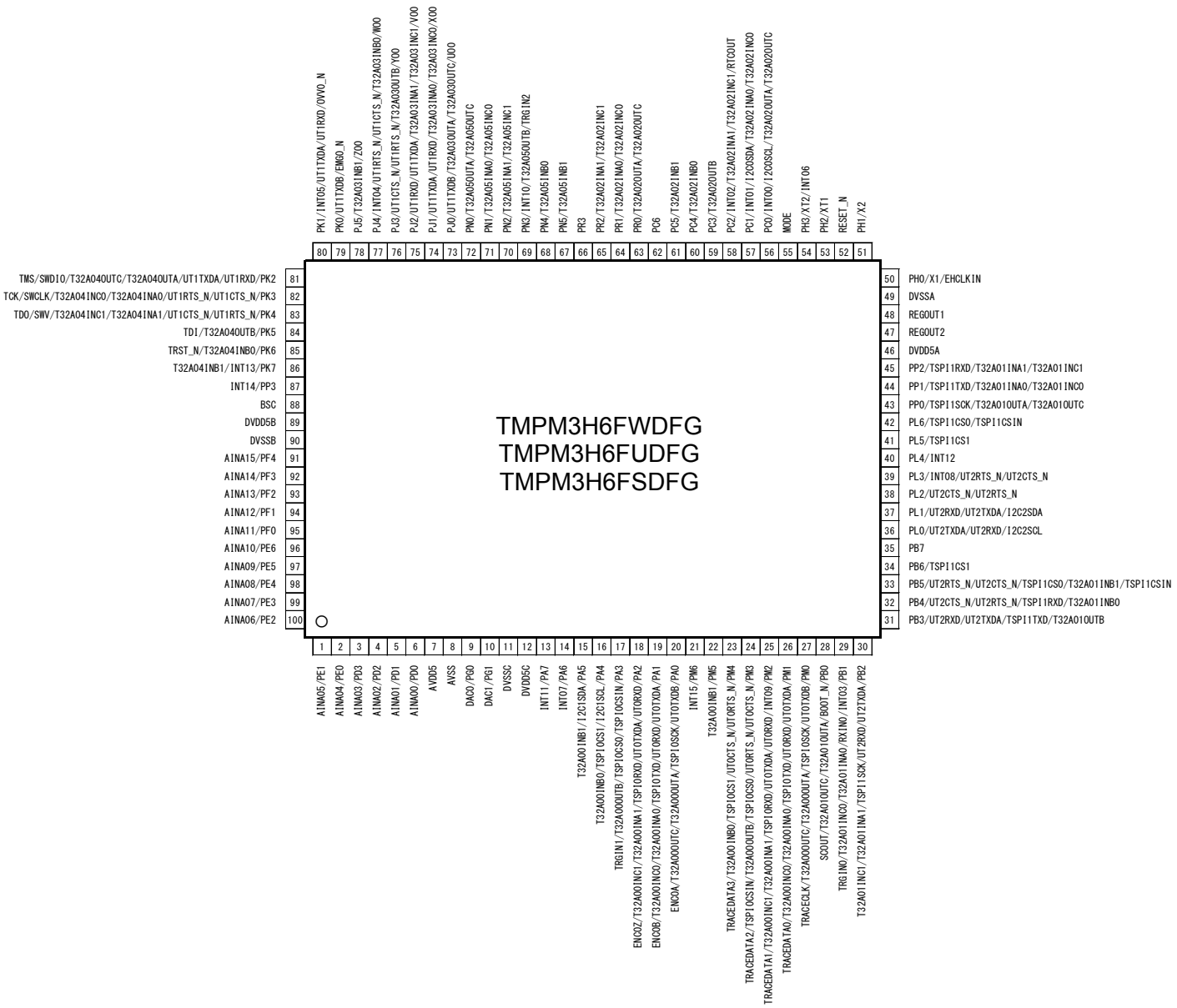
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, WDT
Number of I/O	40
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-VQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/toshiba-semiconductor-and-storage/tmpm3h2fsqg-a-el

2.2. QFP100


TMPM3H6FWDFG
TMPM3H6FUDFG
TMPM3H6FSDFG
1 AINA05/PE1
2 AINA04/PE0
3 AINA03/PD3
4 AINA02/PD2
5 AINA01/PD1
6 AINA00/PD0
7 AVDD5
8 AVSS
9 DAC0/PG0
10 DAC1/PG1
11 DVSSC
12 DVDD5C
13 INT11/PA7
14 INT07/PA6
15 T32A001NB1/I2C1SDA/PA5
16 T32A001NB0/TSPI0CS1/I2C1SCL/PA4
17 TRGIN1/T32A000UTB/TSPI0CS0/TSPI0CSIN/PA3
18 ENC0Z/T32A001INC1/T32A001NA1/TSPI0RXD/UT0TXDA/UT0RXD/PA2
19 ENC0B/T32A001INC0/T32A001NA0/TSPI0TXD/UT0RXD/UT0TXDA/PA1
20 ENC0A/T32A000UTC/T32A000UTA/TSPI0SCK/UT0TXDB/PA0
21 INT15/PN6
22 T32A001NB1/PN5
23 TRACEDATA3/T32A001NB0/TSPI0CS1/UT0CTS_N/UT0RTS_N/PN4
24 TRACEDATA2/TSPI0CSIN/T32A000UTB/TSPI0CS0/UT0RTS_N/UT0CTS_N/PN3
25 TRACEDATA1/T32A001INC1/T32A001NA1/TSPI0RXD/UT0TXDA/UT0RXD/INT09/PN2
26 TRACEDATA0/T32A001INC0/T32A001NA0/TSPI0TXD/UT0RXD/UT0TXDA/PN1
27 TRACECLK/T32A000UTC/T32A000UTA/TSPI0SCK/UT0TXDB/PN0
28 SCOUT/T32A010UTC/T32A010UTA/BOOT_N/PB0
29 TRGIN0/T32A011INC0/T32A011NA0/RXIN0/INT03/PB1
30 T32A011INC1/T32A011NA1/TSPI1SCK/UT2RXD/UT2TXDA/PB2
31 PB3/UT2RXD/UT2TXDA/TSPI1TXD/T32A010UTB
32 PB4/UT2CTS_N/UT2RTS_N/TSPI1RXD/T32A011NB0
33 PB5/UT2RTS_N/UT2CTS_N/TSPI1CS0/T32A011NB1/TSPI1CSIN
34 PB6/TSPI1CS1
35 PB7
36 PL0/UT2TXDA/UT2RXD/I2C2SCL
37 PL1/UT2RXD/UT2TXDA/I2C2SDA
38 PL2/UT2CTS_N/UT2RTS_N
39 PL3/INT08/UT2RTS_N/UT2CTS_N
40 PL4/INT12
41 PL5/TSPI1CS1
42 PL6/TSPI1CS0/TSPI1CSIN
43 PP0/TSPI1SCK/T32A010UTA/T32A010UTC
44 PP1/TSPI1TXD/T32A011NA0/T32A011INC0
45 PP2/TSPI1RXD/T32A011NA1/T32A011INC1
46 DVDD5A
47 REGOUT2
48 REGOUT1
49 DVSSA
50 PH0/X1/EHCLKIN
51 PH1/X2
52 RESET_N
53 PH2/XT1
54 PH3/XT2/INT06
55 MODE
56 PC0/INT00/I2C0SCL/T32A020UTA/T32A020UTC
57 PC1/INT01/I2C0SDA/T32A021NA0/T32A021INC0
58 PC2/INT02/T32A021NA1/T32A021INC1/RTCOUT
59 PC3/T32A020UTB
60 PC4/T32A021NB0
61 PC5/T32A021NB1
62 PG6
63 PR0/T32A020UTA/T32A020UTC
64 PR1/T32A021NA0/T32A021INC0
65 PR2/T32A021NA1/T32A021INC1
66 PR3
67 PN5/T32A051NB1
68 PN4/T32A051NB0
69 PN3/INT10/T32A050UTB/TRGIN2
70 PN2/T32A051NA1/T32A051INC1
71 PN1/T32A051NA0/T32A051INC0
72 PN0/T32A050UTA/T32A050UTC
73 PJ0/UT1TXDB/T32A030UTA/T32A030UTC/U00
74 PJ1/UT1TXDA/UT1RXD/T32A031NA0/T32A031INC0/X00
75 PJ2/UT1RXD/UT1TXDA/T32A031NA1/T32A031INC1/Y00
76 PJ3/UT1CTS_N/UT1RTS_N/T32A030UTB/Y00
77 PJ4/INT04/UT1RTS_N/UT1CTS_N/T32A031NB0/W00
78 PJ5/T32A031NB1/Z00
79 PK0/UT1TXDB/EMG0_N
80 PK1/INT05/UT1TXDA/UT1RXD/OVV0_N
81 TMS/SWDIO/T32A040UTC/T32A040UTA/UT1TXDA/UT1RXD/PK2
82 TCK/SWCLK/T32A041INC0/T32A041NA0/UT1RTS_N/UT1CTS_N/PK3
83 TDO/SWV/T32A041INC1/T32A041NA1/UT1CTS_N/UT1RTS_N/PK4
84 TDI/T32A040UTB/PK5
85 TRST_N/T32A041NB0/PK6
86 T32A041NB1/INT13/PK7
87 INT14/PP3
88 BSC
89 DVDD5B
90 DVSSB
91 AINA15/PF4
92 AINA14/PF3
93 AINA13/PF2
94 AINA12/PF1
95 AINA11/PF0
96 AINA10/PE6
97 AINA09/PE5
98 AINA08/PE4
99 AINA07/PE3
100 AINA06/PE2

3. Memory Map

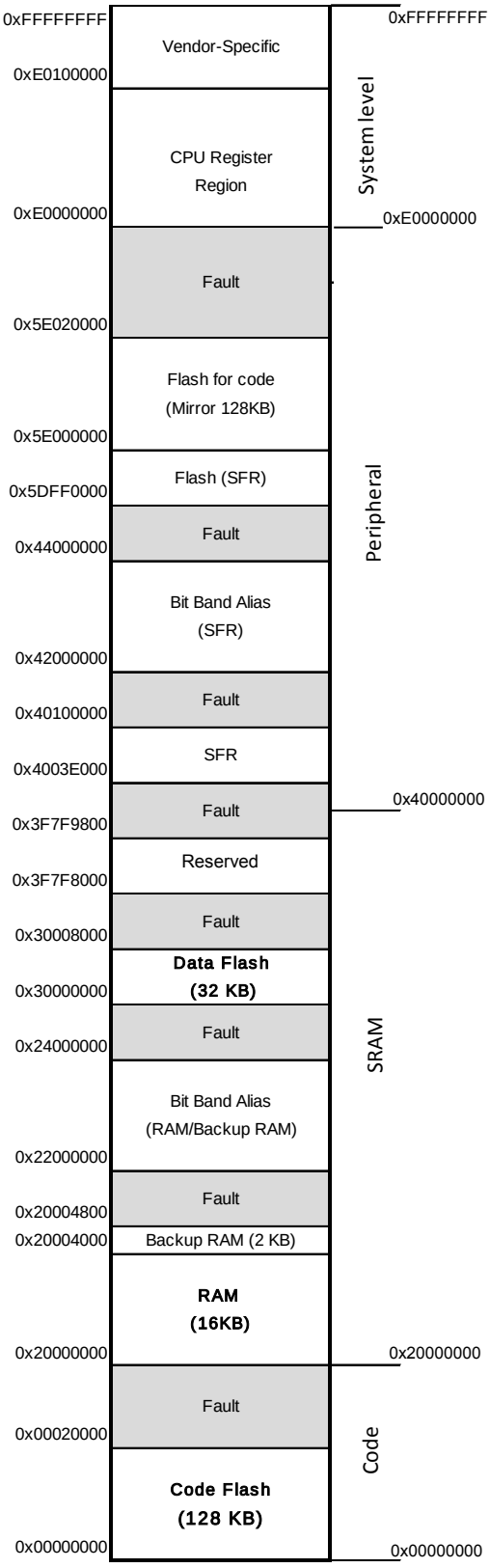


Figure 3.1 Example of the TMPM3H6FW

Table 4.14 PMD+, A-ENC

Combination functional pin name	Port Name	M3H6 (LQFP100)	M3H6 (QFP100)	M3H5 (LQFP80)	M3H4 (LQFP64)	M3H3 (LQFP52)	M3H2 (LQFP48) (VQFN48)	M3H1 (LQFP44)	M3H0 (LQFP32)
EMG0_N	PK0	77	79	62	50	41	38	34	27
OVV0_N	PK1	78	80	63	51	42	39	35	28
UO0	PJ0	71	73	56	44	35	32	28	21
VO0	PJ2	73	75	58	46	37	34	30	23
WO0	PJ4	75	77	60	48	39	36	32	25
XO0	PJ1	72	74	57	45	36	33	29	22
YO0	PJ3	74	76	59	47	38	35	31	24
ZO0	PJ5	76	78	61	49	40	37	33	26
Combination functional pin name	**Port Name**	**M3H6 (LQFP100)**	**M3H6 (QFP100)**	**M3H5 (LQFP80)**	**M3H4 (LQFP64)**	**M3H3 (LQFP52)**	**M3H2 (LQFP48) (VQFN48)**	**M3H1 (LQFP44)**	**M3H0 (LQFP32)**
ENC0A	PA0	18	20	17	13	13	12	11	7
ENC0B	PA1	17	19	16	12	12	11	10	6
ENC0Z	PA2	16	18	15	11	11	10	9	5

Table 4.21 Port names, and specifications of Port G, J, K, L, M

Port Name	Input/Output	PU/PD	OD	5V_T	SMT/ CMOS	Under Reset	After Reset
PG0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PH0	Input	PD	N/A	N/A	SMT	Hi-z	Hi-z
PH1	Input	PD	N/A	N/A	SMT	Hi-z	Hi-z
PH2	Input	PD	N/A	N/A	SMT	Hi-z	Hi-z
PH3	Input	PD	N/A	N/A	SMT	Hi-z	Hi-z
PJ0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK2	I/O	PU/PD	YES	N/A	SMT	PU(Note)	PU(Note)
PK3	I/O	PU/PD	YES	N/A	SMT	PD(Note)	PD(Note)
PK4	I/O	PU/PD	YES	N/A	SMT	Hi-z (Note)	Hi-z(Note)
PK5	I/O	PU/PD	YES	N/A	SMT	PU(Note)	PU(Note)
PK6	I/O	PU/PD	YES	N/A	SMT	PU(Note)	PU(Note)
PK7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL0	I/O	PU/PD	YES	YES	SMT	Hi-z	Hi-z
PL1	I/O	PU/PD	YES	YES	SMT	Hi-z	Hi-z
PL2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z

Note: It is assigned to a debugging pin in the state of the initial stage. (PK2:TMS/SWDIO, PK3:TCK/SWCLK, PK4:TDO/SWV, PK5:TDI, PK6:TRST_N)

5.2. Processor Core

The TMPM3H Group(1) incorporates a high-performance 32-bit processor core (Arm Cortex-M3 core).
For the operation of the processor core, refer to the Arm documentation set of the Arm "Cortex-M" series processor. This section explains the product-specific information.

5.2.1. Core Information

The Cortex-M3 core revision used in the TMPM3H Group(1) is shown as below:
For details of the CPU core and the architecture, refer to the documentation of the Arm in the following URL:
http: //infocenter.arm.com/help/index.jsp

Table 5.2 Core revision

Group name	Core revision
TMPM3H Group(1)	r2p1

5.2.2. Configurable Options

In the Cortex-M3 core, some blocks can be selected to implement. The following table shows the configurations of the TMPM3H Group(1).

Table 5.3 Configurable options and their implementations

Configurable option	Implementation
FWB	Literal comparator: 2 Instruction comparator: 6
DWT	Comparator: 4
ITM	Available
MPU	Available
ETM	Available
AHB-AP	Available
AHB trace macro cell interface	Not available
TPIU	Available
WIC	Not available
Debug port	JTAG/serial wire
Bit band	Available
Sequential control of AHB	Not available

5.3. Clock Control and Operation mode (CG)

The CG selects a clock gear ratio and the prescaler clock, or warm up time of the oscillator.
There are NORMAL mode and low-power consumption mode as operation modes. Power consumption can be decreased by mode transition.

The outline of the clock control circuit is as follows:

- Internal high-speed oscillation circuit: 10MHz
- Selectable from the external high-speed oscillation circuit or internal high-speed oscillation circuit.
- PLL (Clock Multiplication Circuit): Capable of 40 MHz output by changing the multiplication ratio according to the frequency of the high-speed oscillation circuit
- Clock gear: The high-speed clock can be divided by 1/1, 1/2, 1/4, 1/8, or 1/16 and the clock is used as the system clock (fsys).
- Low-power consumption mode:

  IDLE: Only the CPU is stopped in this mode. Each peripheral circuit can enabling or disabling operation in the IDLE mode.

  STOP1: Except some peripheral circuits, all the internal circuits including the internal oscillator are brought to a stop in STOP1 mode. External low frequency oscillator can oscillate. RTC and RMC can be used.

  STOP2: This mode halts voltage supply, retaining some peripheral circuits operation. External low frequency oscillator can oscillate (RTC can be used.), and wake-up by I^2C slave address matching.

5.4. Flash Memory (Code FLASH, Data FLASH)

The cord flash stores instruction code, and CPU reads instruction code and executes. The data flash stores data, and even if a power supply is off, data can be kept.

It has the dual mode that possible to write and erase a data flash while executing an order by a code flash, and it's also possible to continue executing an application program during writing or erasing data flash.

It has protection function which prohibits write or erase by the block unit and it has the security function which prohibits the reading of the program code by the 3rd person.

5.5. Oscillation Circuit

External High Speed Oscillator (EHOSC): Connect crystal resonator or ceramic resonator to terminals. Use clock source for System clock.

External Low Speed Oscillator (ELOSC): Connect crystal resonator (32.768 kHz) to terminals. Use clock source for Real Time Clock or Power consumption mode.

Internal High Speed Oscillator 1(IHOSC1): Oscillation frequency is 10MHz. Use clock source for System clock.

Internal High Speed Oscillator 2(IHOSC2): Oscillation frequency is 10MHz. Use clock source for OFD and SIWDT.

Table 5.4 Built-in Oscillator

	M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
EHOSC	✓	✓	✓	✓	✓	✓	✓
ELOSC	✓	✓	✓	✓	✓	-	-
IHOSC1	✓	✓	✓	✓	✓	✓	✓
IHOSC2	✓	✓	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.6. Trimming Circuit (TRM)

The trimming function can adjust frequency of the internal high-speed oscillator 1 (IHOSC1).
In the coarse trimming, -20.4% to +33.0% adjustment by 0.8%-step is feasible. In the delicate trimming,-0.8% to +0.7% adjustment by 0.1%-step is feasible.

Table 5.5 Built-in TRM

	M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
TRM	✓	✓	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

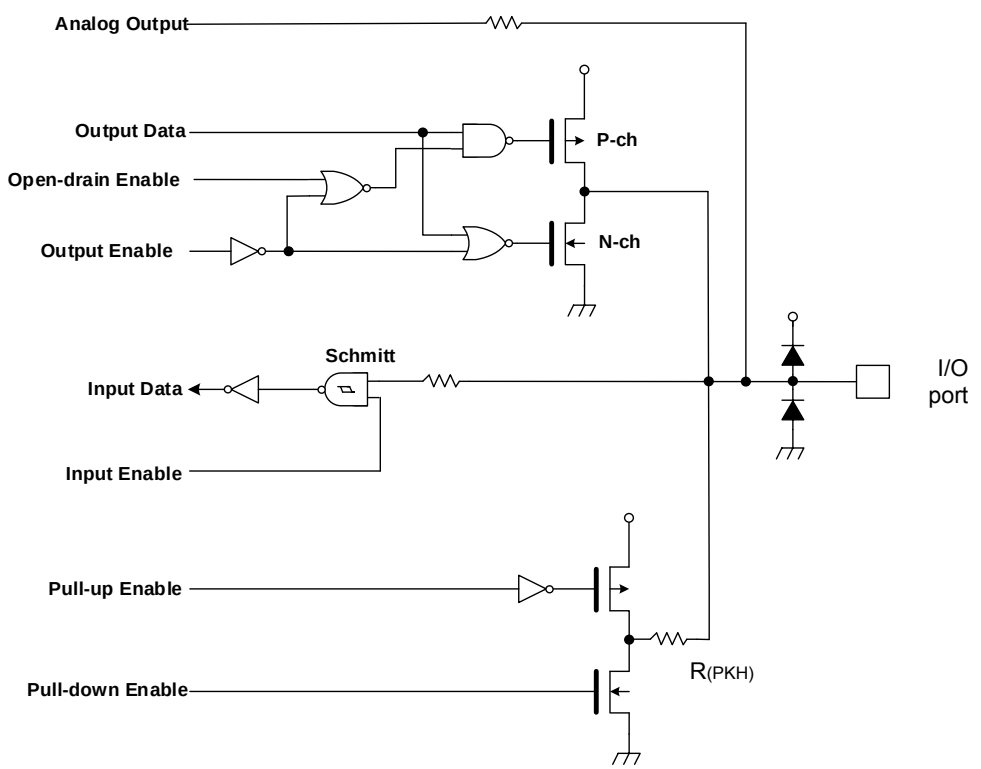
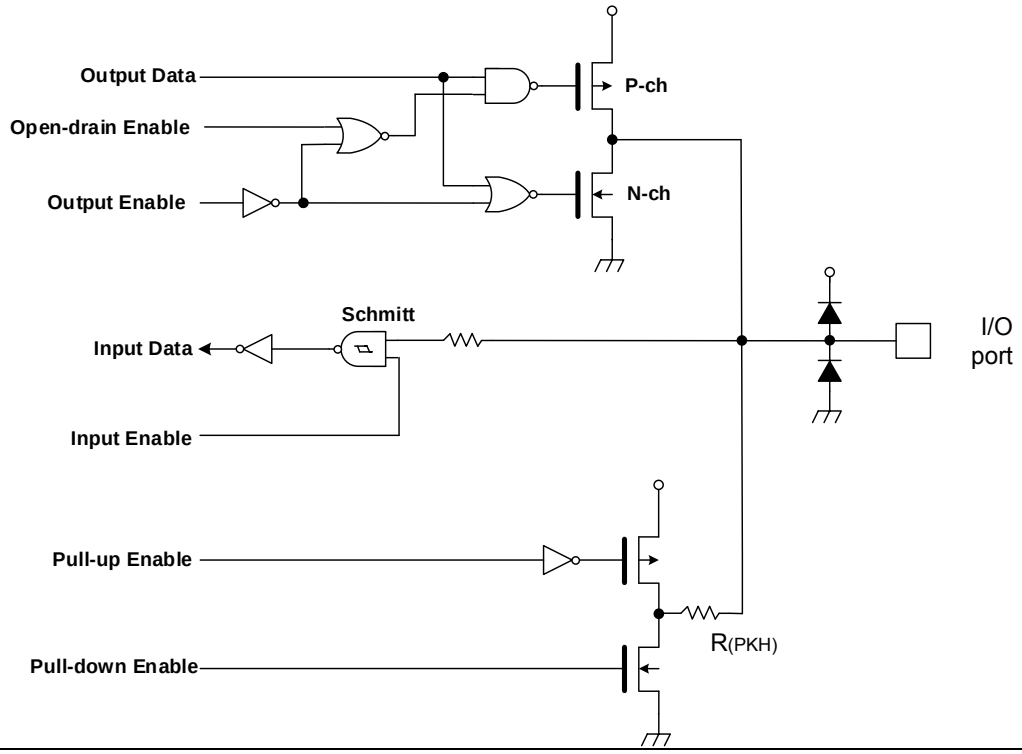
5.7. Oscillation Frequency Detection Circuit (OFD)

The oscillation frequency detection circuit (OFD) is a function that detects an abnormal state of the clock. It measures the external high-speed oscillation (f_{EHOSC}) or high-speed clock (fc) based on the internal reference clock (f_{IHOSC2}). If an oscillation or clock frequency is out of the specified range, a reset signal occurs.
The upper limit and the lower limit of detection frequency ranges can be specified respectively.

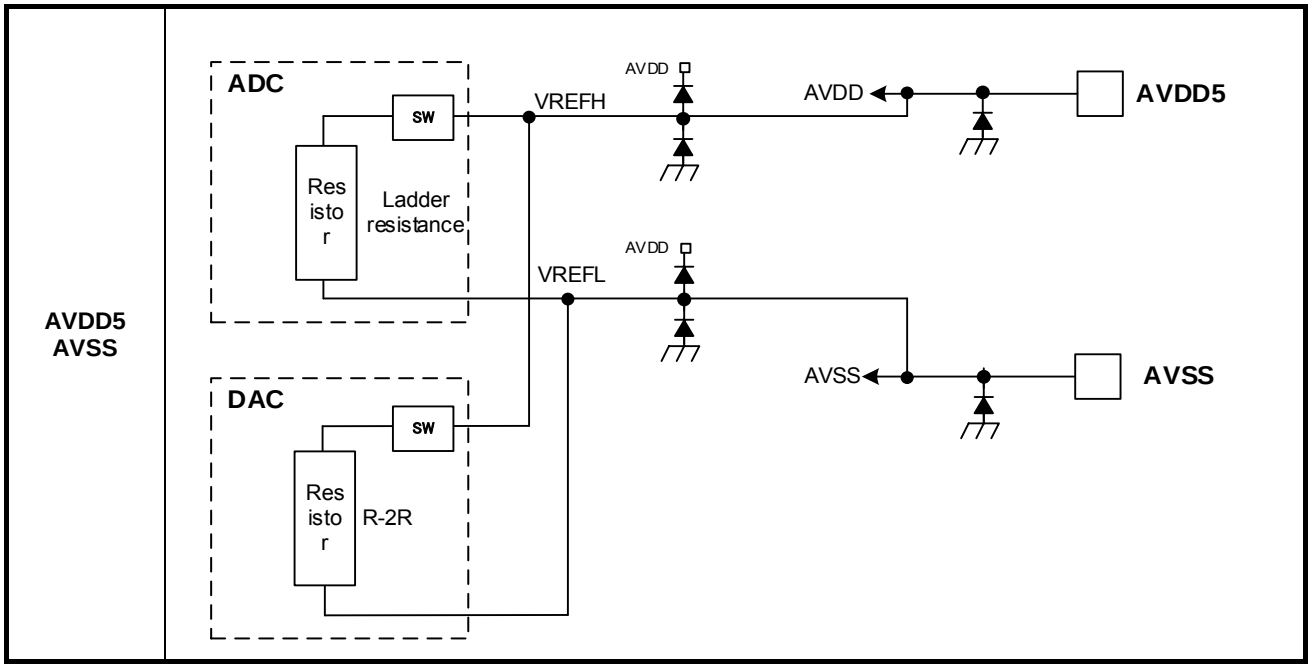
Table 5.6 Built-in OFD

	M3H6	M3H5	M3H4	M3H3	M3H2	M3H1	M3H0
OFD	✓	✓	✓	✓	✓	✓	✓

Note: ✓: Available, -: N/A

PG0 to PG1	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input, Analog Output) 
PA0 to PA3 PB2 to PB7 PC3 to PC6 PJ0 to PJ3, PJ5, PK0, PK2 to PK6 PL2, PL5, PL6 PM0, PM1, PM3 to PM5 PN0 to PN2, PN4 ,PN5 PP0 to PP2 PR0 to PR3	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input) 

6.2. Analog Power pin



Note: SW: ON/OFF Switch Circuit

7.3. DC Electrical Characteristics (2/2)

Ta =-40 to 85°C

Parameter	Symbol	Conditions				Min	Typ. (Note2)	Max	Unit
		Supply voltage	High-speed oscillator	Low-speed oscillator	Operating condition				
Normal	I_{DD}	DVDD5= AVDD5= 5.5V	Refer to the table 7.2 and 7.3 for detai			-	9.5	12.5	mA
IDLE			Oscillation	Oscillation	CPU only	-	1.2	3.7	
STOP1			Stop	Oscillation	Refer to the table 7.2 and 7.3 for detail	-	140	1900	μA
STOP2						-	13	100	
				Stop		-	12	100	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

Note2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5.0V, unless otherwise noted.

Note3: Apply same voltage to DVDD5 and AVDD5.

Note4: Input pin is fixed level, Output pin is open.

Table 7.2 IDD measurement condition (Pin setting, Oscillation Circuit)

		NORMAL	IDLE	STOP1	STOP2	
				LOSC run		LOSC stop
Pin setting	DVDD5= AVDD5=	5.0V(Typ.), 5.5V(max)				
	X1,X2	Oscillator connected (10MHz)				
	XT1,XT2	Oscillator connected(32.768kHz)				
	Input pins	Fixed				
	Output pins	Open				
Operation condition (Oscillation Circuit)	System clock (fsys)	40MHz		Stop		
	External High-speed frequency oscillator (EHOSC)	Oscillation		Stop		
	Internal High-speed frequency oscillator (IHOSC)	Stop				
	PLL	run(4times)		Stop		
	Low-speed oscillator (ELOSC)	Oscillation				Stop

7.5. 8-bit DA Converter Characteristics

DVDD5=AVDD5=2.7V to 5.5V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	AVDD5 (VREFH)		AVDD5-0.3	-	AVDD5+0.3	V
Integral nonlinearity error (INL)	-	4.5V ≤ AVDD5 ≤ 5.5V Rload = 10MΩ	-1	-	+1	LSB
Differential nonlinearity error (DNL)			-1	-	+1	
Total errors			-1	-	+1	
Integral nonlinearity error (INL)	-	2.7V ≤ AVDD5 < 4.5V Rload = 10MΩ	-2	-	+2	LSB
Differential nonlinearity error (DNL)			-1	-	+1	
Total errors			-2	-	+2	
Stable time	t_{sta}	Cload = 20pF	4.5	-	-	μs

Note 1; DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.
Note 2: Typ. value is in Ta = 25 °C, DVDD5 = AVDDA5 = 5V, unless otherwise noted.
Note 3: 1LSB = (AVDD5(VREFH) - AVSS(VREFL)) / 256 [V]
Note 4: This is the characteristic in case only DA converter is operating.

7.6. Characteristics of Internal processing at RESET

DVSS=AVSS=0V
Ta= -40to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Internal Initialized time	T_{IINIT}	Power-On	-	-	2.15	ms
		STOP2 Release by RESET with RESET_N	-	-	1.8	
		STOP2 Release by Interrupt	-	-	1.55	
Internal processing time for Reset	T_{IRST}		0.16	-	0.2	
Waiting time till CPU running	T_{CPUWT}	Cold Reset	12	-	15	μs
		Warm Reset	70	-	90	
Power-on rising gradient	V_{PON}		0.01	-	100	mV/μs

7.7. Characteristics of Power-on Reset

DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{PREL}	Power-up	2.25	2.4	2.55	V
	V_{PDET}	Power-down	2.2	2.35	2.5	
Detection pulse width	T_{PDET}		200	-	-	μs

7.9. AC Electrical Characteristics

7.9.1. Serial Peripheral Interface (TSPI)

7.9.1.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7V to 5.5V
- Ta = -40 to 85°C
- Output level: High = 0.8 × DVDD5, Low = 0.2 × DVDD5
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

7.9.1.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the TSPI. This operation clock has the same cycle of the system clock (fsys). This cycle depends on the clock gear setting.

The number of cycles can be 1 to 16. It is specified with TSPIxSCK. The value of k1 is specified with ***[TSPIxFMTR0]***<CSSCKDL[3:0]>; the value of k2 is specified with ***[TSPIxFMTR0]***<SCKCSDL[3:0]>. These values are 1 to 16.

(1) Master mode

4.5V ≤DVDD5=AVDD5≤ 5.5V

Parameter	Symbol	Calculation		fsys = 40MHz		Unit
		Min	Max	Min	Max	
TSPIxSCK output frequency	f_{CYC}	-	20	-	20	MHz
TSPIxSCK output cycle	t_{CYC}	50	-	50	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2) - 13	-	12	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2) - 13	-	12	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSU}	(t_{CYC} x k1) - 20	(t_{CYC} x k1) + 15	30	65	
TSPIxSCK rise/fall time → TSPIxCSn hold time	t_{CHD}	(t_{CYC} x (k2 + 0.5))-20	-	55	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	35 - T(Note)	-	10	-	
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	T (Note)	-	25	-	
TSPIxSCK rise/fall time → TSPIxTXD hold time	t_{ODLY1}	-18	-	-18	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	16	-	16	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	(t_{CYC} x (k1 - 0.5))-25	(t_{CYC} x (k1 - 0.5))+17	0	42	

Note: In this case ***[TSPIxCR]***<RXDLY>=0

7.9.3. 32-bit Timer Event Counter (T32A)

This section describes AC characteristics of T32AxINA0/A1, T32AxINB0/B1, and T32AxINC0/C1.

7.9.3.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5=AVDD5=2.7V to 5.5V
- Ta = -40 to 85°C
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

7.9.3.2. AC Characteristics

"T" in the table below indicates the operation clock cycle of the T32A. The operation clock of the T32A is the same cycle asΦT0 clock. This cycle is depending on the Prescaler Clock setting.

(1) Operation other than the pulse count

Parameter	Symbol	Calculation		fsys=40 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{VCKL}	2T + 20	-	70	-	ns
High level pulse width	t_{VCKH}	2T + 20	-	70	-	

(2) At the pulse count

Parameter	Symbol	Calculation		fsys=40 MHz In this case, NF=4		Unit
		Min	Max	Min	Max	
Pulse cycle	t_{DCYC}	1000	-	1000	-	ns
Low level pulse width	t_{PWL}	500	-	500	-	
High level pulse width	t_{PWH}	500	-	500	-	
Input setup	t_{ABS}	(NF+1)×T+20	-	145	-	
Input hold	t_{ABH}	(NF+1)×T+20	-	145	-	

NF Value is depend on the ***[T32AxPLSCR]***<NF[1:0]> setting as following.

[T32AxPLSCR]<NF[1:0]>	NF Value of Formula
00	0
01	2
10	4
11	8

7.9.9. External Clock Input

7.9.9.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD5 = AVDD5 = 2.7V to 5.5V
- Ta = -40℃～85℃
- Input level: High = 0.75 × DVDD5, Low = 0.25 × DVDD5
- Load capacity: CL = 30pF

Note: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.

7.9.9.2. AC Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
Clock frequency($1/t_{ehcin}$)	$f_{EHCLKIN}$	6	-	20	MHz
Clock duty	-	45	-	55	%
Clock rise time	t_r	-	-	10	ns
Clock fall time	t_f	-	-	10	ns

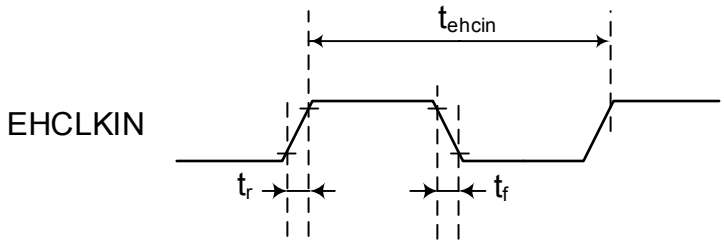


Figure 7.10 External clock input waveform

7.10. Flash Memory Characteristics

7.10.1. Code Flash

DVDD5=2.7V to 5.5V
Ta=-40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance		-	-	10,000	cycles
Programming time	Word Program time	-	29.5	-	μs
Erase time	Page Erase time	1.1	-	4.3	ms
	Block Erase time	8.6	-	34	
	Area Erase time(Note2)	-	9.2	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.
Note2: No block with effective protection.

7.10.2. Data Flash

DVDD5=2.7V to 5.5V
Ta=-40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance		-	-	100,000	cycles
Programing time		-	64.7	-	μs
Erase time	Page Erase time	1	-	3.9	ms
	Block Erase time	15.4	-	62.1	
	Area Erase time(Note2)	-	9.2	-	

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.
Note2: No block with effective protection.

7.10.3. Chip Erase

DVDD5= 2.7V to 5.5V
Ta= -40 to 85°C

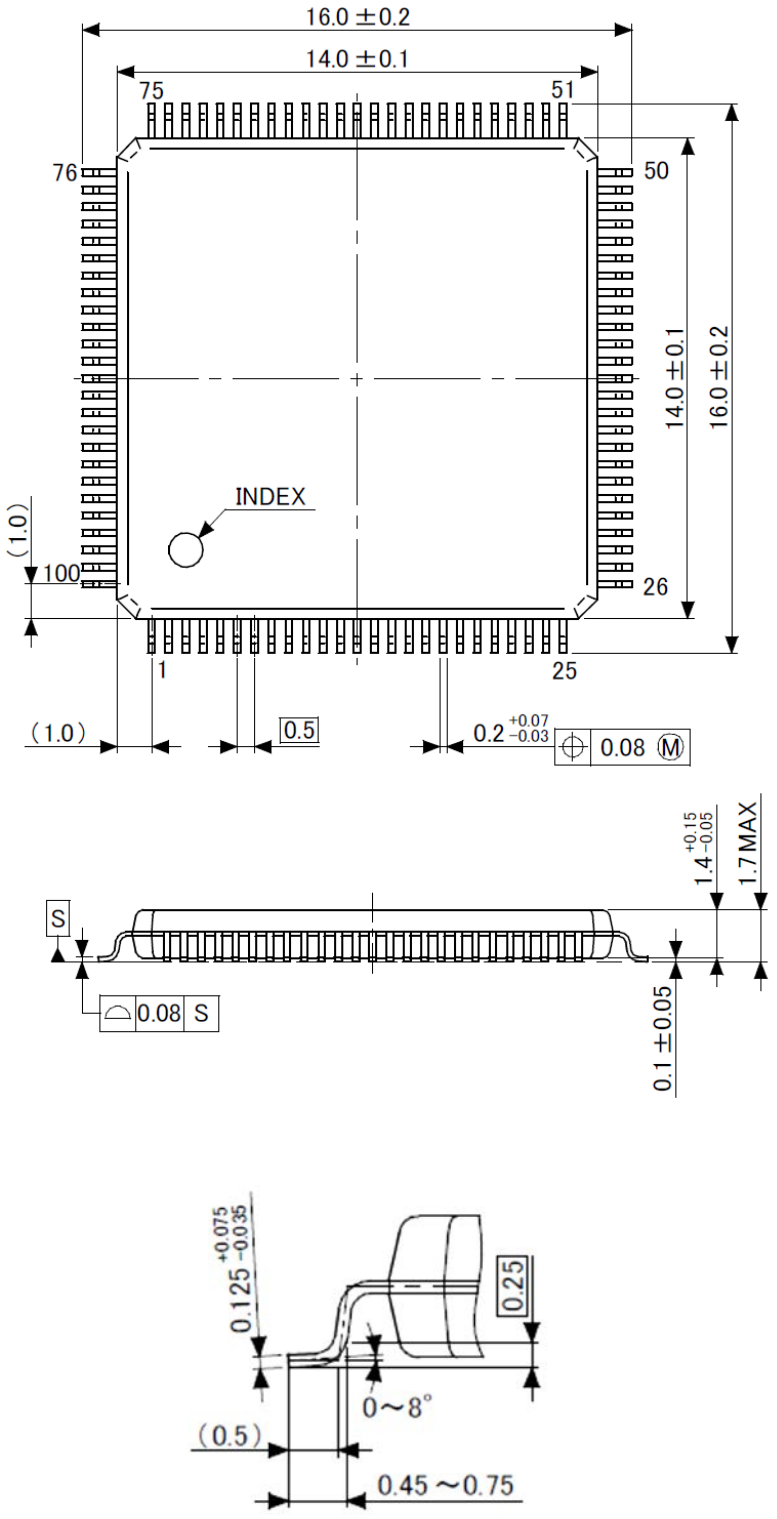
Parameter	Condition	Min	Typ.	Max	Unit
Chip Erase time	Erasing of Code Flash, Data Flash, Protect Bits(Code), Protect Bits(Data), User Information Area and Security bits	23.4	-	62.7	ms

Note1: DVDD5 is a generic name for DVDD5A, DVDD5B, and DVDD5C.
Note2: When Chip Erase command executes, no block with effective protection.

8. Package Dimensions

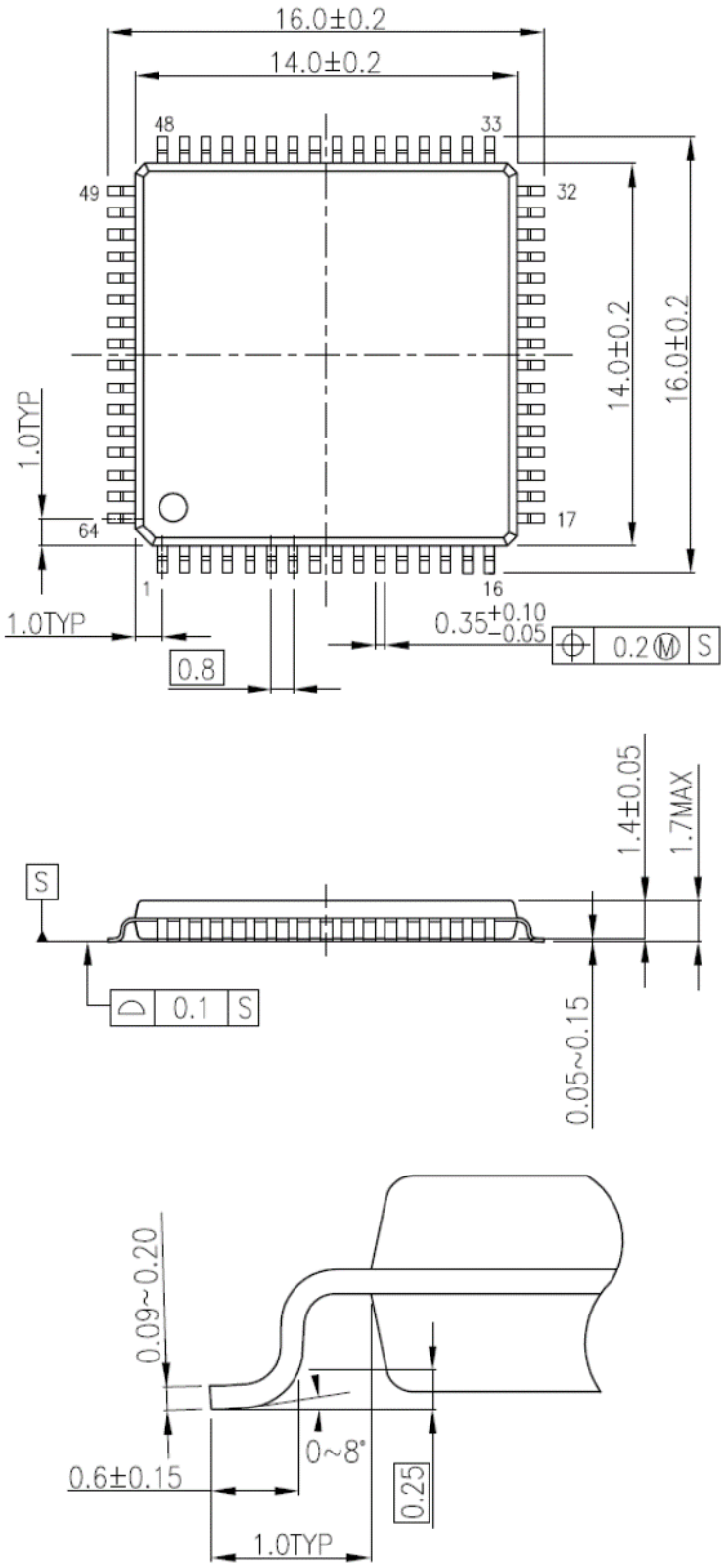
8.1. LQFP100-P-1414-0.50H

Unit: mm



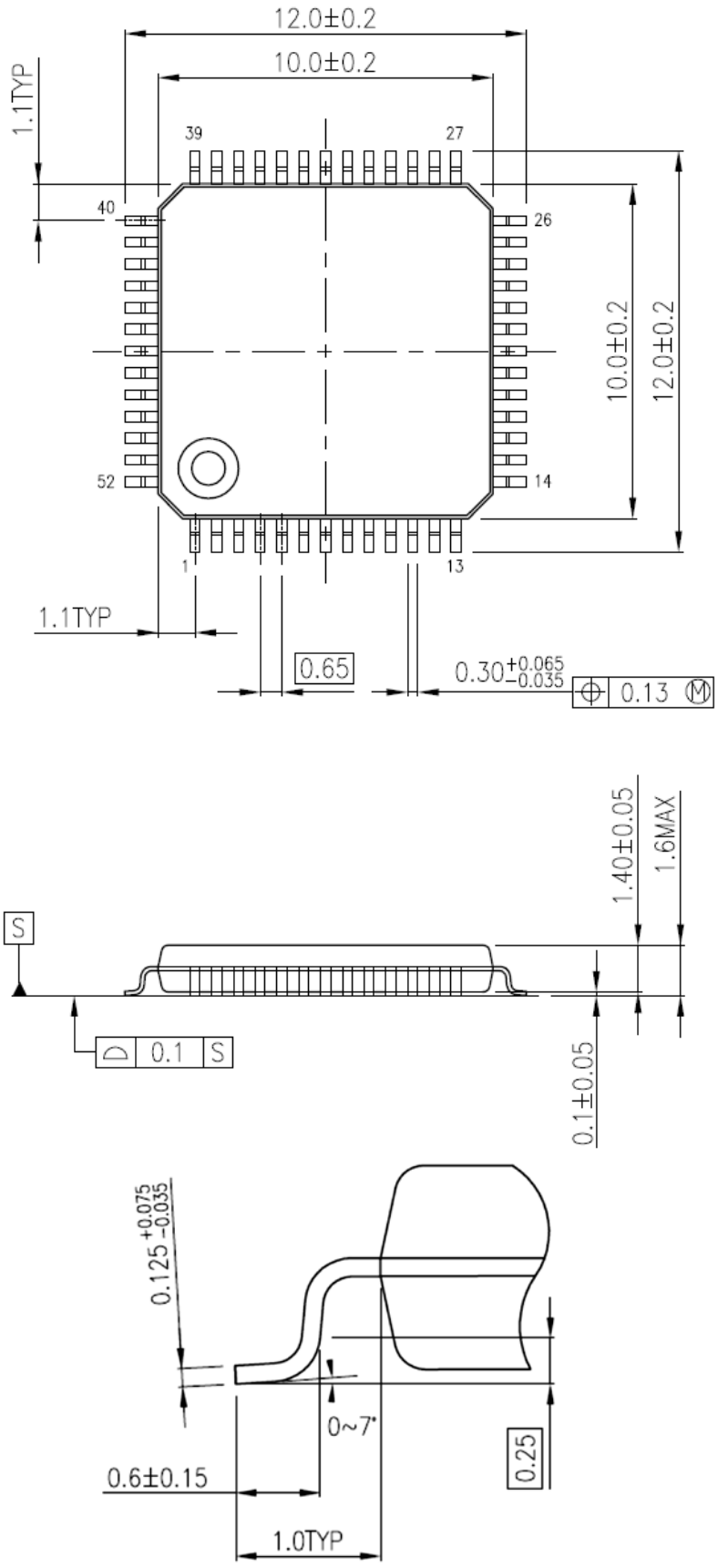
8.6. P-LQFP64-1414-0.80-002

Unit: mm



8.7. P-LQFP52-1010-0.65-001

Unit: mm



8.11. P-LQFP32-0707-0.80-002

Unit: mm