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Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	21
Program Memory Size	7.5KB (7.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc908gr8amfaer

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$0022	Timer 1 Counter Register Low (T1CNTL) See page 210.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
\$0023	Timer 1 Counter Modulo Register High (T1MODH) See page 211.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
\$0024	Timer 1 Counter Modulo Register Low (T1MODL) See page 211.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
\$0025	Timer 1 Channel 0 Status and Control Register (T1SC0) See page 214.	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
\$0026	Timer 1 Channel 0 Register High (T1CH0H) See page 214.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
\$0027	Timer 1 Channel 0 Register Low (T1CH0L) See page 214.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
\$0028	Timer 1 Channel 1 Status and Control Register (T1SC1) See page 214.	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
\$0029	Timer 1 Channel 1 Register High (T1CH1H) See page 214.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
\$002A	Timer 1 Channel 1 Register Low (T1CH1L) See page 214.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
\$002B	Timer 2 Status and Control Register (T2SC) See page 211.	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
\$002C	Timer 2 Counter Register High (T2CNTH) See page 210.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 4 of 7)

Table 2-1. Vector Addresses

Vector Priority	Vector	Address	Vector
<div> <div>Lowest</div> <div>↑</div> <div>↓</div> <div>Highest</div> </div>	IF16	\$FFDC	Timebase Vector (High)
		\$FFDD	Timebase Vector (Low)
	IF15	\$FFDE	ADC Conversion Complete Vector (High)
		\$FFDF	ADC Conversion Complete Vector (Low)
	IF14	\$FFE0	Keyboard Vector (High)
		\$FFE1	Keyboard Vector (Low)
	IF13	\$FFE2	SCI Transmit Vector (High)
		\$FFE3	SCI Transmit Vector (Low)
	IF12	\$FFE4	SCI Receive Vector (High)
		\$FFE5	SCI Receive Vector (Low)
	IF11	\$FFE6	SCI Error Vector (High)
		\$FFE7	SCI Error Vector (Low)
	IF10	\$FFE8	SPI Transmit Vector (High)
		\$FFE9	SPI Transmit Vector (Low)
	IF9	\$FFEA	SPI Receive Vector (High)
		\$FFEB	SPI Receive Vector (Low)
	IF8	\$FFEC	TIM2 Overflow Vector (High)
		\$FFED	TIM2 Overflow Vector (Low)
	IF7	\$FFEE	Reserved
		\$FFEF	Reserved
	IF6	\$FFF0	TIM2 Channel 0 Vector (High)
		\$FFF1	TIM2 Channel 0 Vector (Low)
	IF5	\$FFF2	TIM1 Overflow Vector (High)
		\$FFF3	TIM1 Overflow Vector (Low)
	IF4	\$FFF4	TIM1 Channel 1 Vector (High)
		\$FFF5	TIM1 Channel 1 Vector (Low)
	IF3	\$FFF6	TIM1 Channel 0 Vector (High)
		\$FFF7	TIM1 Channel 0 Vector (Low)
	IF2	\$FFF8	PLL Vector (High)
		\$FFF9	PLL Vector (Low)
	IF1	\$FFFA	$\overline{\text{IRQ}}$ Vector (High)
		\$FFFB	$\overline{\text{IRQ}}$ Vector (Low)
	—	\$FFFC	SWI Vector (High)
		\$FFFD	SWI Vector (Low)
	—	\$FFFE	Reset Vector (High)
		\$FFFF	Reset Vector (Low)

2.5 Random-Access Memory (RAM)

Addresses \$0040 through \$01BF are RAM locations. The location of the stack RAM is programmable. The 16-bit stack pointer allows the stack to be anywhere in the 64-Kbyte memory space.

NOTE

For correct operation, the stack pointer must point only to RAM locations.

Within page zero are 192 bytes of RAM. Because the location of the stack RAM is programmable, all page zero RAM locations can be used for I/O control and user data or code. When the stack pointer is moved from its reset location at \$00FF out of page zero, direct addressing mode instructions can efficiently access all page zero RAM locations. Page zero RAM, therefore, provides ideal locations for frequently accessed global variables.

Before processing an interrupt, the CPU uses five bytes of the stack to save the contents of the CPU registers.

NOTE

For M6805 compatibility, the H register is not stacked.

During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements during pushes and increments during pulls.

NOTE

Be careful when using nested subroutines. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation.

2.6 FLASH Memory (FLASH)

This subsection describes the operation of the embedded FLASH memory. This memory can be read, programmed, and erased from a single external supply. The program, erase, and read operations are enabled through the use of an internal charge pump.

2.6.1 Functional Description

The FLASH memory is an array of 7,680 bytes for the MC68HC908GR8A or 4,096 bytes for the MC68HC908GR4A with an additional 36 bytes of user vectors and one byte of block protection. *An erased bit reads as 1 and a programmed bit reads as a 0.* Memory in the FLASH array is organized into two rows per page basis. The page size is 64 bytes per page and the row size is 32 bytes per row. Hence the minimum erase page size is 64 bytes and the minimum program row size is 32 bytes. Program and erase operation operations are facilitated through control bits in FLASH control register (FLCR). Details for these operations appear later in this section.

The address ranges for the user memory and vectors are:

- \$E000–\$FDFF; user memory for the MC68HC908GR8A
- \$EE00–\$FDFF; user memory for the MC68HC908GR4A
- \$FE08; FLASH control register
- \$FF7E; FLASH block protect register
- \$FFDC–\$FFFF; these locations are reserved for user-defined interrupt and reset vectors

NOTE

A security feature prevents viewing of the FLASH contents.⁽¹⁾

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

2.6.2 FLASH Control Register

The FLASH control register (FLCR) controls FLASH program and erase operations.

Address: \$FE08

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
Write:								
Reset:	0	0	0	0	0	0	0	0


 = Unimplemented

Figure 2-3. FLASH Control Register (FLCR)

HVEN — High-Voltage Enable Bit

This read/write bit enables the charge pump to drive high voltages for program and erase operations in the array. HVEN can only be set if either PGM = 1 or ERASE = 1 and the proper sequence for program or erase is followed.

- 1 = High voltage enabled to array and charge pump on
- 0 = High voltage disabled to array and charge pump off

MASS — Mass Erase Control Bit

Setting this read/write bit configures the FLASH array for mass erase operation.

- 1 = MASS erase operation selected
- 0 = PAGE erase operation selected

ERASE — Erase Control Bit

This read/write bit configures the memory for erase operation. ERASE is interlocked with the PGM bit such that both bits cannot be equal to 1 or set to 1 at the same time.

- 1 = Erase operation selected
- 0 = Erase operation unselected

PGM — Program Control Bit

This read/write bit configures the memory for program operation. PGM is interlocked with the ERASE bit such that both bits cannot be equal to 1 or set to 1 at the same time.

- 1 = Program operation selected
- 0 = Program operation unselected



4.5.4 PLL Multiplier Select Register Low

The PLL multiplier select register low (PMSL) contains the programming information for the low byte of the modulo feedback divider.

Address: \$0038

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	MUL7	MUL6	MUL5	MUL4	MUL3	MUL2	MUL1	MUL0
Write:								
Reset:	0	1	0	0	0	0	0	0

Figure 4-7. PLL Multiplier Select Register Low (PMSL)

NOTE

For applications using 1–8 MHz reference frequencies, this register must be reprogrammed before enabling the PLL. The reset value of this register will cause applications using 1–8 MHz reference frequencies to become unstable if the PLL is enabled without programming an appropriate value. The programmed value must not allow the VCO clock to exceed 32 MHz. See 4.3.6 Programming the PLL for detailed instructions on choosing the proper value for PMSL.

MUL7–MUL0 — Multiplier Select Bits

These read/write bits control the low byte of the modulo feedback divider that selects the VCO frequency multiplier, N. (See 4.3.3 PLL Circuits and 4.3.6 Programming the PLL.) MUL7–MUL0 cannot be written when the PLLON bit in the PCTL is set. A value of \$0000 in the multiplier select registers configures the modulo feedback divider the same as a value of \$0001. Reset initializes the register to \$40 for a default multiply value of 64.

NOTE

The multiplier select bits have built-in protection such that they cannot be written when the PLL is on (PLLON = 1).

4.5.5 PLL VCO Range Select Register

The PLL VCO range select register (PMRS) contains the programming information required for the hardware configuration of the VCO.

Address: \$003A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	VRS7	VRS6	VRS5	VRS4	VRS3	VRS2	VRS1	VRS0
Write:								
Reset:	0	1	0	0	0	0	0	0

Figure 4-8. PLL VCO Range Select Register (PMRS)

VRS7–VRS0 — VCO Range Select Bits

These read/write bits control the hardware center-of-range linear multiplier L which, in conjunction with E (see 4.3.3 PLL Circuits, 4.3.6 Programming the PLL, and 4.5.1 PLL Control Register), controls the hardware center-of-range frequency, f_{VRS} . VRS7–VRS0 cannot be written when the PLLON bit in the PCTL is set. (See 4.3.7 Special Programming Exceptions.) A value of \$00 in the VCO range select

6.3.6 COPD (COP Disable)

The COPD signal reflects the state of the COP disable bit (COPD) in the configuration register. See Chapter 5 Configuration Register (CONFIG).

6.3.7 COPRS (COP Rate Select)

The COPRS signal reflects the state of the COP rate select bit (COPRS) in the configuration register. See Chapter 5 Configuration Register (CONFIG).

6.4 COP Control Register

The COP control register (COPCTL) is located at address \$FFFF and overlaps the reset vector. Writing any value to \$FFFF clears the COP counter and starts a new timeout period. Reading location \$FFFF returns the low byte of the reset vector.

Address: \$FFFF	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Low byte of reset vector							
Write:	Clear COP counter							
Reset:	Unaffected by reset							

Figure 6-2. COP Control Register (COPCTL)

6.5 Interrupts

The COP does not generate central processor unit (CPU) interrupt requests.

6.6 Monitor Mode

When monitor mode is entered with V_{TST} on the \overline{IRQ} pin, the COP is disabled as long as V_{TST} remains on the \overline{IRQ} pin or the \overline{RST} pin. When monitor mode is entered by having blank reset vectors and not having V_{TST} on the \overline{IRQ} pin, the COP is automatically disabled until a POR occurs.

6.7 Low-Power Modes

The WAIT and STOP instructions put the microcontroller unit (MCU) in low power-consumption standby modes.

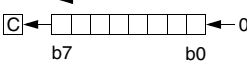
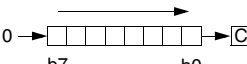
6.7.1 Wait Mode

The COP remains active during wait mode. If COP is enabled, a reset will occur at COP timeout.

6.7.2 Stop Mode

Stop mode turns off the CGMXCLK input to the COP and clears the COP prescaler. Service the COP immediately before entering or after exiting stop mode to ensure a full COP timeout period after entering or exiting stop mode.

Table 7-1. Instruction Set Summary (Sheet 4 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z				
JMP <i>opr</i> JMP <i>opr</i> JMP <i>opr</i> ,X JMP <i>opr</i> ,X JMP ,X	Jump	PC ← Jump Address	–	–	–	–	–	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff	2 3 4 3 2
JSR <i>opr</i> JSR <i>opr</i> JSR <i>opr</i> ,X JSR <i>opr</i> ,X JSR ,X	Jump to Subroutine	PC ← (PC) + <i>n</i> (<i>n</i> = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Unconditional Address	–	–	–	–	–	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff	4 5 6 5 4
LDA # <i>opr</i> LDA <i>opr</i> LDA <i>opr</i> LDA <i>opr</i> ,X LDA <i>opr</i> ,X LDA ,X LDA <i>opr</i> ,SP LDA <i>opr</i> ,SP	Load A from M	A ← (M)	0	–	–	↑	↑	IMM DIR EXT IX2 IX1 IX SP1 SP2	A6 B6 C6 D6 E6 F6 9EE6 9ED6	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
LDHX # <i>opr</i> LDHX <i>opr</i>	Load H:X from M	H:X ← (M:M + 1)	0	–	–	↑	↑	IMM DIR	45 55	ii jj dd	3 4
LDX # <i>opr</i> LDX <i>opr</i> LDX <i>opr</i> LDX <i>opr</i> ,X LDX <i>opr</i> ,X LDX ,X LDX <i>opr</i> ,SP LDX <i>opr</i> ,SP	Load X from M	X ← (M)	0	–	–	↑	↑	IMM DIR EXT IX2 IX1 IX SP1 SP2	AE BE CE DE EE FE 9EEE 9EDE	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
LSL <i>opr</i> LSLA LSLX LSL <i>opr</i> ,X LSL ,X LSL <i>opr</i> ,SP	Logical Shift Left (Same as ASL)		↑	–	–	↑	↑	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
LSR <i>opr</i> LSRA LSRX LSR <i>opr</i> ,X LSR ,X LSR <i>opr</i> ,SP	Logical Shift Right		↑	–	–	0	↑	DIR INH INH IX1 IX SP1	34 44 54 64 74 9E64	dd ff ff ff	4 1 1 4 3 5
MOV <i>opr</i> , <i>opr</i> MOV <i>opr</i> ,X+ MOV # <i>opr</i> , <i>opr</i> MOV X+, <i>opr</i>	Move	(M) _{Destination} ← (M) _{Source} H:X ← (H:X) + 1 (IX+D, DIX+)	0	–	–	↑	↑	DD DIX+ IMD IX+D	4E 5E 6E 7E	dd dd dd ii dd dd	5 4 4 4
MUL	Unsigned multiply	X:A ← (X) × (A)	–	0	–	–	–	INH	42		5
NEG <i>opr</i> NEGA NEGX NEG <i>opr</i> ,X NEG ,X NEG <i>opr</i> ,SP	Negate (Two's Complement)	M ← –(M) = \$00 – (M) A ← –(A) = \$00 – (A) X ← –(X) = \$00 – (X) M ← –(M) = \$00 – (M) M ← –(M) = \$00 – (M)	↑	–	–	↑	↑	DIR INH INH IX1 IX SP1	30 40 50 60 70 9E60	dd ff ff ff	4 1 1 4 3 5
NOP	No Operation	None	–	–	–	–	–	INH	9D		1
NSA	Nibble Swap A	A ← (A[3:0]:A[7:4])	–	–	–	–	–	INH	62		3
ORA # <i>opr</i> ORA <i>opr</i> ORA <i>opr</i> ORA <i>opr</i> ,X ORA <i>opr</i> ,X ORA ,X ORA <i>opr</i> ,SP ORA <i>opr</i> ,SP	Inclusive OR A and M	A ← (A) (M)	0	–	–	↑	↑	IMM DIR EXT IX2 IX1 IX SP1 SP2	AA BA CA DA EA FA 9EEA 9EDA	ii dd hh ll ee ff ff ff ff ee ff	2 3 4 4 3 2 4 5
PSHA	Push A onto Stack	Push (A); SP ← (SP) – 1	–	–	–	–	–	INH	87		2
PSHH	Push H onto Stack	Push (H); SP ← (SP) – 1	–	–	–	–	–	INH	8B		2
PSHX	Push X onto Stack	Push (X); SP ← (SP) – 1	–	–	–	–	–	INH	89		2

Chapter 9

Keyboard Interrupt Module (KBI)

9.1 Introduction

The keyboard interrupt module (KBI) provides four independently maskable external interrupts which are accessible via PTA0–PTA3. When a port pin is enabled for keyboard interrupt function, an internal pullup device is also enabled on the pin.

9.2 Features

Features include:

- Four keyboard interrupt pins with separate keyboard interrupt enable bits and one keyboard interrupt mask
- Hysteresis buffers
- Programmable edge-only or edge- and level- interrupt sensitivity
- Exit from low-power modes
- I/O (input/output) port bit(s) software configurable with pullup device(s) if configured as input port bit(s)

9.3 Functional Description

Writing to the KBIE3–KBIE0 bits in the keyboard interrupt enable register independently enables or disables each port A pin as a keyboard interrupt pin. Enabling a keyboard interrupt pin also enables its internal pullup device. A low level applied to an enabled keyboard interrupt pin latches a keyboard interrupt request.

A keyboard interrupt is latched when one or more keyboard pins goes low after all were high. The MODEK bit in the keyboard status and control register controls the triggering mode of the keyboard interrupt.

- If the keyboard interrupt is edge-sensitive only, a falling edge on a keyboard pin does not latch an interrupt request if another keyboard pin is already low. To prevent losing an interrupt request on one pin because another pin is still low, software can disable the latter pin while it is low.
- If the keyboard interrupt is falling edge- and low-level sensitive, an interrupt request is present as long as any keyboard interrupt pin is low and the pin is keyboard interrupt enabled.

Chapter 11

Low-Voltage Inhibit (LVI)

11.1 Introduction

This section describes the low-voltage inhibit (LVI) module, which monitors the voltage on the V_{DD} pin and can force a reset when the V_{DD} voltage falls below the LVI trip falling voltage, V_{TRIPF} .

11.2 Features

Features of the LVI module include:

- Programmable LVI reset
- Selectable LVI trip voltage
- Programmable stop mode operation

11.3 Functional Description

Figure 11-1 shows the structure of the LVI module. The LVI is enabled out of reset. The LVI module contains a bandgap reference circuit and comparator. Clearing the LVI power disable bit, $LVIPWRD$, enables the LVI to monitor V_{DD} voltage. Clearing the LVI reset disable bit, $LVIRSTD$, enables the LVI module to generate a reset when V_{DD} falls below a voltage, V_{TRIPF} . Setting the LVI enable in stop mode bit, $LVISTOP$, enables the LVI to operate in stop mode. Setting the LVI 5-V or 3-V trip point bit, $LVI5OR3$, enables the trip point voltage, V_{TRIPF} , to be configured for 5-V operation. Clearing the $LVI5OR3$ bit enables the trip point voltage, V_{TRIPF} , to be configured for 3-V operation. The actual trip points are shown in Chapter 19 Electrical Specifications.

NOTE

After a power-on reset (POR) the LVI's default mode of operation is 3 V. If a 5-V system is used, the user must set the $LVI5OR3$ bit to raise the trip point to 5-V operation. Note that this must be done after every power-on reset since the default will revert back to 3-V mode after each power-on reset. If the V_{DD} supply is below the 5-V mode trip voltage but above the 3-V mode trip voltage when POR is released, the part will operate because V_{TRIPF} defaults to 3-V mode after a POR. So, in a 5-V system care must be taken to ensure that V_{DD} is above the 5-V mode trip voltage after POR is released.

If the user requires 5-V mode and sets the $LVI5OR3$ bit after a power-on reset while the V_{DD} supply is not above the V_{TRIPR} for 5-V mode, the microcontroller unit (MCU) will immediately go into reset. The LVI in this case will hold the part in reset until either V_{DD} goes above the rising 5-V trip point, V_{TRIPR} , which will release reset or V_{DD} decreases to approximately 0 V which will re-trigger the power-on reset and reset the trip point to 3-V operation.

Low-Voltage Inhibit (LVI)

LVISTOP, LVIPWRD, LVI5OR3, and LVIRSTD are in the configuration register (CONFIG1). See Figure 5-2. Configuration Register 1 (CONFIG1) for details of the LVI's configuration bits. Once an LVI reset occurs, the MCU remains in reset until V_{DD} rises above a voltage, V_{TRIPR} , which causes the MCU to exit reset. See 14.3.2.5 Low-Voltage Inhibit (LVI) Reset for details of the interaction between the SIM and the LVI. The output of the comparator controls the state of the LVIOUT flag in the LVI status register (LVISR).

An LVI reset also drives the \overline{RST} pin low to provide low-voltage protection to external peripheral devices.

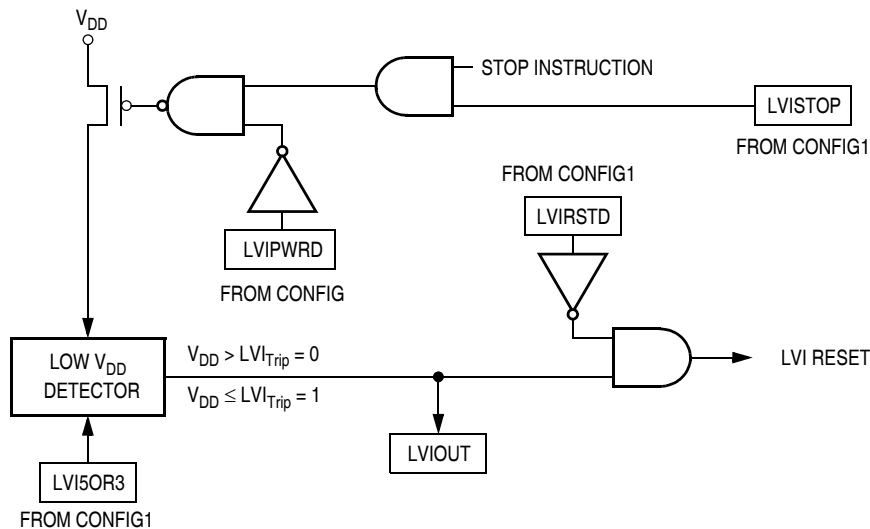


Figure 11-1. LVI Module Block Diagram

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$FE0C	LVI Status Register (LVISR) See page 113.	Read: LVIOUT	0	0	0	0	0	0	0
		Write:							
		Reset:	0	0	0	0	0	0	0

= Unimplemented

Figure 11-2. LVI I/O Register Summary

11.3.1 Polled LVI Operation

In applications that can operate at V_{DD} levels below the V_{TRIPF} level, software can monitor V_{DD} by polling the LVIOUT bit. In the configuration register, the LVIPWRD bit must be 0 to enable the LVI module, and the LVIRSTD bit must be at 1 to disable LVI resets.

11.3.2 Forced Reset Operation

In applications that require V_{DD} to remain above the V_{TRIPF} level, enabling LVI resets allows the LVI module to reset the MCU when V_{DD} falls below the V_{TRIPF} level. In the configuration register, the LVIPWRD and LVIRSTD bits must be cleared to enable the LVI module and to enable LVI resets.

Low-Voltage Inhibit (LVI)

11.6.1 Wait Mode

If enabled, the LVI module remains active in wait mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of wait mode.

11.6.2 Stop Mode

If enabled in stop mode (LVISTOP bit in the configuration register is set), the LVI module remains active in stop mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of stop mode.

Fast Data Tolerance

Figure 13-9 shows how much a fast received character can be misaligned without causing a noise error or a framing error. The fast stop bit ends at RT10 instead of RT16 but is still there for the stop bit data samples at RT8, RT9, and RT10.

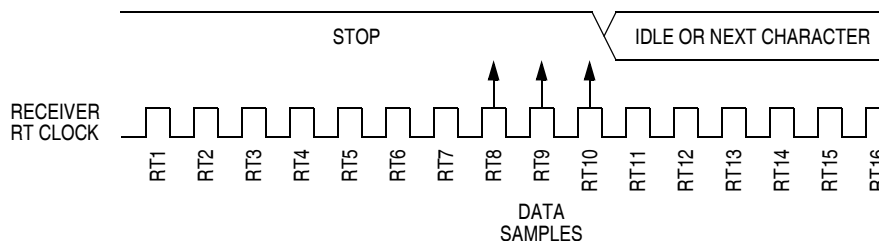


Figure 13-9. Fast Data

For an 8-bit character, data sampling of the stop bit takes the receiver 9 bit times \times 16 RT cycles + 10 RT cycles = 154 RT cycles.

With the misaligned character shown in Figure 13-9, the receiver counts 154 RT cycles at the point when the count of the transmitting device is 10 bit times \times 16 RT cycles = 160 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 8-bit character with no errors is

$$\left| \frac{154 - 160}{154} \right| \times 100 = 3.90\%$$

For a 9-bit character, data sampling of the stop bit takes the receiver 10 bit times \times 16 RT cycles + 10 RT cycles = 170 RT cycles.

With the misaligned character shown in Figure 13-9, the receiver counts 170 RT cycles at the point when the count of the transmitting device is 11 bit times \times 16 RT cycles = 176 RT cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit character with no errors is

$$\left| \frac{170 - 176}{170} \right| \times 100 = 3.53\%$$

13.4.3.6 Receiver Wakeup

So that the MCU can ignore transmissions intended only for other receivers in multiple-receiver systems, the receiver can be put into a standby state. Setting the receiver wakeup bit, RWU, in SCC2 puts the receiver into a standby state during which receiver interrupts are disabled.

Depending on the state of the WAKE bit in SCC1, either of two conditions on the PTE1/RxD pin can bring the receiver out of the standby state:

- **Address mark** — An address mark is a 1 in the most significant bit position of a received character. When the WAKE bit is set, an address mark wakes the receiver from the standby state by clearing the RWU bit. The address mark also sets the SCI receiver full bit, SCRF. Software can then compare the character containing the address mark to the user-defined address of the receiver. If they are the same, the receiver remains awake and processes the characters that follow. If they are not the same, software can set the RWU bit and put the receiver back into the standby state.

Serial Peripheral Interface (SPI) Module

In a master SPI with the mode fault enable bit (MODFEN) set, the mode fault flag (MODF) is set if \overline{SS} goes low. A mode fault in a master SPI causes the following events to occur:

- If ERRIE = 1, the SPI generates an SPI receiver/error CPU interrupt request.
- The SPE bit is cleared.
- The SPTE bit is set.
- The SPI state counter is cleared.
- The data direction register of the shared I/O port regains control of port drivers.

NOTE

To prevent bus contention with another master SPI after a mode fault error, clear all SPI bits of the data direction register of the shared I/O port before enabling the SPI.

When configured as a slave (SPMSTR = 0), the MODF flag is set if \overline{SS} goes high during a transmission. When CPHA = 0, a transmission begins when \overline{SS} goes low and ends once the incoming SPSCCK goes back to its idle level following the shift of the eighth data bit. When CPHA = 1, the transmission begins when the SPSCCK leaves its idle level and \overline{SS} is already low. The transmission continues until the SPSCCK returns to its idle level following the shift of the last data bit. See 15.4 Transmission Formats.

NOTE

Setting the MODF flag does not clear the SPMSTR bit. SPMSTR has no function when SPE = 0. Reading SPMSTR when MODF = 1 shows the difference between a MODF occurring when the SPI is a master and when it is a slave.

NOTE

When CPHA = 0, a MODF occurs if a slave is selected (\overline{SS} is low) and later unselected (\overline{SS} is high) even if no SPSCCK is sent to that slave. This happens because \overline{SS} low indicates the start of the transmission (MISO driven out with the value of MSB) for CPHA = 0. When CPHA = 1, a slave can be selected and then later unselected with no transmission occurring. Therefore, MODF does not occur since a transmission was never begun.

In a slave SPI (MSTR = 0), MODF generates an SPI receiver/error CPU interrupt request if the ERRIE bit is set. The MODF bit does not clear the SPE bit or reset the SPI in any way. Software can abort the SPI transmission by clearing the SPE bit of the slave.

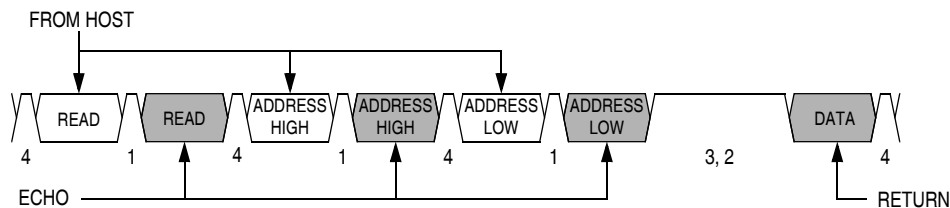
NOTE

A high on the \overline{SS} pin of a slave SPI puts the MISO pin in a high impedance state. Also, the slave SPI ignores all incoming SPSCCK clocks, even if it was already in the middle of a transmission.

To clear the MODF flag, read the SPSCR with the MODF bit set and then write to the SPCR register. This entire clearing mechanism must occur with no MODF condition existing or else the flag is not cleared.

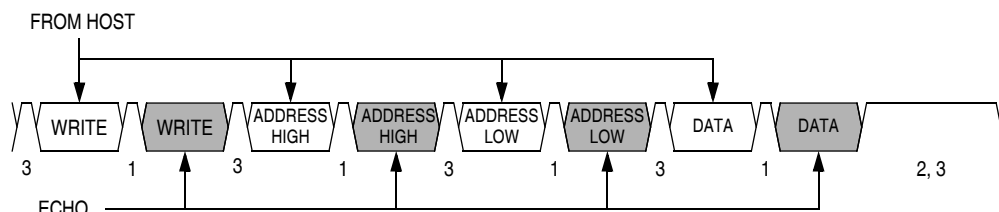
15.7 Interrupts

Four SPI status flags can be enabled to generate CPU interrupt requests. See Table 15-1.



Notes:
 1 = Echo delay, approximately 2 bit times
 2 = Data return delay, approximately 2 bit times
 3 = Cancel command delay, 11 bit times
 4 = Wait 1 bit time before sending next byte.

Figure 18-14. Read Transaction



Notes:
 1 = Echo delay, approximately 2 bit times
 2 = Cancel command delay, 11 bit times
 3 = Wait 1 bit time before sending next byte.

Figure 18-15. Write Transaction

A brief description of each monitor mode command is given in Table 18-3 through Table 18-8.

Table 18-3. READ (Read Memory) Command

Description	Read byte from memory
Operand	2-byte address in high-byte:low-byte order
Data Returned	Returns contents of specified address
Opcode	\$4A
<p style="text-align: center;">Command Sequence</p>	

19.10 Output Low-Voltage Characteristics

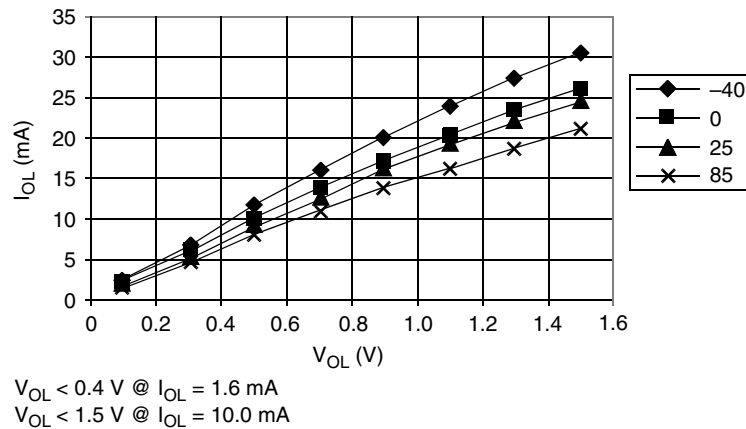


Figure 19-7. Typical Low-Side Driver Characteristics — Port PTA3–PTA0 ($V_{DD} = 5.5 \text{ Vdc}$)

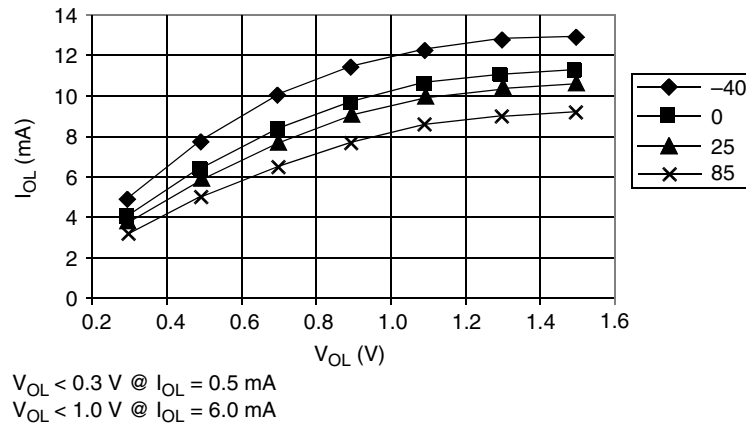


Figure 19-8. Typical Low-Side Driver Characteristics — Port PTA3–PTA0 ($V_{DD} = 2.7 \text{ Vdc}$)

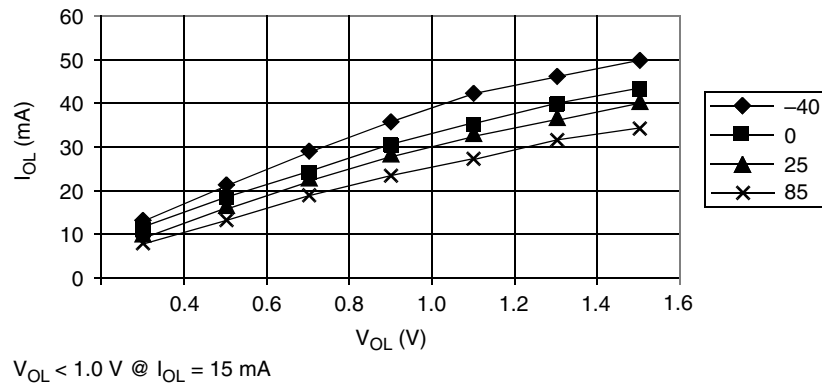


Figure 19-9. Typical Low-Side Driver Characteristics — Port PTC1–PTC0 ($V_{DD} = 4.5 \text{ Vdc}$)

19.15 Clock Generation Module Characteristics

19.15.1 CGM Component Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Crystal reference frequency ⁽¹⁾	f_{XCLK}	1	4	8	MHz
Crystal load capacitance ⁽²⁾	C_L	—	20	—	pF
Crystal fixed capacitance ⁽²⁾	C_1	—	$2 \times C_L$	—	pF
Crystal tuning capacitance ⁽²⁾	C_2	—	$2 \times C_L$	—	pF
Feedback bias resistor	R_B	0.5	1	10	M Ω
Series resistor	R_S	—	0	—	Ω

1. Fundamental mode crystals only

2. Consult crystal manufacturer's data.

19.15.2 CGM Electrical Specifications

Description	Symbol	Min	Typ	Max	Unit
Operating voltage	V_{DD}	2.7	—	5.5	V
Operating temperature	T_A	−40	25	125	°C
Crystal reference frequency	f_{RCLK}	1	4	8	MHz
Range nominal multiplier	f_{NOM}	—	38.4	—	kHz
VCO center-of-range frequency	f_{VRS}	4	—	40	MHz
VCO range linear range multiplier	L	1	—	255	
VCO power-of-two range multiplier	2^E	1	—	4	
VCO multiply factor	N	1	—	4095	
VCO prescale multiplier	2^P	1	1	8	
Reference divider factor	R	1	1	15	
VCO operating frequency	f_{VCLK}	4	—	40	MHz
Bus operating frequency (5-V operation)	f_{BUS}	—	—	8.2	MHz
Bus frequency (3-V operation)	f_{BUS}	—	—	4.1	MHz
Manual acquisition time	t_{Lock}	—	—	5	ms
Automatic lock time	t_{Lock}	—	—	5	ms
PLL jitter ⁽¹⁾	f_J	0	—	$f_{RCLK} \times 0.025\% \times 2^P N/4$	Hz
External clock input frequency PLL disabled	f_{OSC}	dc	—	32.8 M	Hz
External clock input frequency PLL enabled	f_{OSC}	1	4	8	MHz

1. Deviation of average bus frequency over 2 ms. N = VCO multiplier.