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## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Obsolete |
| Applications | Set-Top Boxes, TV |
| Core Processor | x86 |
| Program Memory Type | External Program Memory |
| Controller Series | STPC® Consumer-II |
| RAM Size | External |
| Interface | EBI/EMI, I²C, IDE, ISA, Local Bus |
| Number of I/O | - |
| Voltage - Supply | 2.45V ~ 3.6V |
| Operating Temperature | 0°C ~ 85°C |
| Mounting Type | Surface Mount |
| Package / Case | 388-BGA |
| Supplier Device Package | 388-PBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stpcc5hebc |

**Table 2-2. Definition of Signal Pins**

| Signal Name | Dir | Buffer Type[2] | Description | Qty |
|---|---|---|---|---|
| BASIC CLOCKS AND RESETS | | | | |
| SYSRSETI# | I | SCHMITT_FT | System Power Good Input | 1 |
| SYSRSTO# | O | BD8STRP_FT | System Reset Output | 1 |
| XTALI | I | ANA | 14.3 MHz Crystal Input- External Oscillator Input | 1 |
| XTALO | I/O | OSCI13B | 14.3 MHz Crystal Output | 1 |
| HCLK | I/O | BD4STRP_FT | Host Clock (Test) | 1 |
| DEV_CLK | O | BT8TRP_TC | 24 MHz Peripheral Clock (floppy drive) | 1 |
| DCLK | I/O | BD4STRP_FT | 27-135 MHz Graphics Dot Clock | 1 |
| $V_{DD}$_xxx_PLL[1] | | VDDCO | Power Supply for PLL Clocks | |
| | | | | |
| **SDRAM CONTROLLER** | | | | |
| MCLKI | I | TLCHT_TC | Memory Clock Input | 1 |
| MCLKO | O | BT8TRP_TC | Memory Clock Output | 1 |
| CS#[1:0] | O | BD8STRP_TC | DIMM Chip Select | 2 |
| CS2# / MA11 | O | BD16STARUQP_TC | DIMM Chip Select / Memory Address | 1 |
| CS3# / MA12 / BA1 | O | BD16STARUQP_TC | DIMM Chip Select / Memory Address / Bank Address | 1 |
| BA[0] | O | BD8STRP_TC | Bank Address | 1 |
| MA[10:0] | O | BD16STARUQP_TC | Memory Row & Column Address | 12 |
| MD[63:49] | I/O | BD8STRUP_FT | Memory Data | 15 |
| MD[48:1] | I/O | BD8TRP_TC | Memory Data | 48 |
| MD[0] | I/O | BD8STRUP_FT | Memory Data | 1 |
| RAS#[1:0] | O | BD16STARUQP_TC | Row Address Strobe | 2 |
| CAS#[1:0] | O | BD16STARUQP_TC | Column Address Strobe | 2 |
| MWE# | O | BD16STARUQP_TC | Write Enable | 1 |
| DQM[7:0] | O | BD8STRP_TC | Data Input/Output Mask | 8 |
| | | | | |
| **PCI CONTROLLER** | | | | |
| PCI_CLKI | I | TLCHT_FT | 33 MHz PCI Input Clock | 1 |
| PCI_CLKO | O | BT8TRP_TC | 33 MHz PCI O/P Clk (from internal PLL) | 1 |
| AD[31:0] | I/O | BD8PCIARP_FT | PCI Address / Data | 32 |
| CBE[3:0] | I/O | BD8PCIARP_FT | Bus Commands / Byte Enables | 4 |
| FRAME# | I/O | BD8PCIARP_FT | Cycle Frame | 1 |
| IRDY# | I/O | BD8PCIARP_FT | Initiator Ready | 1 |
| TRDY# | I/O | BD8PCIARP_FT | Target Ready | 1 |
| LOCK# | I | TLCHT_FT | PCI Lock | 1 |
| DEVSEL# | I/O | BD8PCIARP_FT | Device Select | 1 |
| STOP# | I/O | BD8PCIARP_FT | Stop Transaction | 1 |
| PAR | I/O | BD8PCIARP_FT | Parity Signal Transactions | 1 |
| SERR# | O | BD8PCIARP_FT | System Error | 1 |
| PCIREQ#[2:0] | I | BD8PCIARP_FT | PCI Request | 3 |
| PCIGNT#[2:0] | O | BD8PCIARP_FT | PCI Grant | 3 |
| PCI_INT#[3:0] | I | BD4STRUP_FT | PCI Interrupt Request | 4 |
| | | | | |

Note[1]: These pins are must be connected to the 2.5 V power supply. They **must not** be connected to the 3.3 V supply.
Note[2]: See Table 2-3 for buffer type descriptions

*2.2.7. VGA CONTROLLER*

**RED, GREEN, BLUE** *RGB Video Outputs.* These are the three analog colour outputs from the RAMDACs. These signals are sensitive to interference, therefore they need to be properly shielded.

**VSYNC** *Vertical Synchronisation Pulse.* This is the vertical synchronization signal from the VGA controller.

**HSYNC** *Horizontal Synchronisation Pulse.* This is the horizontal synchronization signal from the VGA controller.

**VREF_DAC** *DAC Voltage reference.* An external voltage reference is connected to this pin to bias the DAC.

**RSET** *Resistor Current Set.* This reference current input to the RAMDAC is used to set the full-scale output of the RAMDAC.

**COMP** *Compensation.* This is the RAMDAC compensation pin. Normally, an external capacitor (typically 10nF) is connected between this pin and $V_{DD}$ to damp oscillations.

*2.2.8. VIDEO INPUT PORT*

**VCLK** *Pixel Clock Input.*This signal is used to synchronise data being transferred from an external video device to either the frame buffer, or alternatively out the TV output in bypass mode. This pin can be sourced from STPC if no external VCLK is detected, or can be input from an external video clock source.

**VIN[7:0]** *YUV Video Data Input CCIR 601 or 656.* Time multiplexed 4:2:2 luminance and chrominance data as defined in ITU-R Rec601-2 and Rec656 (except for TTL input levels). This bus typically carries a stream of Cb,Y,Cr,Y digital video at VCLK frequency, clocked on the rising edge (by default) of VCLK.

*2.2.9. ANALOG TV OUTPUT PORT*

**RED_TV / C_TV** *Analog video outputs synchronized with CVBS.* This output is current-driven and must be connected to analog ground over a load resistor ($R_{LOAD}$). Following the load resistor, a simple analog low pass filter is recommended. In S-VHS mode, this is the Chrominance Output.

**GREEN_TV / Y_TV** *Analog video outputs synchronized with CVBS.* This output is current-driven and must be connected to analog ground over a load resistor ($R_{LOAD}$). Following the load resistor, a simple analog low pass filter is recommended. In S-VHS mode, this is the Luminance Output.

**BLUE_TV / CVBS** *Analog video outputs synchronized with CVBS.* This output is current-driven and must be connected to analog ground over a load resistor ($R_{LOAD}$). Following the load resistor, a simple analog low pass filter is recommended. In S-VHS mode, this is a second composite output.

**CVBS** *Analog video composite output (luminance/ chrominance).* CVBS is current-driven and must be connected to analog ground over a load resistor ($R_{LOAD}$). Following the load resistor, a simple analog low pass filter is recommended.

**IREF1_TV** *Ref. current* for CVBS 10-bit DAC.

**IREF2_TV** *Reference current* for RGB 10-bit DAC.

**VREF1_TV** *Ref. voltage* for CVBS 10-bit DAC. Connect to analog ground.

**VREF2_TV** *Reference voltage* for RGB 10-bit DAC. Connect to analog ground.

**VSSA_TV** *Analog $V_{SS}$* for DACs.

**VDDA_TV** *Analog $V_{DD}$* for DACs.

JTAG Signals

**VCS** *Line synchronisation Output.* This pin is an input in ODDEV+HSYNC or VSYNC + HSYNC or VSYNC slave modes and an output in all other modes (master/slave)

**ODD_EVEN** *Frame Synchronisation Output.* This pin supports the Frame synchronisation signal. It is an input in slave modes, except when sync is extracted from YCrCbdata, and an output in master mode and when sync is extracted from YCrCb data
The signal is synchronous to rising edge of DCLK. The default polarity for this pin is:
- odd (not-top) field: LOW level
- even (bottom) field: HIGH level

*2.2.10. MISCELLANEOUS*

**SPKRD** *Speaker Drive.* This the output to the speaker. It is an AND of the counter 2 output with bit 1 of Port 61, and drives an external speaker driver. This output should be connected to 7407 type high voltage driver.

**SCL, SDA** $I^2C$ Interface. These bidirectional pins are connected to CRTC register 3Fh to implement DDC capabilities. They conform to $I^2C$ electrical specifications, they have open-collector output drivers which are internally connected to $V_{DD}$ through pull-up resistors.

They can be used for the DDC1 (SCL) and DDC0 (SDA) lines of the VGA interface.

**SCAN_ENABLE** *Reserved*. The pin is reserved for Test and Miscellaneous functions.

**COL_SEL** *Colour Select.* Can be used for Picture in Picture function. Note however that this signal, brought out from the video pipeline, is not in sync with the VGA output signals, i.e. the VGA signals run four clock cycles after the Col_Sel signal.

**VDD_CORE** *2.5 V Power Supply.* These power pins are necessary to supply the core with 2.5 V.

**TCLK** *Test clock*

**TDI** *Test data input*

**TMS** *Test mode input*

**TDO** *Test data output*

**Table 2-7. Pinout.**

| Pin # | Pin name |
|---|---|
| AF3 | SYSRSETI# |
| AE4 | SYSRSETO# |
| A3 | XTALI |
| C4 | XTALO |
| G23 | HCLK |
| H24 | DEV_CLK |
| AD11 | DCLK |
| AF15 | MCLKI |
| AB23 | MCLKO |
| AE16 | MA[0] |
| AD15 | MA[1] |
| AF16 | MA[2] |
| AE17 | MA[3] |
| AD16 | MA[4] |
| AF17 | MA[5] |
| AE18 | MA[6] |
| AD17 | MA[7] |
| AF18 | MA[8][3] |
| AE19 | MA[9][3] |
| AE20 | MA[10] |
| AC19 | MA[11]/BA[0] |
| AF22 | CS#[0] |
| AD21 | CS#[1] |
| AE24 | CS#[2]/MA[11] |
| AD23 | CS#[3]/MA[12]/BA[1] |
| AF23 | RAS#[0] |
| AD22 | RAS#[1] |
| AE21 | CAS#[0] |
| AC20 | CAS#[1] |
| AF20 | DQM#[0] |
| AD19 | DQM#[1] |
| AF21 | DQM#[2] |
| AD20 | DQM#[3] |
| AE22 | DQM#[4] |
| AE23 | DQM#[5] |
| AF19 | DQM#[6] |
| AD18 | DQM#[7] |
| AC22 | MWE# |
| R1 | MD[0][3] |
| T2 | MD[1][3] |
| R3 | MD[2] |
| T1 | MD[3] |
| R4 | MD[4] |
| U2 | MD[5] |
| T3 | MD[6] |
| U1 | MD[7] |
| U4 | MD[8] |
| V2 | MD[9] |
| U3 | MD[10] |
| V1 | MD[11] |
| W2 | MD[12] |
| V3 | MD[13] |
| Y2 | MD[14] |
| W4 | MD[15] |
| Y1 | MD[16] |
| W3 | MD[17] |
| AA2 | MD[18] |
| Y4 | MD[19] |
| AA1 | MD[20] |
| Y3 | MD[21] |
| AB2 | MD[22] |
| AB1 | MD[23] |
| AA3 | MD[24] |
| AB4 | MD[25] |
| AC1 | MD[26] |
| AB3 | MD[27] |
| AD2 | MD[28] |
| AC3 | MD[29] |
| AD1 | MD[30] |
| AF2 | MD[31] |
| AF24 | MD[32] |
| AE26 | MD[33] |
| AD25 | MD[34] |
| AD26 | MD[35] |
| AC25 | MD[36] |
| AC24 | MD[37] |
| AC26 | MD[38] |
| AB25 | MD[39] |
| AB24 | MD[40] |
| AB26 | MD[41] |
| AA25 | MD[42] |
| Y23 | MD[43] |
| AA24 | MD[44] |
| AA26 | MD[45] |
| Y25 | MD[46] |
| Y26 | MD[47] |
| Y24 | MD[48] |
| W25 | MD[49][3] |
| V23 | MD[50][3] |
| W26 | MD[51][3] |
| W24 | MD[52][3] |
| V25 | MD[53][3] |
| V26 | MD[54][3] |
| U25 | MD[55][3] |
| V24 | MD[56][3] |
| U26 | MD[57][3] |
| U23 | MD[58][3] |
| T25 | MD[59][3] |
| U24 | MD[60][3] |
| T26 | MD[61][3] |
| R25 | MD[62][3] |
| R26 | MD[63][3] |
| F24 | PCI_CLKI |
| D25 | PCI_CLKO |
| B20 | AD[0] |
| C20 | AD[1] |
| B19 | AD[2] |
| A19 | AD[3] |
| C19 | AD[4] |
| B18 | AD[5] |
| A18 | AD[6] |
| B17 | AD[7] |
| C18 | AD[8] |
| A17 | AD[9] |
| D17 | AD[10] |
| B16 | AD[11] |
| C17 | AD[12] |
| B15 | AD[13] |
| A15 | AD[14] |
| C16 | AD[15] |
| B14 | AD[16] |
| D15 | AD[17] |
| A14 | AD[18] |
| B13 | AD[19] |
| D13 | AD[20] |
| A13 | AD[21] |
| C14 | AD[22] |
| B12 | AD[23] |
| C13 | AD[24] |
| A12 | AD[25] |
| C12 | AD[26] |
| A11 | AD[27] |
| D12 | AD[28] |
| B10 | AD[29] |
| C11 | AD[30] |
| A10 | AD[31] |
| D10 | CBE[0] |
| C10 | CBE[1] |
| A9 | CBE[2] |
| B8 | CBE[3] |
| A8 | FRAME# |
| B7 | TRDY# |
| D8 | IRDY# |
| A7 | STOP# |
| C8 | DEVSEL# |
| B6 | PAR |

| Pin # | Pin name |
|---|---|
| AC2 | TDO |
| | |
| AD12 | VDDA_TV |
| AF8 | VDD_DAC1 |
| G24 | VDD_CPUCLK_PLL[1] |
| AD13 | VDD_DCLK_PLL[1] |
| F25 | VDD_DEVCLK_PLL[1] |
| AC17 | VDD_MCLKI_PLL[1] |
| AC15 | VDD_MCLKO_PLL[1] |
| F26 | VDD_HCLK_PLL[1] |
| E25 | VDD_SKEW_PLL[1] |
| | |
| D11 | VDD_CORE[1] |
| L23 | VDD_CORE[1] |
| T4 | VDD_CORE[1] |
| AC6 | VDD_CORE[1] |
| | |
| D6 | VDD |
| D16 | VDD |
| D21 | VDD |
| F4 | VDD |
| F23 | VDD |
| AC11 | VDD |
| AC16 | VDD |
| AC21 | VDD |
| AA4 | VDD |
| AA23 | VDD |
| T23 | VDD |
| L4 | VDD |
| | |
| AF13 | VSSA_TV |
| AC9 | VSS_DAC1 |
| A1:2 | VSS |
| A26 | VSS |
| B2 | VSS |
| B25:26 | VSS |
| C3 | VSS |
| C24 | VSS |
| D4 | VSS |
| D9 | VSS |
| D14 | VSS |
| D19 | VSS |
| D23 | VSS |
| H4 | VSS |
| J23 | VSS |
| L11:16 | VSS |
| M11:16 | VSS |
| N4 | VSS |
| N11:16 | VSS |

| Pin # | Pin name |
|---|---|
| P11:16 | VSS |
| P23 | VSS |
| R11:16 | VSS |
| T11:16 | VSS |
| V4 | VSS |
| W23 | VSS |
| AC4 | VSS |
| AC8 | VSS |
| AC13 | VSS |
| AC18 | VSS |
| AC23 | VSS |
| AD3 | VSS |
| AD14 | COMPENSATION_VS |
| AD24 | VSS |
| AE1:2 | VSS |
| AE25 | VSS |
| AF1 | VSS |
| AF25 | VSS |
| AF26 | VSS |
| | |
| A16 | *Unconnected* |
| B9 | *Unconnected* |
| B11 | *Unconnected* |
| D18 | *Unconnected* |
| E26 | *Unconnected* |
| AD9 | *Unconnected* |
| AF10 | *Unconnected* |

Note[1]; These pins must be connected to the 2.5 V power supply. They **must not** be connected to the 3.3 V supply.

### *3.1.2. ADPC STRAP REGISTER 1 CONFIGURATION*

*Strap1* Access = 0022h/0023h Regoffset = 04Bh

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Rsv | | Rsv | | Rsv | Rsv | Rsv | |
| This register defaults to the values sampled on MD[13:10] pins after reset | | | | | | | |

| Bit Number Sampled | Mnemonic | Description |
|---|---|---|
| Bits 7-6 | Rsv | Reserved |
| Bits 5-2 | MD[13:10] | Reserved |
| Bits 1-0 | Rsv | Reserved |

## 4.4. DC CHARACTERISTICS

**Table 4-2. DC Characteristics**

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating Voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{CORE}$ | Operating Voltage | | 2.45 | 2.5 | 2.7 | V |
| $P_{DD}$ | Supply Power | $3.0V < V_{DD} < 3.6V$ | | | 0.18 | W |
| $P_{CORE}$ | Supply Power | $2.45V < V_{CORE} < 2.7V$ | | | 2.90 | W |
| $V_{IL}$ | Input Low Voltage | Except XTALI | -0.3 | | 0.8 | V |
| | | XTALI | -0.3 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | Except XTALI | 2.1 | | $V_{DD}$+0.3 | V |
| | | XTALI | 2.35 | | $V_{DD}$+0.3 | V |
| $I_{LK}$ | Input Leakage Current | Input, I/O | -5 | | 5 | µA |
| | Integrated Pull up/down | | | 50 | | KΩ |

**Table 4-3. PAD buffers DC Characteristics**

| Buffer Type | I/O count | $V_{IH}$ min (V) | $V_{IL}$ max (V) | $V_{OH}$ min (V) | $V_{OL}$ max (V) | $I_{OL}$ min (mA) | $I_{OH}$ max (mA) | $C_{load}$ max (pF) | Derating (ps/pF)[1] | $C_{IN}$ (pF) |
|---|---|---|---|---|---|---|---|---|---|---|
| ANA | 8 | 2.35 | 0.9 | - | - | - | - | - | - | - |
| OSCI13B | 1 | 2.1 | 0.8 | 2.4 | 0.4 | 2 | - 2 | 50 | - | - |
| BT8TRP_TC | 5 | - | - | 2.4 | 0.4 | 8 | - 8 | 200 | 21 | 6.89 |
| BD4STRP_FT | 50 | 2 | 0.8 | 2.4 | 0.4 | 4 | - 4 | 100 | 42 | 5.97 |
| BD4STRUP_FT | 10 | 2 | 0.8 | 2.4 | 0.4 | 4 | - 4 | 100 | 41 | 5.97 |
| BD8STRP_FT | 26 | 2 | 0.8 | 2.4 | 0.4 | 8 | - 8 | 200 | 23 | 5.96 |
| BD8STRUP_FT | 40 | 2 | 0.8 | 2.4 | 0.4 | 8 | - 8 | 200 | 23 | 5.96 |
| BD8STRP_TC | 10 | 2 | 0.8 | 2.4 | 0.4 | 8 | - 8 | 200 | 21 | 7.02 |
| BD8TRP_TC | 60 | 2 | 0.8 | 2.4 | 0.4 | 8 | - 8 | 200 | 21 | 7.03 |
| BD8PCIARP_FT | 49 | $0.5*V_{DD}$ | $0.3*V_{DD}$ | $0.9*V_{DD}$ | $0.1*V_{DD}$ | 1.5 | - 0.5 | 200 | 15 | 6.97 |
| BD16STARUQP_TC | 19 | 2 | 0.8 | 2.4 | 0.4 | 16 | -16 | 400 | 12 | 9.34 |
| SCHMITT_FT | 1 | 2 | 0.8 | - | - | - | - | - | - | 5.97 |
| TLCHT_FT | 5 | 2 | 0.8 | - | - | - | - | - | - | 5.97 |
| TLCHT_TC | 1 | 2 | 0.8 | - | - | - | - | - | - | 5.97 |
| TLCHTD_TC | 1 | 2 | 0.8 | - | - | - | - | - | - | 5.97 |
| Note 1: time to output variation depending on the capacitive load. | | | | | | | | | | |

**Table 4-4. RAMDAC DC Specification**

| Symbol | Parameter | Min | Max |
|---|---|---|---|
| Vref_dac | Voltage Reference | 1.00 V | 1.24 V |
| INL | Integrated Non Linear Error | - | 3 LSB |
| DNL | Differentiated Non Linear Error | - | 1 LSB |
| BLC | Black Level Current | 1.0 mA | 2.0 mA |
| WLC | White Level Current | 15.00 mA | 18.50 mA |

*4.5.7. LOCAL BUS INTERFACE*

Figure 4-3 to Figure 4-11 and Table 4-15 list the AC characteristics of the Local Bus interface.

**Figure 4-8. Synchronous Read Cycle**

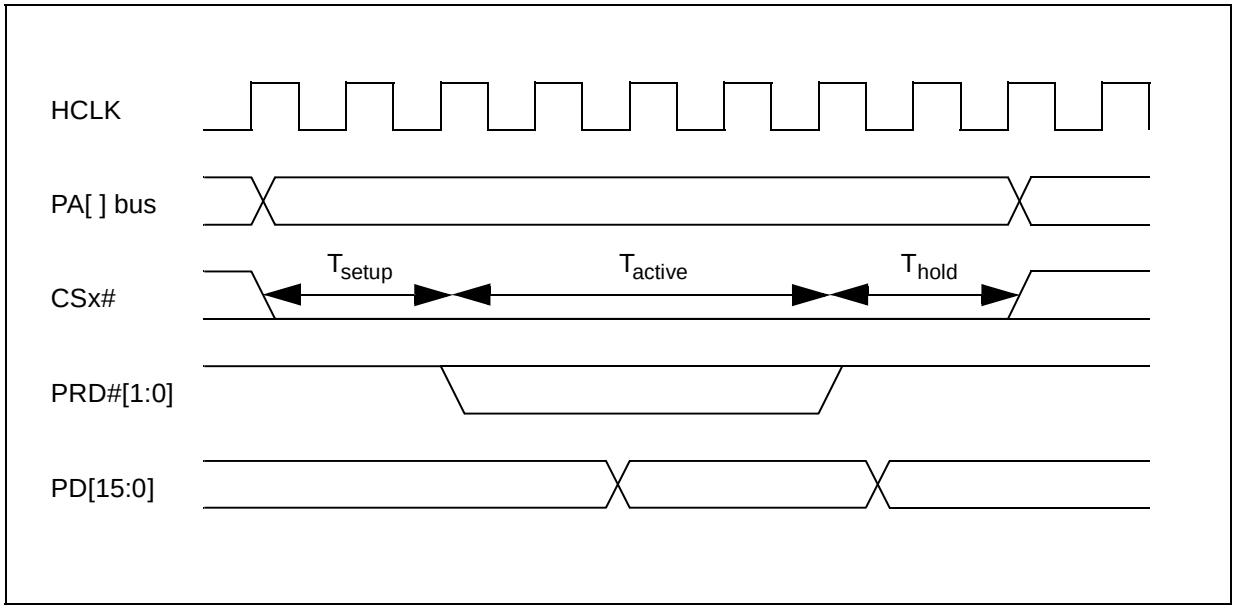
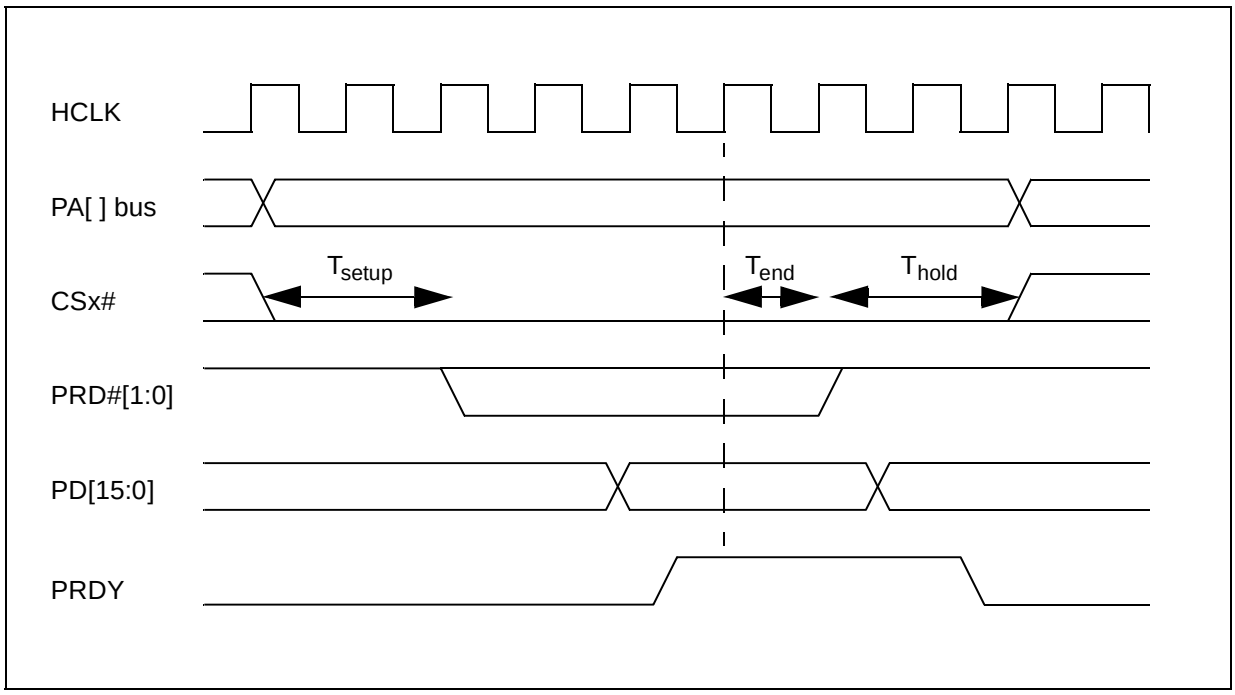



**Figure 4-9. Asynchronous Read Cycle**



The Table 4-14 below refers to Vh, Va, Vs which are the register value for Setup time, Active Time and Hold time, as described in the Programming Manual.

**Table 4-14. Local Bus cycle lenght**

| Cycle | $T_{setup}$ | $T_{active}$ | $T_{hold}$ | $T_{end}$ | Unit |
|---|---|---|---|---|---|
| Memory (FCSx#) | 4 + Vh | 2 + Va | 4 + Vs | 4 | HCLK |
| Peripheral (IOCSx#) | 8 + Vh | 3 + Va | 4 + Vs | 4 | HCLK |

**Table 4-15. Local Bus Interface AC Timing**

| Name | Parameters | Min | Max | Units |
|---|---|---|---|---|
| | HCLK to PA bus | - | 15 | nS |
| | HCLK to PD bus | - | 15 | nS |
| | HCLK to FCS#[1:0] | - | 15 | nS |
| | HCLK to IOCS#[3:0] | - | 15 | nS |
| | HCLK to PWR#[1:0] | - | 15 | nS |
| | HCLK to PRD#[1:0] | - | 15 | nS |
| | PD[15:0] Input setup to HCLK | - | 4 | nS |
| | PD[15:0] Input hold to HCLK | 2 | - | nS |
| | PRDY Input setup to HCLK | - | 4 | nS |
| | PRDY Input hold to HCLK | 2 | - | nS |

*4.5.12 INTENSIONNALY BLANK*

*6.3.3. SDRAM*

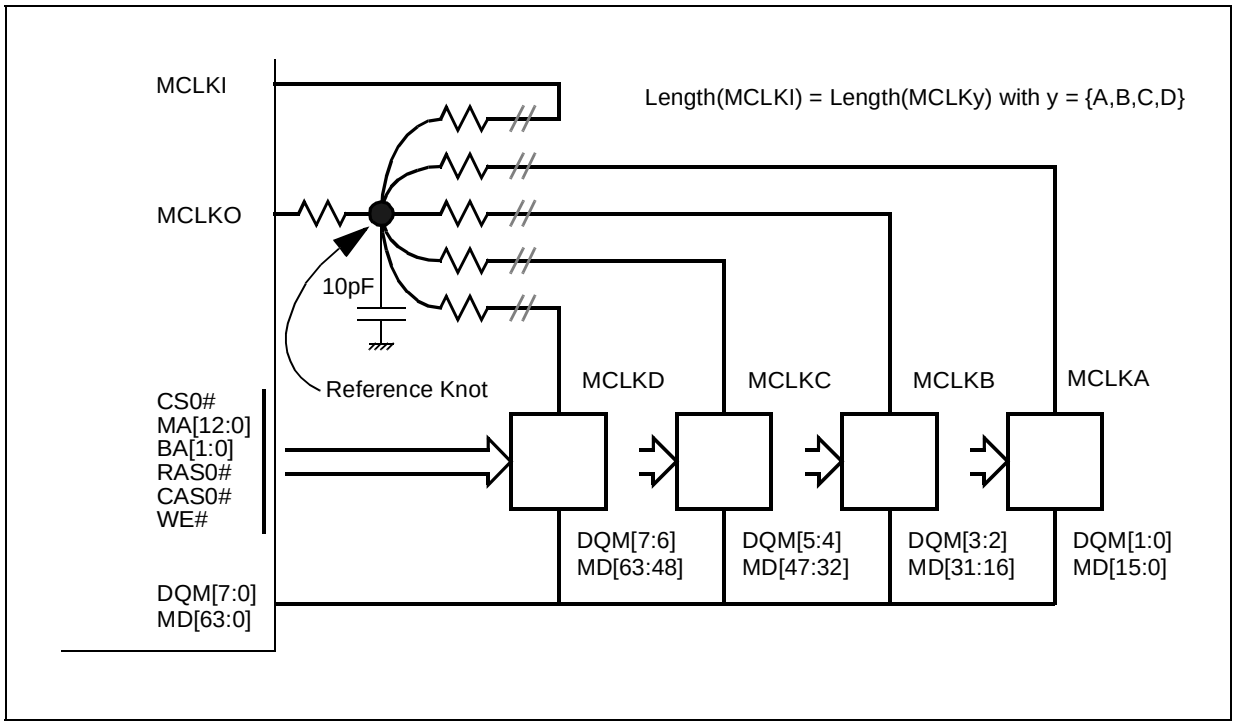
The STPC provides all the signals for SDRAM control. Up to 128 MBytes of main memory are supported. All Banks must be 64 bits wide. Up to 4 memory banks are available when using 16Mbit devices. Only up to 2 banks can be connected when using 64Mbit and 128Mbit components due to the reallocation of CS2# and CS3# signals. This is described in Table 6-4 and Table 6-5.

Graphics memory resides at the beginning of Bank 0. Host memory begins at the top of graphics memory and extends to the top of populated SDRAM. Bank 0 must always be populated.

Figure 6-4, Figure 6-5 and Figure 6-6 show some typical implementations.

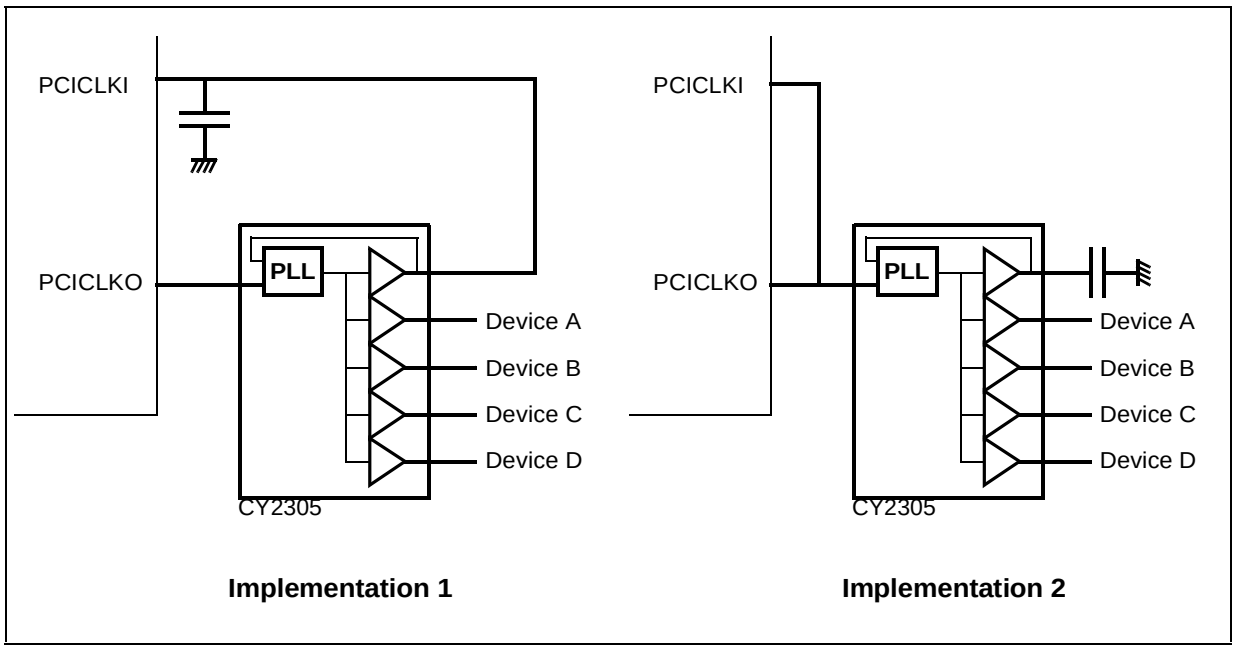
The purpose of the serial resistors is to reduce signal oscillation and EMI by filtering line reflections. The capacitance in Figure 6-4 has a filtering effect too, while it is used for propagation delay compensation in the 2 other figures.

**Figure 6-4. One Memory Bank with 4 Chips (16-bit)**



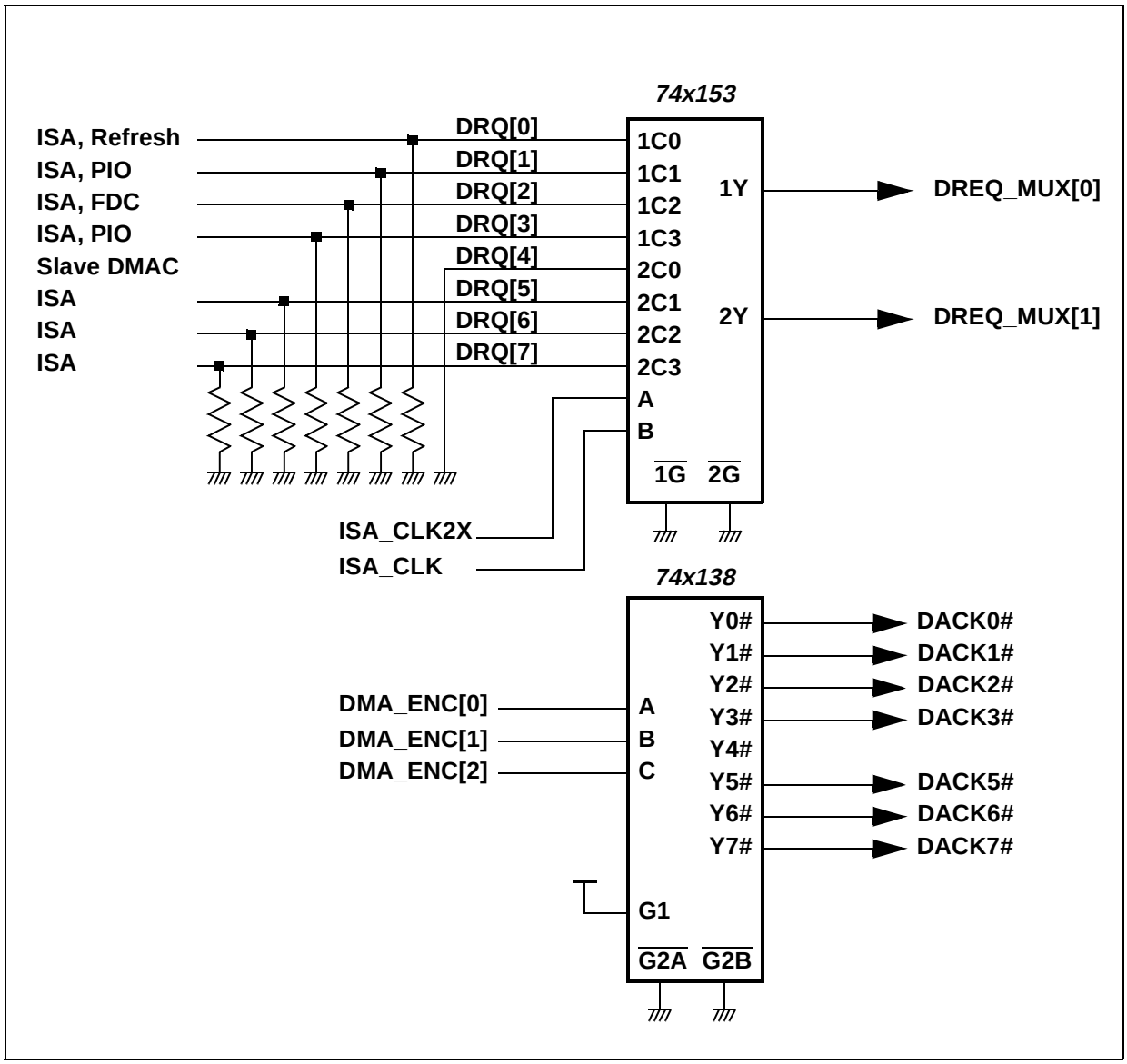
In the case of higher clock load it is recommended to use a zero-delay clock buffer as described in Figure 6-8. This approach is also recommended when implementing the delay on PCICLKI according to the PCI section of the **Electrical Specifications** chapter.

**Figure 6-8. PCI clock routing with zero-delay clock buffer**



The figure below describes a complete implementation of the external glue logic for DMA Request time-multiplexing and DMA Acknowledge demultiplexing. Like for the interrupt lines, this logic can be simplified when only few DMA channels are used in the application.
This glue logic is not needed in Local bus mode as it does not support DMA transfers.

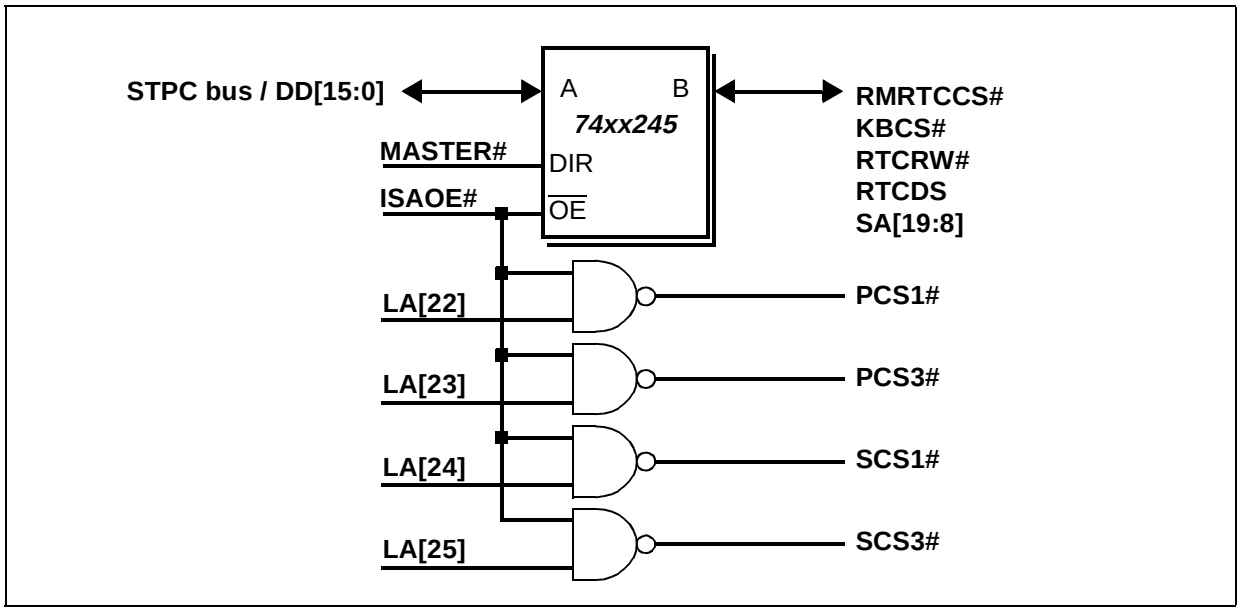
**Figure 6-11. Typical DMA multiplexing and demultiplexing**



### *6.3.7. IDE / ISA DYNAMIC DEMULTIPLEXING*

Some of the ISA bus signals are dynamically multiplexed to optimize the pin count. Figure 6-12 describes how to implement the external glue logic to demultiplex the IDE and ISA interfaces. In Local Bus mode the two buffers are not needed and the NAND gates can be simplified to inverters.

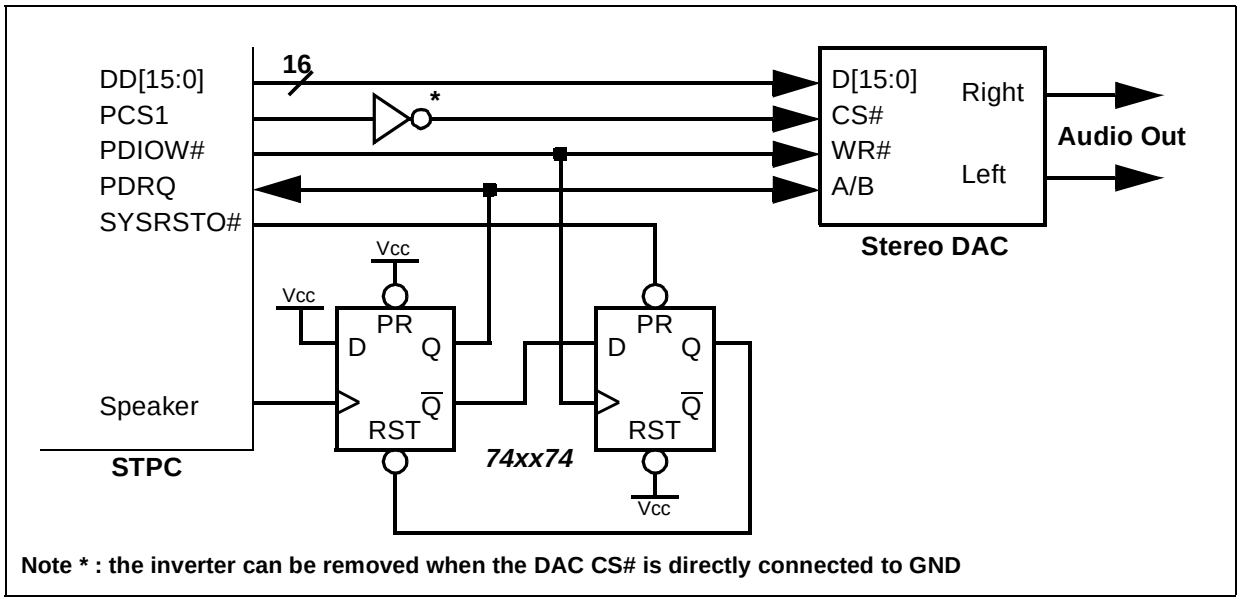
**Figure 6-12. Typical IDE / ISA Demultiplexing**




### *6.3.8. BASIC AUDIO USING IDE INTERFACE*

When the application requires only basic audio capabilities, an audio DAC on the IDE interface can avoid using a PCI-based audio device. This low cost solution is not CPU consuming thanks to the DMA controller implemented in the IDE controller and can generate 16-bit stereo sound. The clock speed is programmable when using the speaker output.

**Figure 6-13. Basic audio on IDE**




**Note * : the inverter can be removed when the DAC CS# is directly connected to GND**

## 6.4. PLACE AND ROUTE RECOMMENDATIONS

### *6.4.1. GENERAL RECOMMENDATIONS*

Some STPC Interfaces run at high speed and need to be carefully routed or even shielded like:

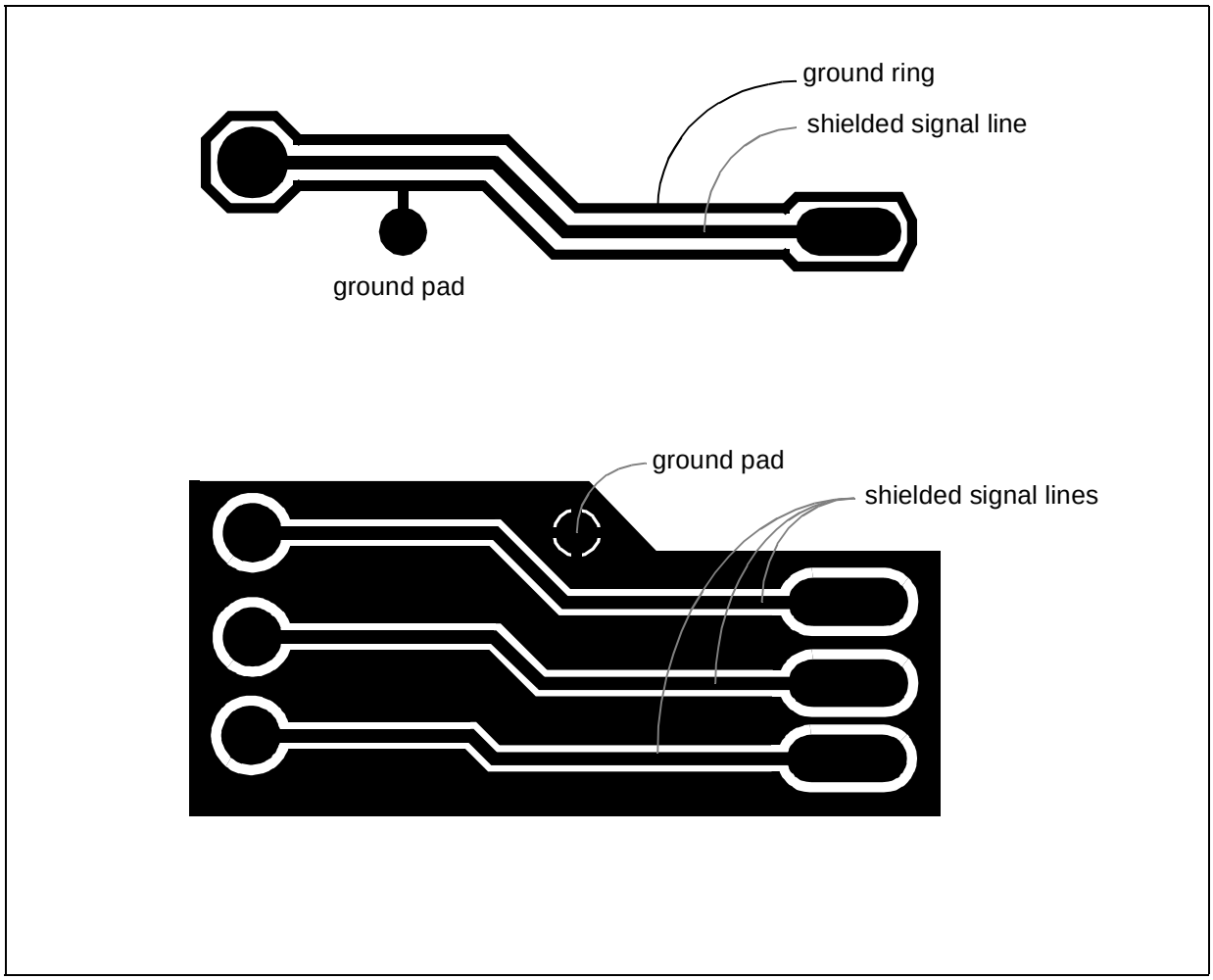
1) Memory Interface
2) PCI bus
3) Graphics and video interfaces
4) 14 MHz oscillator stage

All clock signals have to be routed first and shielded for speeds of 27MHz or higher. The high speed signals follow the same constraints, as for the memory and PCI control signals.

The next interfaces to be routed are Memory, PCI, and Video/graphics.

All the analog noise-sensitive signals have to be routed in a separate area and hence can be routed indepedently.

**Figure 6-17. Shielding signals**




### *6.4.2. PLL DEFINITION AND IMPLIMENTATION*

PLLs are analog cells which supply the internal STPC Clocks. To get the cleanest clock, the jitter on the power supply must be reduced as much as possible. This will result in a more stable system.

Each of the integrated PLL has a dedicated power pin so a single power plane for all of these PLLs, or one wire for each, or any solution in between which help the layout of the board can be used.

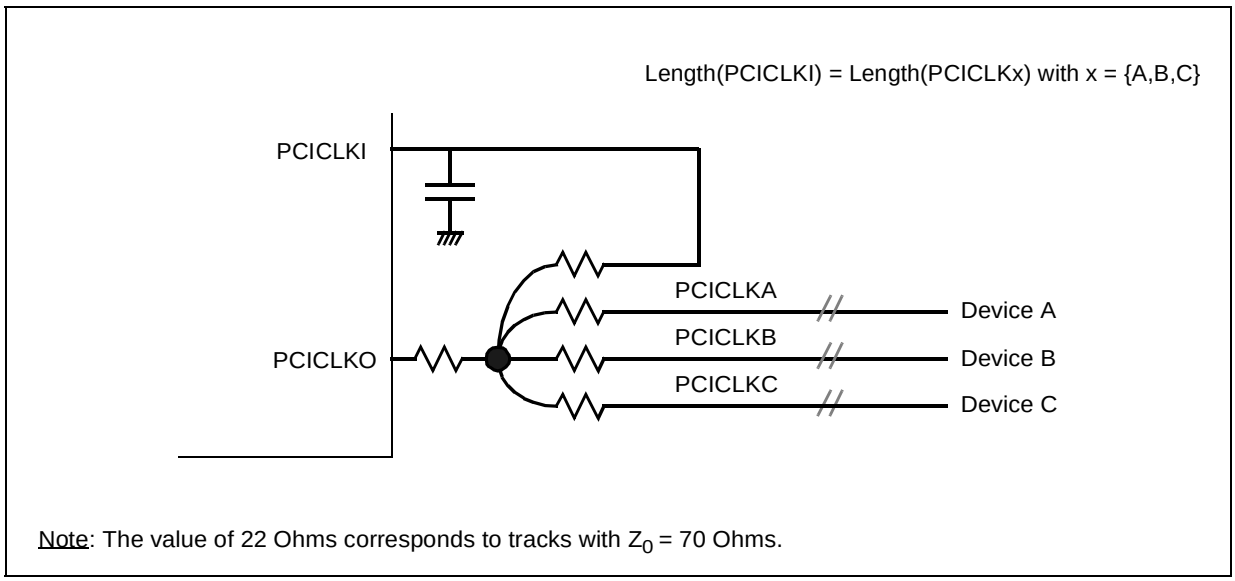
Powering these pins with one Ferrite + capacitances is enough. We recommend at least 2 capacitances: one 'big' (few uF) for power storage, and one or 2 smalls (100nF + 1nF) for noise filtering.

*6.4.4.3. Board Layout Issues*

The physical layout of the motherboard PCB assumed in this presentation is as shown in Figure 6-24. For the PCI interface, the most critical signal is the clock. Any skew between the clocks at the PCI components and the STPC will impact the timing budget. In order to get well matched clocks at all components it is recommended that all the PCI clocks are individually driven from a serial resistance with matched routing lengths. In other words, all clock line lengths that go from the resistor to the PCI chips (PCICLKx) must be identical.

The figure below is for PCI devices soldered on-board. In the case of a PCI slot, the wire length must be shortened by 2.5" to compensate the clock layout on the PCI board. The maximum clock skew between all devices is 2ns according to PCI specifications.

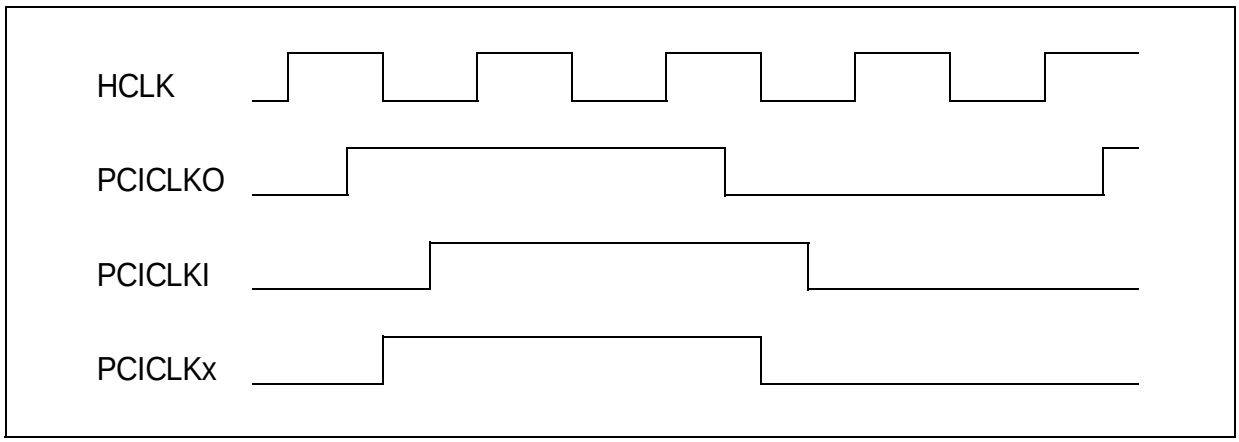
**Figure 6-24. Typical PCI clock routing**




Note: The value of 22 Ohms corresponds to tracks with $Z_0$ = 70 Ohms.

The Figure 6-25 describes a typical clock delay implementation. The exact timing constraints are listed in the PCI section of the **Electrical Specifications** Chapter.

**Figure 6-25. Clocks relationships**



*6.4.5. THERMAL DISSIPATION*

*6.4.5.1. Power saving*

Thermal dissipation of the STPC depends mainly on supply voltage. When the system does not need to work at the upper voltage limit, it may therefore be beneficial to reduce the voltage to the lower voltage limit, where possible. This could save a few 100's of mW.

The second area to look at is unused interfaces and functions. Depending on the application, some input signals can be grounded, and some blocks not powered or shutdown. Clock speed dynamic adjustment is also a solution that can be used along with the integrated power management unit.

*6.4.5.2. Thermal balls*

The standard way to route thermal balls to ground layer implements only one via pad for each ball pad, connected using a 8-mil wire.

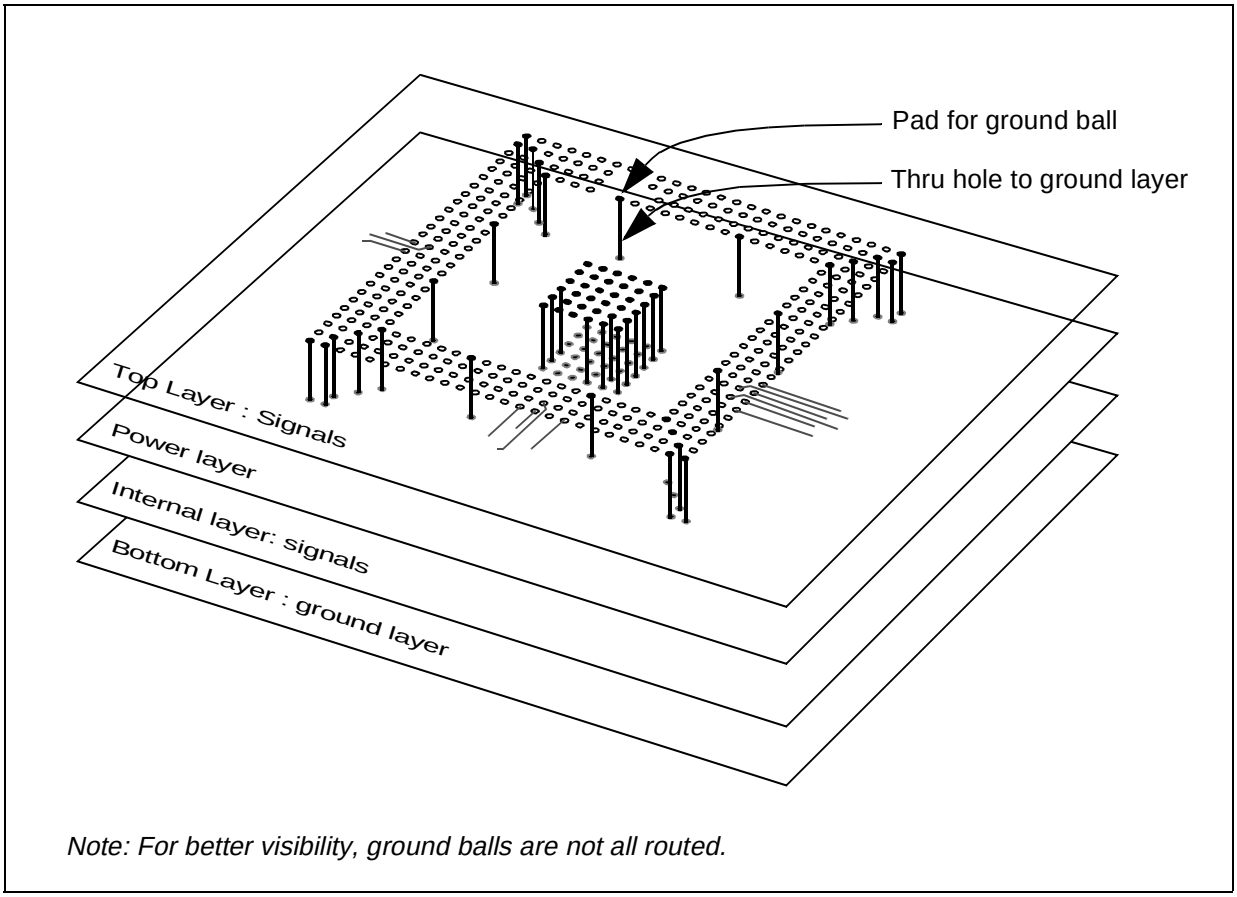
With such configuration the Plastic BGA package does 90% of the thermal dissipation through the ground balls, and especially the central thermal balls which are directly connected to the die. The remaining 10% is dissipated through the case. Adding a heat sink reduces this value to 85%.

As a result, some basic rules must be followed when routing the STPC in order to avoid thermal problems.

As the whole ground layer acts as a heat sink, the ground balls must be directly connected to it, as illustrated in Figure 6-26. If one ground layer is not enough, a second ground plane may be added.

When possible, it is important to avoid other devices on-board using the PCB for heat dissipation, like linear regulators, as this would heat the STPC itself and reduce the temperature range of the whole system, In case these devices can not use a separate heat sink, they must not be located just near the STPC

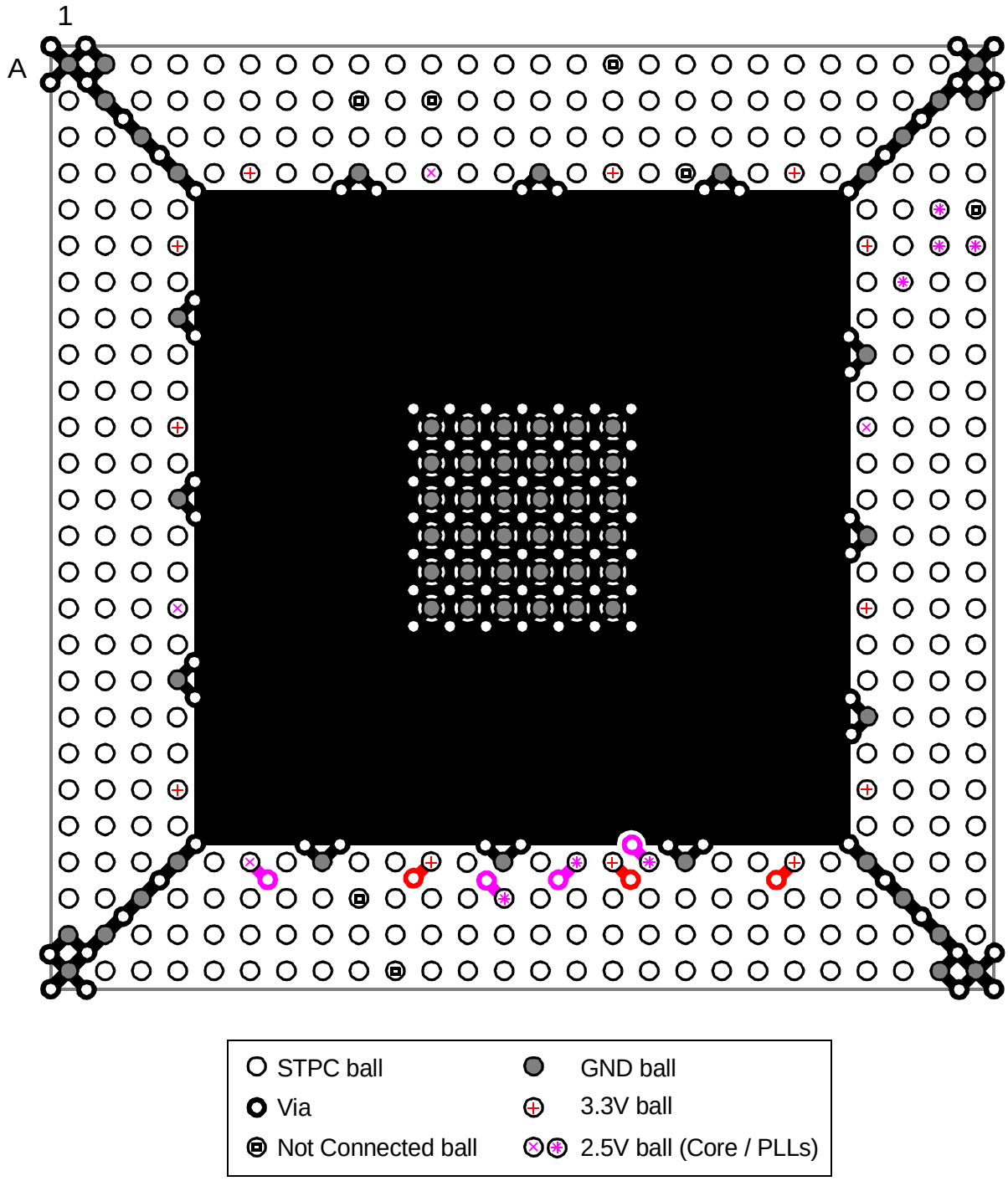
**Figure 6-26. Ground routing**




*Note: For better visibility, ground balls are not all routed.*

As the PCB acts as a heat sink, the layout of top and ground layers must be done with care to maximize the board surface dissipating the heat. The only limitation is the risk of losing routing channels. Figure 6-31 and Figure 6-32 show a routing with a good thermal dissipation thanks to an optimized placement of power and signal vias. The ground plane should be on bottom layer for the best heat spreading (thicker layer than internal ones) and dissipation (direct contact with air). .

**Figure 6-31. Layout for Good Thermal Dissipation - top layer**



RMRTCCS# cycle to inform the ISA controller of a 16-bit device.

*6.5.3.3. POST code*

Once the 16 first bytes are fetched and decoded, the CPU core continue its execution depending on the content of these first data. Usually, it corresponds to a JUMP instruction and the code fetching continues, generating read cycles on the ISA bus.

Most of the BIOS and boot loaders are reading the content of the flash, decompressing it in SDRAM, and then continue the execution by jumping to the entry point in RAM. This boot process ends with a JUMP to the entry point of the OS launcher.
These various steps of the booting sequence are codified by the so-called POST codes (Power-On Self-Test). A 8-bit code is written to the port 80H at the beginning of each stage of the booting process (I/O write to address 0080H) and can be displayed on two 7-segment display, enabling a fast visual check of the booting completion level.
Usually, the last POST code is 0x00 and corresponds to the jump into the OS launcher.

When the execution fails or hangs, the lastest written code stays visible on that display, indicating either the piece of code to analyse, either the area of the hardware not working properly.

*6.5.4. LOCAL BUS MODE*

As the Local Bus controller is located into the Host interface, there is no access to the cycles on the PCI, reducing the amount of signals to check.

*6.5.4.1. First code fetches*

When booting on the Local Bus, the key signal to check at the very beginning is FCS0#. This signal is a Chip Select for the boot flash and should toggle together with PRD# to fetch the first 16 bytes of code. This corresponds to the loading of the first line of the CPU cache.
In case FCS0# does not toggle, then one of the previous steps has not been done properly, like HCLK speed and CPU clock multiplier (x1, x2).

*6.5.4.2. Boot Flash size*

The Local Bus support 16-bit boot memory devices only.

*6.5.4.3. POST code*

Like in ISA mode, POST codes can be implemented on the Local Bus. The difference is that an IOCS# must be programmed at I/O address 80H prior to writing these code, the POST display being connected to this IOCS# and to the lower 8 bits of the bus.

*6.5.5. SUMMARY*

Here is a check-list for the STPC board debug from power-on to CPU execution.

For each step, in case of failure, verify first the corresponding balls of the STPC:
- check if the voltage or activity is correct
- search for potential shortcuts.

For troubleshooting in steps 5 to 10, verify the related strap options:
- value & connection. Refer to Section 3.
- see Figure 4-3 for timing constraints

Steps 8a and 9a are for debug in ISA mode while steps 8b and 9b are for Local Bus mode.

| | Check: | How? | Troubleshooting |
|---|---|---|---|
| 1 | Power supplies | Verify that voltage is within specs:<br>- this must include HF & LF noise<br>- avoid full range sweep<br>Refer to Table 4-1 for values | Measure voltage near STPC balls:<br>- use very low GND connection.<br>Add some decoupling capacitor:<br>- the smallest, the nearest to STPC balls. |
| 2 | 14.318 MHz | Verify OSC14M speed | The 2 capacitors used with the quartz must match with the capacitance of the crystal.<br>Try other values. |
| 3 | SYSRSTI#<br>(Power Good) | Measure SYSRSTI# of STPC<br>See Figure 4-3 for waveforms. | Verify reset generation circuit:<br>- device reference<br>- components value |
| 5 | HCLK | Measure HCLK is at selected frequency<br>25MHz < HCLK < 100MHz | HCLK wire must be as short as possible |

| | Check: | How? | Troubleshooting |
|---|---|---|---|
| 6 | PCI clocks | Measure PCICLKO:<br>- maximum is 33MHz by standard<br>- check it is at selected frequency<br>- it is generated from HCLK by a division (1/2, 1/3 or 1/4)<br>Check PCICLKI equals PCICLKO | Verify PCICLKO loops to PCICLKI.<br>Verify maximum skew between any PCI clock branch is below 2ns.<br>In Synchronous mode, check MCLKI. |
| 7 | Memory clocks | Measure MCLKO:<br>- use a low-capacitance probe<br>- maximum is 100MHz<br>- check it is at selected frequency<br>- In SYNC mode MCLK=HCLK<br>- in ASYNC mode, default is 66MHz<br>Check MCLKI equals MCLKO | Verify load on MCLKI.<br>Verify MCLK programming (BIOS setting). |
| 4 | SYSRSTO# | Measure SYSRSTO# of STPC<br>See Figure 4-3 for waveforms. | Verify SYSRSTI# duration.<br>Verify SYSRSTI# has no glitch<br>Verify clocks are running. |
| 8a | PCI cycles | Check PCI signals are toggling:<br>- FRAME#, IRDY#, TRDY#, DEVSEL#<br>- these signals are active low.<br>Check, with a logic analyzer, that first PCI cycles are the expected ones: memory read starting at address with lower bits to 0xFFF0 | Verify PCI slots<br>If the STPC don't boot<br>- verify data read from boot memory is OK<br>- ensure Flash is correctly programmed<br>- ensure CMOS is cleared. |
| 9a | ISA cycles to boot memory | Check RMRTCCS# & MEMRD#<br>Check directly on boot memory pin | Verify MEMCS16#:<br>- must not be asserted for 8-bit memory<br>Verify IOCHRDY is not be asserted<br>Verify ISAOE# pin:<br>- it controls IDE / ISA bus demultiplexing |
| 8b | Local Bus cycles to boot memory | Check FCS0# & PRD#<br>Check directly on boot memory pin | Verify HCLK speed and CPU clock mode. |
| 9b | | Check, with a logic analyzer, that first Local Bus cycles are the expected one: memory read starting at the top of boot memory less 16 bytes | If the STPC don't boot<br>- verify data read from boot memory is OK<br>- ensure Flash is correctly programmed<br>- ensure CMOS is cleared. |
| 10 | The CPU fills its first cache line by fetching 16 bytes from boot memory.<br>Then, first instructions are executed from the CPU.<br>Any boot memory access done after the first 16 bytes are due to the instructions executed by the CPU<br>=> Minimum hardware is correctly set, CPU executes code.<br>Please have a look to the Bios Writer's Guide or Programming Manual to go further with your board testing. | | |

**6.6.**