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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c54-10-so

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8.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

8.1.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 8-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

8.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 8-5 shows the delay from the external clock edge to the timer incrementing.



the error in measuring the interval between two edges on Timer0 input = ± 4 Tosc max.

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TABLE 11-1: DEVELOPMENT TOOLS FROM MICROCHIP

	PIC12CXXX	PIC14000	PIC16C5X	X92912IA	PIC16CXXX	PIC16F62X	X7D81DI9	XX7O91OI9	78291219	PIC16F8XX	PIC16C9XX	PIC17C4X	XXTOTIOI9	PIC18CXX2	PIC18FXXX	63CXX 52CXX/ 54CXX/	хххсэн	мсвеххх	MCP2510
MPLAB [®] Integrated Development Environment	>	>	>	>	>	>	>	>	>	>	>	>	>	>	>				
MPLAB® C17 C Compiler												>	>						
MPLAB® C18 C Compiler														~	>				
MPASM TM Assembler/ MPLINK TM Object Linker	>	>	>	>	^	>	>	>	>	>	>	>	>	>	>	>	>		
MPLAB® ICE In-Circuit Emulator	<	>	>	~	~	×*`	~	>	>	>	>	>	>	~	>				
ICEPIC TM In-Circuit Emulator	>		>	>	>		>	>	>		>								
et MPLAB® ICD In-Circuit Debugger Debugger				*			*			>					>				
ଏ PICSTART® Plus Entry Level ଅପେତା Programmer	<	>	>	>	>	**`	>	>	>	>	>	>	>	>	>				
PRO MATE® II Do Universal Device Programmer D	>	>	>	>	>	** ⁄	>	>	>	>	>	>	>	>	>	>	>		
PICDEM TM 1 Demonstration Board			>		>		* +		>			>							
PICDEM TM 2 Demonstration Board				∕+			<↓ ↓							>	>				
PICDEM TM 3 Demonstration Board											>								
면 PICDEM TM 14A Demonstration Board		>																	
☐ PICDEM™ 17 Demonstration B Board													>						
KEELoq® Evaluation Kit																	>		
KEELoa® Transponder Kit																	>		
e microlD™ Programmer's Kit																		>	
₫ 125 kHz microID™ Developer's Kit																		>	
125 kHz Anticollision microlD TM Developer's Kit																		~	
13.56 MHz Anticollision microlD TM Developer's Kit																		~	
MCP2510 CAN Developer's Kit																			>
* Contact the Microchip Technology In ** Contact Microchip Technology Inc. fo [†] Development tool is available on sel	nc. web s or avails lect devi	site at w ability da ices.	ww.micr tte.	ochip.cc	om for inf	ormation	on how 1	to use the	MPLAB	® ICD In	Circuit I	Debugg	er (DV16	4001) w	ith PIC16	SC62, 63,	64, 65, 7	2, 73, 74,	76, 77.

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FIGURE 12-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING -PIC16C54/55/56/57

TABLE 12-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57

AC Chara	cteristics	Standard Operating Conditions (uOperating Temperature $0^{\circ}C \leq$ $-40^{\circ}C \leq$ $-40^{\circ}C \leq$	I NIESS (TA ≤ +7 TA ≤ +8 TA ≤ +1	otherwi 0°C for 5°C for 25°C for	se spec commei industria r extend	tified) rcial al led	
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	100*	—	_	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low		_	100*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 12-5: TIMER0 CLOCK TIMINGS - PIC16C54/55/56/57



TABLE 12-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54/55/56/57

AC Ch	aracterist	Standard Operating (Operating Temperature	$\begin{array}{llllllllllllllllllllllllllllllllllll$	s other +70°C f +85°C f +125°C	wise s or com or indu for ext	pecifiec mercial strial ended	1)
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
40	Tt0H	TOCKI High Pulse Width - No Prescaler - With Prescaler	0.5 Tcy + 20* 10*		_	ns ns	
41	TtOL	T0CKI Low Pulse Width - No Prescaler - With Prescaler	0.5 Tcy + 20* 10*			ns ns	
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> * N	_	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LC PIC16LC (Comm	R54A-04 R54A-04I ercial, Indus	trial)	Standa Operat	ard Opei ting Tem	ating C perature	ondition • 0° -40°	s (unless otherwise specified) $C \le TA \le +70^{\circ}C$ for commercial $C \le TA \le +85^{\circ}C$ for industrial
PIC16CR PIC16CR (Comm	254A-04, 10 254A-04I, 10 ercial, Indus	, 20 01, 201 strial)	Standa Operat	ard Oper ting Tem	ating C perature	ondition 0° –40°	s (unless otherwise specified) C \leq TA \leq +70°C for commercial C \leq TA \leq +85°C for industrial
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions
	Vdd	Supply Voltage					
D001		PIC16LCR54A	2.0		6.25	V	
D001 D001A		PIC16CR54A	2.5 4.5		6.25 5.5	V V	RC and XT modes HS mode
D002	Vdr	RAM Data Retention Voltage ⁽¹⁾		1.5*	_	V	Device in SLEEP mode
D003	Vpor	VDD Start Voltage to ensure Power-on Reset	_	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	Svdd	VDD Rise Rate to ensure Power-on Reset	0.05*		—	V/ms	See Section 5.1 for details on Power-on Reset
	IDD	Supply Current ⁽²⁾					
D005		PICLCR54A	—	10	20 70	μA μA	Fosc = 32 kHz, VDD = 2.0V Fosc = 32 kHz, VDD = 6.0V
D005A		PIC16CR54A		2.0 0.8 90 4.8	3.6 1.8 350 10	mA mA μA	RC ⁽³⁾ and XT modes: Fosc = 4.0 MHz, VDD = 6.0V Fosc = 4.0 MHz, VDD = 3.0V Fosc = 200 kHz, VDD = 2.5V HS mode: Fosc = 10 MHz, VDD = 5.5V
			—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5 V

Legend: Rows with standard voltage device data only are shaded for improved readability.

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

- 2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .

FIGURE 14-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED



FIGURE 14-7: TYPICA

TYPICAL IPD vs. VDD, WATCHDOG ENABLED



FIGURE 14-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED



IPD, with WDT enabled, has two components: The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At -40° C, the latter dominates explaining the apparently anomalous behavior.











FIGURE 14-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD





FIGURE 14-22: PORTA, B AND C IOL vs. VoL, VDD = 5 V



15.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings ^(†)	
Ambient temperature under bias	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	–0.6V to (VDD + 0.6V)
Total power dissipation ⁽¹⁾	
Max. current out of Vss pin	150 mA
Max. current into VDD pin	100 mA
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, Iik (VI < 0 or VI > VDD)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)	±20 mA
Max. output current sunk by any I/O pin	
Max. output current sourced by any I/O pin	
Max. output current sourced by a single I/O port (PORTA or B)	
Max. output current sunk by a single I/O port (PORTA or B)	50 mA
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH	$+ \sum \{(VDD-VOH) \times IOH\} + \sum (VOL \times IOL)$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

15.6 Timing Diagrams and Specifications

FIGURE 15-2: EXTERNAL CLOCK TIMING - PIC16C54A



TABLE 15-1:	EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

AC Chara	acteristics	Standard Operating Con Operating Temperature	dition: 0°(-40°(-20°(-40°(s (unless o $C \le TA \le +7$ $C \le TA \le +8$ $C \le TA \le +8$ $C \le TA \le +1$	otherwise 0°C for c 5°C for in 5°C for in 25°C for for	e speci commer ndustria ndustria extend	i fied) rcial al al - PIC16LV54A-02I ed
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
	Fosc	External CLKIN Fre-	DC		4.0	MHz	XT OSC mode
		quency ⁽¹⁾	DC	—	2.0	MHz	XT osc mode (PIC16LV54A)
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency ⁽¹⁾	DC	_	4.0	MHz	RC osc mode
			DC	—	2.0	MHz	RC osc mode (PIC16LV54A)
			0.1	—	4.0	MHz	XT osc mode
			0.1	—	2.0	MHz	XT osc mode (PIC16LV54A)
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	10	MHz	HS osc mode (10)
			4.0	—	20	MHz	HS osc mode (20)
			5.0		200	kHz	LP osc mode

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.
 - Instruction cycle period (TcY) equals four times the input oscillator time base period.

FIGURE 16-7: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS - VDD







PIC16C5X



FIGURE 16-9: VIH, VIL OF MCLR, TOCKI AND OSC1 (IN RC MODE) vs. VDD



TABLE 16-2:INPUT CAPACITANCE FOR
PIC16C54A/C58A

Pin	Typical Capa	acitance (pF)
FIII	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
MCLR	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
TOCKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of $\pm 25\%$ (three standard deviations) should be taken into account.

FIGURE 16-23: PORTA, B AND C IOL vs. VOL, VDD = 5V









17.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC PIC16LC (Comm	5X CR5X nercial, Ind	ustrial)	Stand Opera	ard Ope ting Terr	e rating peratu	Condit ire	ions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial
PIC16C5 PIC16CF (Comm	5X R5X nercial, Ind	ustrial)	Stand Opera	ard Ope ting Terr	e rating nperatu	Condit ire	ions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial
Param No.	Symbol	Characteristic/Device	Min	Тур†	Max	Units	Conditions
	IPD	Power-down Current ⁽²⁾					
D020		PIC16LC5X	—	0.25	2	μΑ	VDD = 2.5V, WDT disabled, Commercial
			—	0.25	3	μA	VDD = 2.5V, WDT disabled, Industrial
			_	1 1 25	5	μΑ	VDD = $2.5V$, WDT enabled, Commercial VDD = $2.5V$ WDT enabled Industrial
		PIC16C5X		0.25	4.0	μ.	$V_{DD} = 3.0V$ WDT disabled Commercial
DOZOR			_	0.25	5.0	μΑ	$V_{DD} = 3.0V$, W_{DT} disabled, our intercent VDD = 3.0V. WDT disabled. Industrial
			—	1.8	7.0*	μA	VDD = 5.5V, WDT disabled, Commercial
			—	2.0	8.0*	μA	VDD = 5.5V, WDT disabled, Industrial
			—	4	12*	μΑ	VDD = 3.0V, WDT enabled, Commercial
			—	4	14*	μA	VDD = 3.0V, WDT enabled, Industrial
			—	9.8	27*	μA	VDD = 5.5V, WDT enabled, Commercial
			—	12	30*	μA	VDD = 5.5V, WDT enabled, Industrial

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- **3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .



FIGURE 19-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X-40

TABLE 19-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X-40

AC Charac	teristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$	unless o ≤ +70°0 cribed i	otherwi C (comr n Sectio	se spec nercial) on 19.1.	ified)	
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1000*		_	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



TABLE 20-1: INPUT CAPACITANCE

Pin	Typical Capa	acitance (pF)
FIII	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
MCLR	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
TOCKI	3.2	2.8

All capacitance values are typical at 25° C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.



APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

- 1. Check any CALL, GOTO or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
- 2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change RESET vector to proper value for processor used.
- 6. Remove any use of the ADDLW, RETURN and SUBLW instructions.
- 7. Rewrite any code segments that use interrupts.

APPENDIX B: REVISION HISTORY

Revision KE (January 2013)

Added a note to each package outline drawing.

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4.	. What additions to the data sheet do you think would enhance the structure and subject?		
_			
5.	. What deletions from the data sheet could be made without affecting the overall usefulness?		
6	Is there any incorrect or misleading inform	nation (what and where)?	
0.			
7.	How would you improve this document?		
8.	How would you improve our software, sys	stems, and silicon products?	