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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c54-hs-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 1-1: PIC16C5X FAMILY OF DEVICES

Features	PIC16C54	PIC16CR54	PIC16C55	PIC16C56	PIC16CR56				
Maximum Operation Frequency	40 MHz	20 MHz	40 MHz	40 MHz	20 MHz				
EPROM Program Memory (x12 words)	512	—	512	1K	—				
ROM Program Memory (x12 words)	—	512	—	—	1K				
RAM Data Memory (bytes)	25	25	24	25	25				
Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0				
I/O Pins	12	12	20	12	12				
Number of Instructions	33	33	33	33	33				
Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP				
All PIC [®] Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high									

PIC16C58 Features **PIC16C57** PIC16CR57 PIC16CR58 Maximum Operation Frequency 20 MHz 40 MHz 40 MHz 20 MHz EPROM Program Memory (x12 words) 2K 2K ____ _ ROM Program Memory (x12 words) 2K 2K _ _ RAM Data Memory (bytes) 72 72 73 73 Timer Module(s) TMR0 TMR0 TMR0 TMR0 I/O Pins 20 20 12 12 Number of Instructions 33 33 33 33 28-pin DIP, SOIC; 28-pin DIP, SOIC; 18-pin DIP, SOIC; 18-pin DIP, SOIC; Packages 28-pin SSOP 28-pin SSOP 20-pin SSOP 20-pin SSOP All PIC® Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.

2.0 PIC16C5X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC16C5X Product Identification System at the back of this data sheet to specify the correct part number.

For the PIC16C5X family of devices, there are four device types, as indicated in the device number:

- 1. **C**, as in PIC16**C**54C. These devices have EPROM program memory and operate over the standard voltage range.
- LC, as in PIC16LC54A. These devices have EPROM program memory and operate over an extended voltage range.
- 3. **CR**, as in PIC16**CR**54A. These devices have ROM program memory and operate over the standard voltage range.
- 4. LCR, as in PIC16LCR54A. These devices have ROM program memory and operate over an extended voltage range.

2.1 UV Erasable Devices (EPROM)

The UV erasable versions offered in CERDIP packages, are optimal for prototype development and pilot programs.

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's

PICSTART[®] Plus⁽¹⁾ and PRO MATE[®] programmers both support programming of the PIC16C5X. Third party programmers also are available. Refer to the Third Party Guide (DS00104) for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates, or small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

Note 1: PIC16LC54C and PIC16C54A devices require OSC2 not to be connected while programming with PICSTART[®] Plus programmer.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTPSM) Devices

Microchip offers the unique programming service where a few user defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, giving the customer a low cost option for high volume, mature products.

6.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not

writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as $000u \ u1uu$ (where u = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 10.0, Instruction Set Summary.

REGISTER 6-1: STATUS REGISTER (ADDRESS: 03h)

	R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x		
	PA2	PA1	PA0	TO	PD	Z	DC	С		
	bit 7							bit 0		
bit 7:	PA2: This bit unused at this time.									
	Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.									
bit 6-5:	PA<1:0> : Pr	ogram page p	preselect bits	(PIC16C56/0	CR56)(PIC16	C57/CR57)(P	IC16C58/CR5	58)		
	00 = Page 0	(000h - 1FFh) - PIC16C56	6/CR56, PIC1	6C57/CR57,	PIC16C58/C	R58			
	01 = Page 1	(200h - 3FFh) - PIC16C5	6/CR56, PIC1	6C57/CR57,	PIC16C58/C	R58			
	10 = Page 2 11 = Page 3	. (400h - 3FFh . (600h - 7FFh) - PIC16C5	7/CR57, PIC1	16C58/CR58					
	Each page is	s 512 words.	.,	., e ,						
	Using the PA	A<1:0> bits as	general purp	oose read/wri	te bits in devi	ces which do	not use them	for program		
1.1.4	page presele	ect is not reco	mmended si	nce this may	affect upward	l compatibility	with future pr	oducts.		
Dit 4:	IO: Time-ou	it dit								
	1 = After poly0 = A WDT t	ime-out occur	T instruction	1, Or SLEEP IR	Istruction					
bit 3:	PD: Power-c	down bit								
	1 = After pov	wer-up or by t	he Clrwdt ii	nstruction						
	0 = By exect	ution of the SI	LEEP instruct	ion						
bit 2:	Z: Zero bit									
	1 = The result of the result	ult of an arithm	netic or logic	operation is z	zero					
bit 1.	D = The lest	$\frac{1}{100}$ $\frac{1}$	(for ADDWE 2		tructions)					
DIC 1.			(IOI ADDWF a		silucions					
	1 = A carry f	rom the 4th lo	w order bit o	f the result of	ccurred					
	0 = A carry f	rom the 4th lo	w order bit o	f the result di	d not occur					
	SUBWF	from the Ath	low order bit	of the requit	did not occur					
	1 = A borrow 0 = A borrow	v from the 4th	low order bit	of the result	occurred					
bit 0:	C: Carry/bor	row bit (for AD	DWF, SUBWF	and RRF, RLI	F instructions))				
	ADDWF		SUBW	/F		RRF or RLF				
	1 = A carry c	bccurred	1 = A	borrow did no	ot occur red	Loaded with	LSb or MSb,	respectively		
	v = A carry c		0 = A I							
Lenendi										

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

NOTES:

7.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., MOVF PORTB, W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

7.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used (RA<3:0>). Bits 7-4 are unimplemented and read as '0's.

7.2 PORTB

PORTB is an 8-bit I/O Register (PORTB<7:0>).

7.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16CR56, PIC16CR56, PIC16CS8 and PIC16CR58.

7.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the TRIS f instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

Note:	A read of the ports reads the pins, not the
	output data latches. That is, if an output
	driver on a pin is enabled and driven high,
	but the external system is holding it low, a
	read of the port will indicate that the pin is
	low.

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

TABLE 7-1:	SUMMARY O	F PORT	REGISTERS
			LOIOI LIVO

Value on Value on Bit 4 Bit 3 Bit 1 Bit 0 MCLR and Address Name Bit 7 Bit 6 Bit 5 Bit 2 Power-On Reset WDT Reset TRIS N/A I/O Control Registers (TRISA, TRISB, TRISC) 1111 1111 1111 1111 05h PORTA RA3 RA2 RA1 RA0 _ _ _ _ xxxx _ _ _ _ uuuu PORTB 06h RB7 RB6 RB5 RB4 RB3 RB2 RB1 RB0 XXXX XXXX uuuu uuuu 07h PORTC RC7 RC6 RC5 RC4 RC3 RC2 RC1 RC0 XXXX XXXX uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'

7.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 7-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

FIGURE 7-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



7.6 I/O Programming Considerations

7.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 7-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 7-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;

;				PORT	latch	PORT	pins
;							
	BCF	PORTB,	7	;01pp	pppp	11pp	pppp
	BCF	PORTB,	6	;10pp	pppp	11pp	pppp
	MOVLW	H'3F'		;			
	TRIS	PORTB		;10pp	pppp	10pp	pppp
;							

;Note that the user may have expected the pin ;values to be 00pp pppp. The 2nd BCF caused ;RB7 to be latched as the pin value (High).

7.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 7-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.



FIGURE 7-2: SUCCESSIVE I/O OPERATION

9.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT Reset or Wake-up Reset generates a device RESET.

The $\overline{\text{TO}}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset (Section 6.3).

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 9.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

9.2.1 WDT PERIOD

An 8-bit counter is available as a prescaler for the Timer0 module (Section 8.2), or as a postscaler for the Watchdog Timer (WDT), respectively. For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not

both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio (Section 6.4).

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see Device Characterization).

Under worst case conditions (VDD = Min., Temperature = Max., WDT prescaler = 1:128), it may take several seconds before a WDT time-out occurs.

9.2.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction RESETS the WDT and the prescaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.



TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	<u>Value</u> on MCLR and WDT Reset
N/A	OPTION	—	—	Tosc	Tose	PSA	PS2	PS1	PS0	11 1111	11 1111

Legend: u = unchanged, - = unimplemented, read as '0'. Shaded cells not used by Watchdog Timer.

11.13 PICDEM 3 Low Cost PIC16CXXX Demonstration Board

The PICDEM 3 demonstration board is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with an LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 3 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer with an adapter socket, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 3 demonstration board to test firmware. A prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM 3 demonstration board is a LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM 3 demonstration board provides an additional RS-232 interface and Windows software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

11.14 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included and the user may erase it and program it with the other sample programs using the PRO MATE II device programmer, or the PICSTART Plus development programmer, and easily debug and test the sample code. In addition, the PICDEM 17 demonstration board supports downloading of programs to and executing out of external FLASH memory on board. The PICDEM 17 demonstration board is also usable with the MPLAB ICE in-circuit emulator, or the PICMASTER emulator and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

11.15 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchip's HCS Secure Data Products. The HCS evaluation kit includes a LCD display to show changing codes, a decoder to decode transmissions and a programming interface to program test transmitters.



FIGURE 14-22: PORTA, B AND C IOL vs. VoL, VDD = 5 V



15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04 PIC16LC54A-04I (Commercial, Industrial)				$\begin{array}{llllllllllllllllllllllllllllllllllll$					
PIC16C54A-04, 10, 20 PIC16C54A-04I, 10I, 20I (Commercial, Industrial)				$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$					
Param No.	Symbol	Characteristic/Device	Min Typ† Max Units Conditions						
	IPD	Power-down Current ⁽²⁾							
D006		PIC16LC5X	—	2.5	12	μΑ	VDD = 2.5V, WDT enabled, Commercial		
			—	0.25	4.0	μΑ	VDD = 2.5V, WDT disabled, Commercial		
			_	0.25	5.0	μΑ μΑ	VDD = 2.5V, WDT enabled, industrial $VDD = 2.5V$, WDT disabled, Industrial		
D006A		PIC16C5X	_	4.0	12	μΑ	VDD = 3.0V, WDT enabled, Commercial		
			—	0.25	4.0	μA	VDD = 3.0V, WDT disabled, Commercial		
			—	5.0	14	μΑ	VDD = 3.0V, WDT enabled, Industrial		
				0.3	5.0	μA	$v \Box U = 3.0v, v U T uisabled, industrial$		

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

- a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/ disabled as specified.
- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.
- 3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in k Ω .



FIGURE 15-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A

TABLE 15-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A

AC Chara	cteristics	Standard Operating Condition Operating Temperature 0 -40 -20 -40	n s (unle)°C ≤ TA)°C ≤ TA)°C ≤ TA)°C ≤ TA	ess othe ≤ +70° ≤ +85° ≤ +85° ≤ +85° ≤ +125	erwise s C for co C for ind C for ind °C for e	specifie mmercia dustrial dustrial - extended	e d) al - PIC16LV54A-02I d
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	100* 1			ns μs	VDD = 5.0V VDD = 5.0V (PIC16LV54A only)
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from MCLR Low			100* 1μs	ns —	(PIC16LV54A only)

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.









FIGURE 16-12: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 PF, 25°C)

FIGURE 16-13: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 PF, -40°C to +85°C)



FIGURE 16-18: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD



FIGURE 16-19:

TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD



TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Chara	cteristics	Standard Operating ConditionsOperating Temperature0°C-40°C-40°C-40°C-40°C	(unle C ≤ TA : C ≤ TA : C ≤ TA : C ≤ TA :	ss other\ ≤ +70°C f ≤ +85°C f ≤ +125°C	wise sp or com or indu for exte	ecifiec mercial strial ended	1)
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions
2	Тсу	Instruction Cycle Time ⁽²⁾	—	4/Fosc			
3	TosL, TosH	Clock in (OSC1) Low or High	50*		_	ns	XT oscillator
		Time	20*	—	_	ns	HS oscillator
			2.0*	—	_	μS	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall	-		25*	ns	XT oscillator
		Time	—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

- * These parameters are characterized but not tested.
- † Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- **Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

PIC16C5X

FIGURE 18-10: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (IN XT, HS AND LP MODES) vs. VDD







FIGURE 19-6: TIMER0 CLOCK TIMINGS - PIC16C5X-40



TABLE 19-4: TIMER0 CLOCK REQUIREMENTS PIC16C5X-40

A	AC Charac	teristics Standard Operatin Operating Tempera	ng Conditions (u ature 0°C \leq TA	inless ∖ ≤ +70°	otherv °C for	vise sp comme	ecified) rcial
Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width					
		- No Prescaler	0.5 Tcy + 20*	—	—	ns	
		- With Prescaler	10*	_	_	ns	
41	Tt0L	T0CKI Low Pulse Width					
		- No Prescaler	0.5 Tcy + 20*	—	—	ns	
		- With Prescaler	10*	_	-	ns	
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> * N	_	_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

21.0 PACKAGING INFORMATION

21.1 Package Marketing Information

18-Lead PDIP



28-Lead Skinny PDIP (.300")



28-Lead PDIP (.600")



18-Lead SOIC



28-Lead SOIC



20-Lead SSOP



28-Lead SSOP





Example



Example



Example



Example



Example



Example



18-Lead Plastic Small Outline (SO) - Wide, 300 mil (SOIC)

For the most current package drawings, please see the Microchip Packaging Specification located Note: at http://www.microchip.com/packaging



	Units	INCHES*		MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	р		.050			1.27	
Overall Height	Α	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	¢	0	4	8	0	4	8
Lead Thickness	С	.009	.011	.012	0.23	0.27	0.30
Lead Width	В	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-013 Drawing No. C04-051

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