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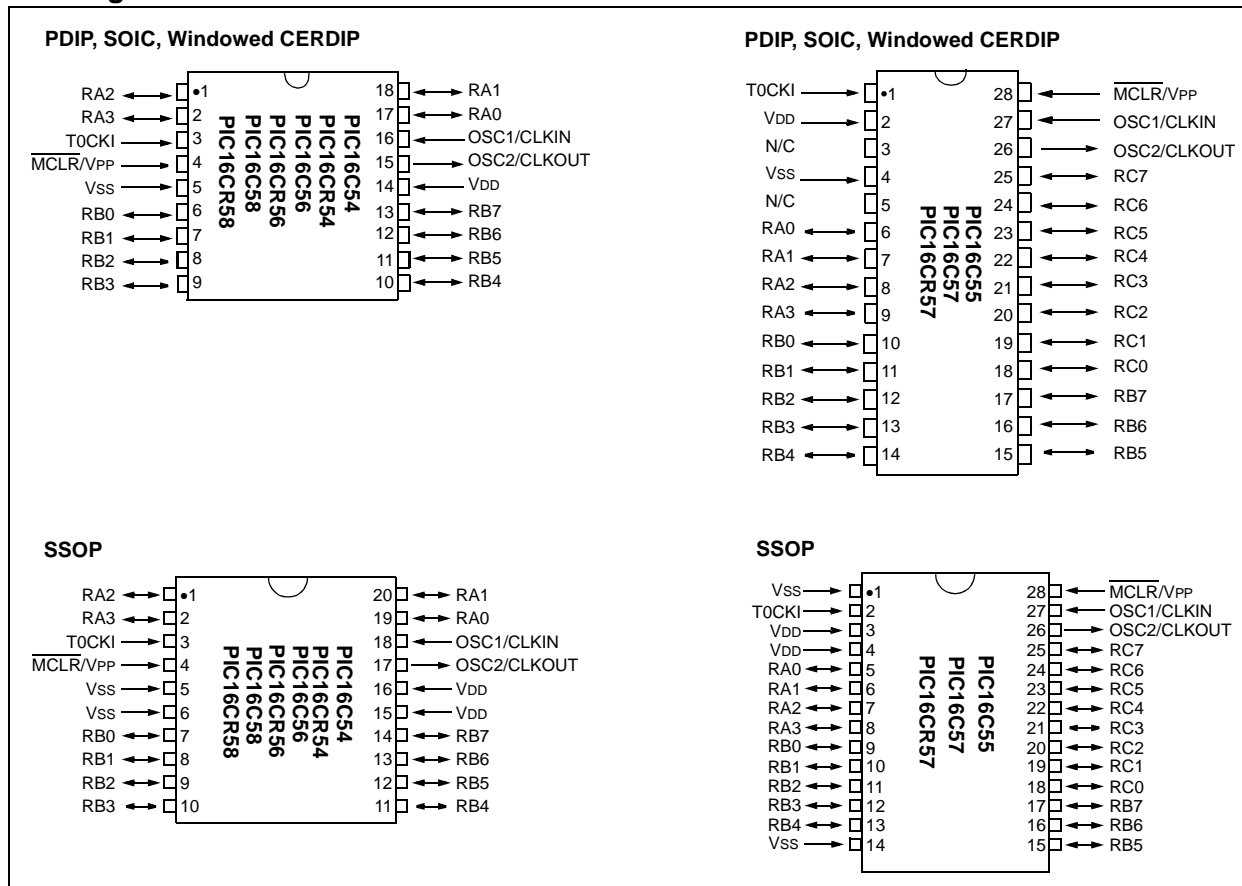
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 6.25V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c54-lpi-so

PIC16C5X

Pin Diagrams



Device Differences

Device	Voltage Range	Oscillator Selection (Program)	Oscillator	Process Technology (Microns)	ROM Equivalent	MCLR Filter
PIC16C54	2.5-6.25	Factory	See Note 1	1.2	PIC16CR54A	No
PIC16C54A	2.0-6.25	User	See Note 1	0.9	—	No
PIC16C54C	2.5-5.5	User	See Note 1	0.7	PIC16CR54C	Yes
PIC16C55	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C55A	2.5-5.5	User	See Note 1	0.7	—	Yes
PIC16C56	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C56A	2.5-5.5	User	See Note 1	0.7	PIC16CR56A	Yes
PIC16C57	2.5-6.25	Factory	See Note 1	1.2	—	No
PIC16C57C	2.5-5.5	User	See Note 1	0.7	PIC16CR57C	Yes
PIC16C58B	2.5-5.5	User	See Note 1	0.7	PIC16CR58B	Yes
PIC16CR54A	2.5-6.25	Factory	See Note 1	1.2	N/A	Yes
PIC16CR54C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR56A	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR57C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR58B	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

Note: The table shown above shows the generic names of the PIC16C5X devices. For device varieties, please refer to Section 2.0.

PIC16C5X

FIGURE 3-1: PIC16C5X SERIES BLOCK DIAGRAM

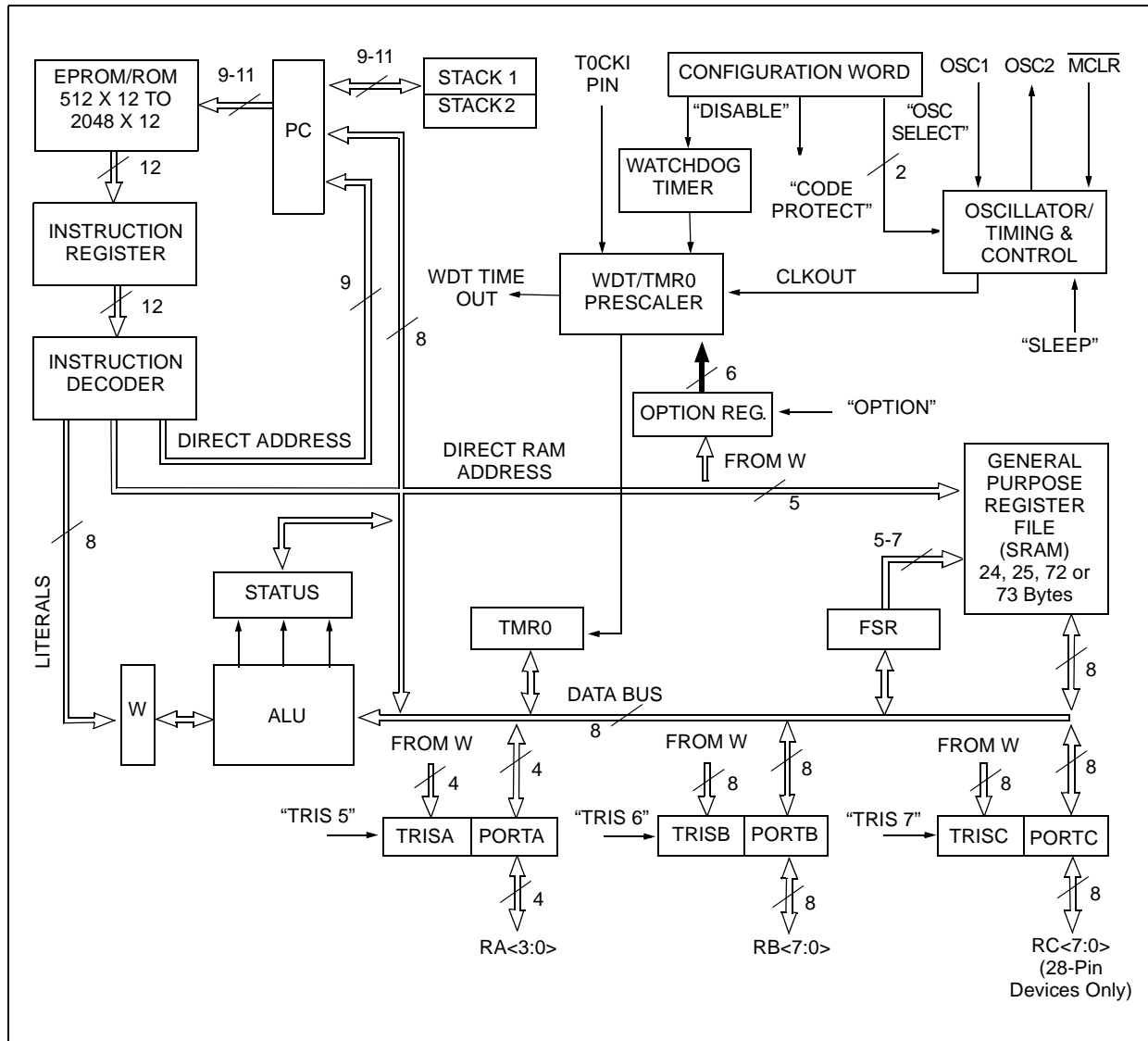


TABLE 3-1: PINOUT DESCRIPTION - PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58, PIC16CR58

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	DIP	SOIC	SSOP			
RA0	17	17	19	I/O	TTL	Bi-directional I/O port
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RB0	6	6	7	I/O	TTL	Bi-directional I/O port
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	
RB5	11	11	12	I/O	TTL	
RB6	12	12	13	I/O	TTL	
RB7	13	13	14	I/O	TTL	
T0CKI	3	3	3	I	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in use, to reduce current consumption.
MCLR/VPP	4	4	4	I	ST	Master clear (RESET) input/programming voltage input. This pin is an active low RESET to the device. Voltage on the MCLR/VPP pin must not exceed VDD to avoid unintended entering of Programming mode.
OSC1/CLKIN	16	16	18	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
VDD	14	14	15,16	P	—	Positive supply for logic and I/O pins.
Vss	5	5	5,6	P	—	Ground reference for logic and I/O pins.

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

PIC16C5X

FIGURE 5-3: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO VDD)

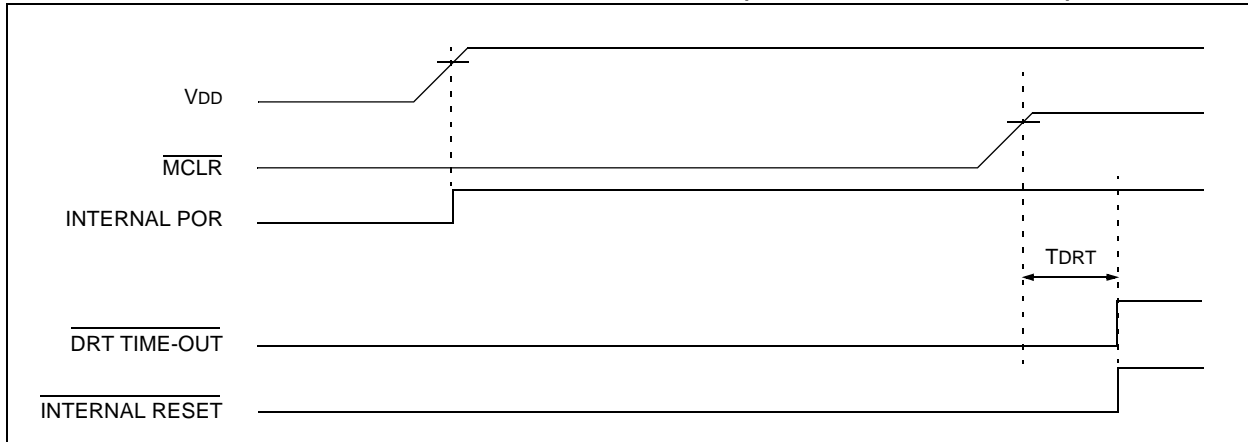


FIGURE 5-4: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO VDD): FAST VDD RISE TIME

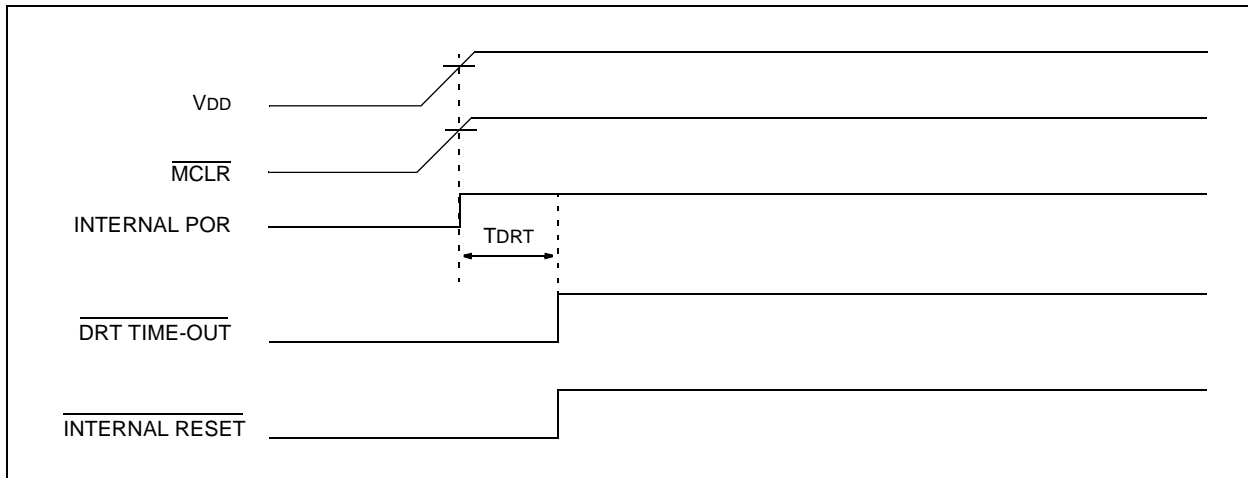
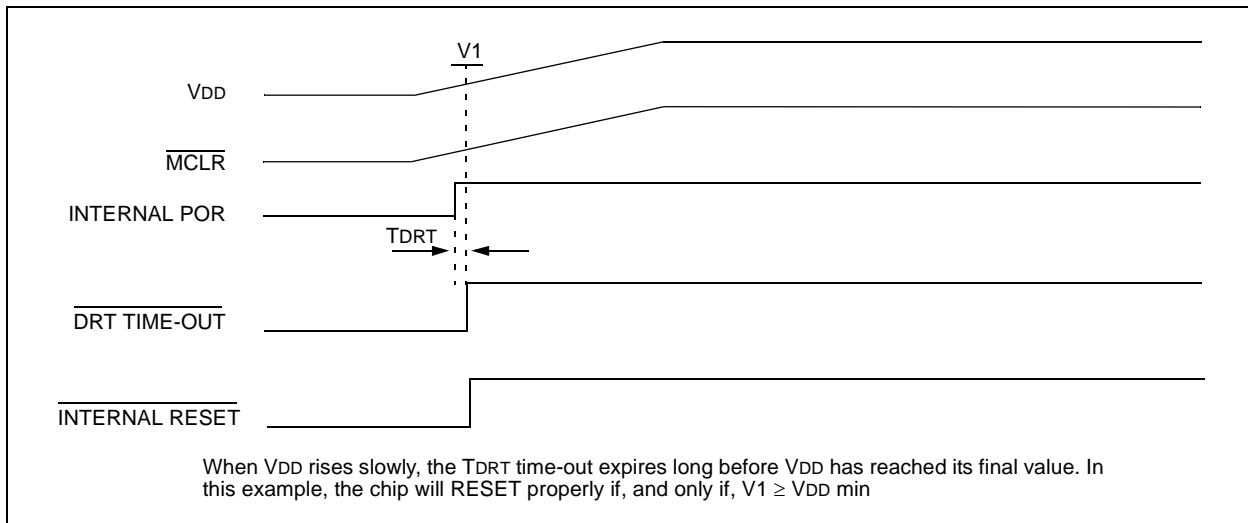


FIGURE 5-5: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO VDD): SLOW VDD RISE TIME



6.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the \overline{TO} and \overline{PD} bits are not

writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS Register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 10.0, Instruction Set Summary.

REGISTER 6-1: STATUS REGISTER (ADDRESS: 03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
PA2	PA1	PA0	\overline{TO}	\overline{PD}	Z	DC	C
bit 7			bit 0				

bit 7: **PA2:** This bit unused at this time.

Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

bit 6-5: **PA<1:0>:** Program page preselect bits (PIC16C56/CR56)(PIC16C57/CR57)(PIC16C58/CR58)

00 = Page 0 (000h - 1FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58

01 = Page 1 (200h - 3FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58

10 = Page 2 (400h - 5FFh) - PIC16C57/CR57, PIC16C58/CR58

11 = Page 3 (600h - 7FFh) - PIC16C57/CR57, PIC16C58/CR58

Each page is 512 words.

Using the PA<1:0> bits as general purpose read/write bits in devices which do not use them for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: **\overline{TO} :** Time-out bit

1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction

0 = A WDT time-out occurred

bit 3: **\overline{PD} :** Power-down bit

1 = After power-up or by the `CLRWDT` instruction

0 = By execution of the `SLEEP` instruction

bit 2: **Z:** Zero bit

1 = The result of an arithmetic or logic operation is zero

0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC:** Digit carry/borrow bit (for `ADDWF` and `SUBWF` instructions)

ADDWF

1 = A carry from the 4th low order bit of the result occurred

0 = A carry from the 4th low order bit of the result did not occur

SUBWF

1 = A borrow from the 4th low order bit of the result did not occur

0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C:** Carry/borrow bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

ADDWF

1 = A carry occurred

0 = A carry did not occur

SUBWF

1 = A borrow did not occur

0 = A borrow occurred

RRF or RLF

Loaded with LSb or MSb, respectively

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

1 = bit is set

0 = bit is cleared

x = bit is unknown

7.6 I/O Programming Considerations

7.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 7-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

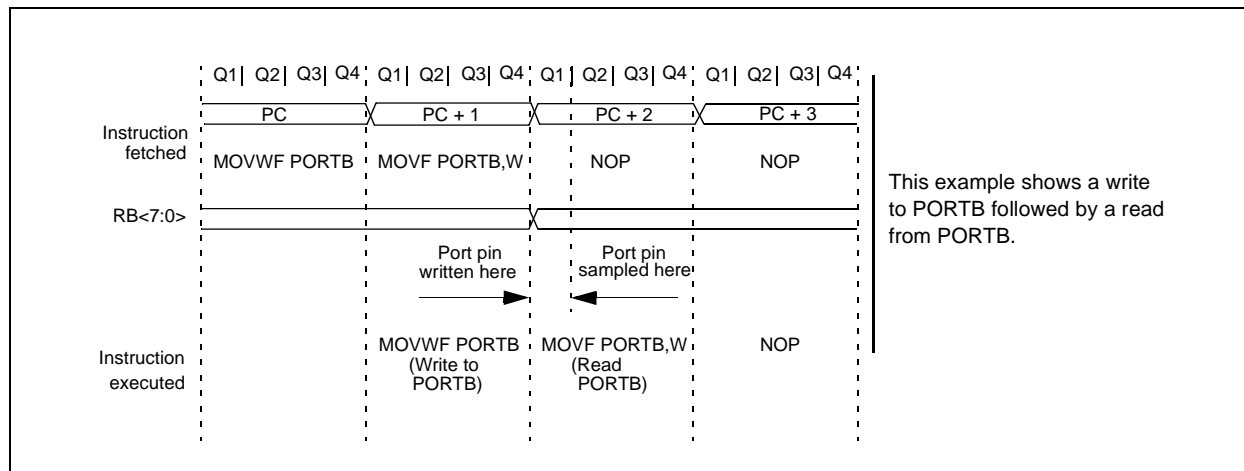
EXAMPLE 7-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                                PORT latch  PORT pins
;                                -----
BCF  PORTB, 7  ;01pp pppp  11pp pppp
BCF  PORTB, 6  ;10pp pppp  11pp pppp
MOVLW H'3F'    ;
TRIS  PORTB    ;10pp pppp  10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

7.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 7-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 7-2: SUCCESSIVE I/O OPERATION



MOVWF Move W to f

Syntax: [*label*] MOVWF f
 Operands: $0 \leq f \leq 31$
 Operation: $(W) \rightarrow (f)$
 Status Affected: None
 Encoding:

0000	001f	ffff
------	------	------

 Description: Move data from the W register to register 'f'.
 Words: 1
 Cycles: 1
 Example: MOVWF TEMP_REG

Before Instruction
 TEMP_REG = 0xFF
 W = 0x4F
 After Instruction
 TEMP_REG = 0x4F
 W = 0x4F

NOP No Operation

Syntax: [*label*] NOP
 Operands: None
 Operation: No operation
 Status Affected: None
 Encoding:

0000	0000	0000
------	------	------

 Description: No operation.
 Words: 1
 Cycles: 1
 Example: NOP

OPTION Load OPTION Register

Syntax: [*label*] OPTION
 Operands: None
 Operation: $(W) \rightarrow \text{OPTION}$
 Status Affected: None
 Encoding:

0000	0000	0010
------	------	------

 Description: The content of the W register is loaded into the OPTION register.
 Words: 1
 Cycles: 1
 Example: OPTION

Before Instruction
 W = 0x07
 After Instruction
 OPTION = 0x07

RETLW Return with Literal in W

Syntax: [*label*] RETLW k
 Operands: $0 \leq k \leq 255$
 Operation: $k \rightarrow (W)$;
 TOS \rightarrow PC
 Status Affected: None
 Encoding:

1000	kkkk	kkkk
------	------	------

 Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
 Words: 1
 Cycles: 2
 Example: CALL TABLE ;W contains
 ;table offset
 ;value.
 • ;W now has table
 • ;value.
 TABLE •
 ADDWF PC ;W = offset
 RETLW k1 ;Begin table
 RETLW k2 ;
 •
 •
 •
 RETLW kn ; End of table

Before Instruction
 W = 0x07
 After Instruction
 W = value of k8

PIC16C5X

RLF Rotate Left f through Carry

Syntax: [*label*] RLF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

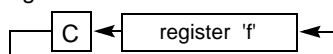
Operation: See description below

Status Affected: C

Encoding:

0011	01df	ffff
------	------	------

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example: RLF REG1,0

Before Instruction

REG1 = 1110 0110

C = 0

After Instruction

REG1 = 1110 0110

W = 1100 1100

C = 1

RRF Rotate Right f through Carry

Syntax: [*label*] RRF f,d

Operands: $0 \leq f \leq 31$
 $d \in [0,1]$

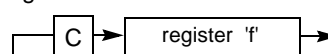
Operation: See description below

Status Affected: C

Encoding:

0011	00df	ffff
------	------	------

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Example: RRF REG1,0

Before Instruction

REG1 = 1110 0110

C = 0

After Instruction

REG1 = 1110 0110

W = 0111 0011

C = 0

SLEEP Enter SLEEP Mode

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT;
 0 → WDT prescaler; if assigned
 1 → \overline{TO} ;
 0 → \overline{PD}

Status Affected: \overline{TO} , \overline{PD}

Encoding:

0000	0000	0011
------	------	------

Description: Time-out status bit (\overline{TO}) is set. The power-down status bit (\overline{PD}) is cleared. The WDT and its prescaler are cleared.
 The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example: SLEEP

PIC16C5X

13.2 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

PIC16CR54A-04E, 10E, 20E (Extended)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage RC, XT and LP modes HS mode	3.25	—	6.0	V	
			4.5	—	5.5	V	
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	VDD Rise Rate to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	Supply Current ⁽²⁾ RC ⁽³⁾ and XT modes HS mode HS mode	—	1.8	3.3	mA	FOSC = 4.0 MHz, VDD = 5.5V
			—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
			—	9.0	20	mA	FOSC = 16 MHz, VDD = 5.5V
D020	IPD	Power-down Current ⁽²⁾	—	5.0	22	μA	VDD = 3.25V, WDT enabled
			—	0.8	18	μA	VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2R_{EXT}$ (mA) with REXT in kΩ.

13.5 Timing Parameter Symbolology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T	T
F Frequency	T Time

Lowercase letters (pp) and their meanings:

pp	mc MCLR
2 to	osc oscillator
ck CLKOUT	os OSC1
cy cycle time	t0 T0CKI
drt device reset timer	wdt watchdog timer
io I/O port	

Uppercase letters and their meanings:

S	P Period
F Fall	R Rise
H High	V Valid
I Invalid (Hi-impedance)	Z Hi-impedance
L Low	

FIGURE 13-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16CR54A

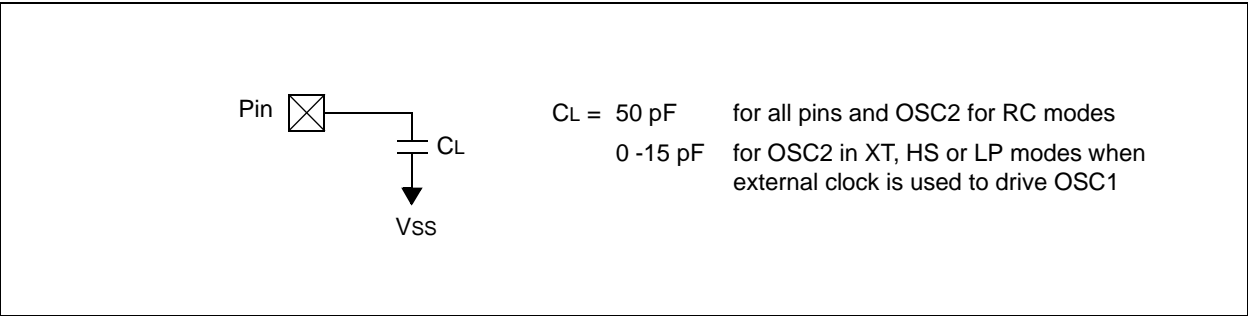


FIGURE 14-9: V_{TH} (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. V_{DD}

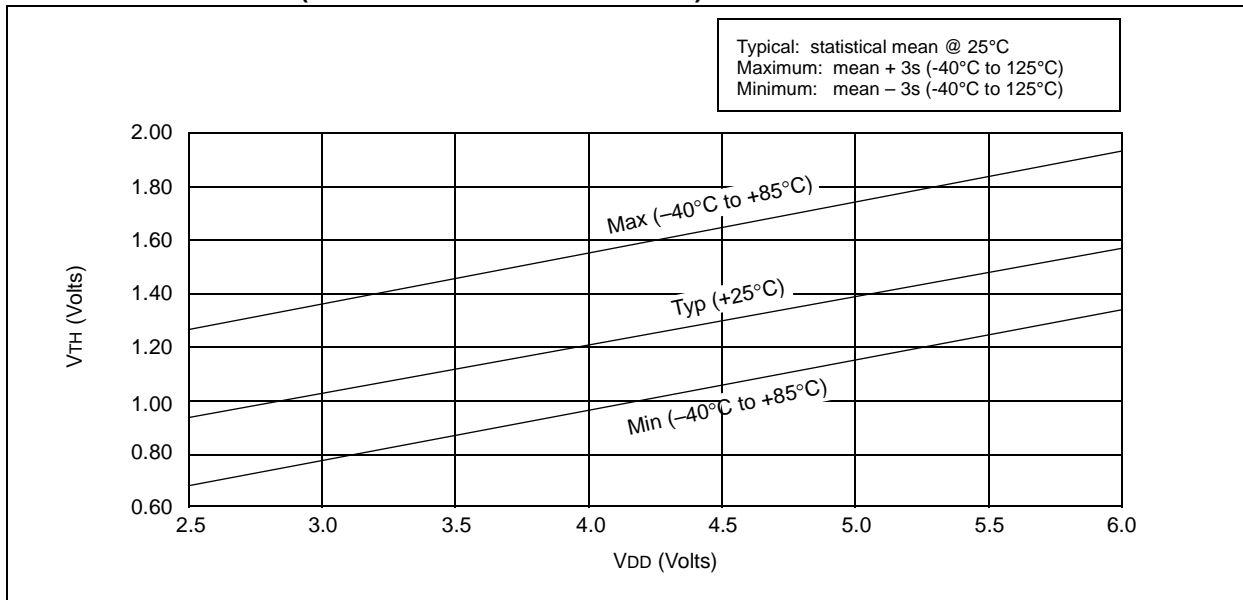
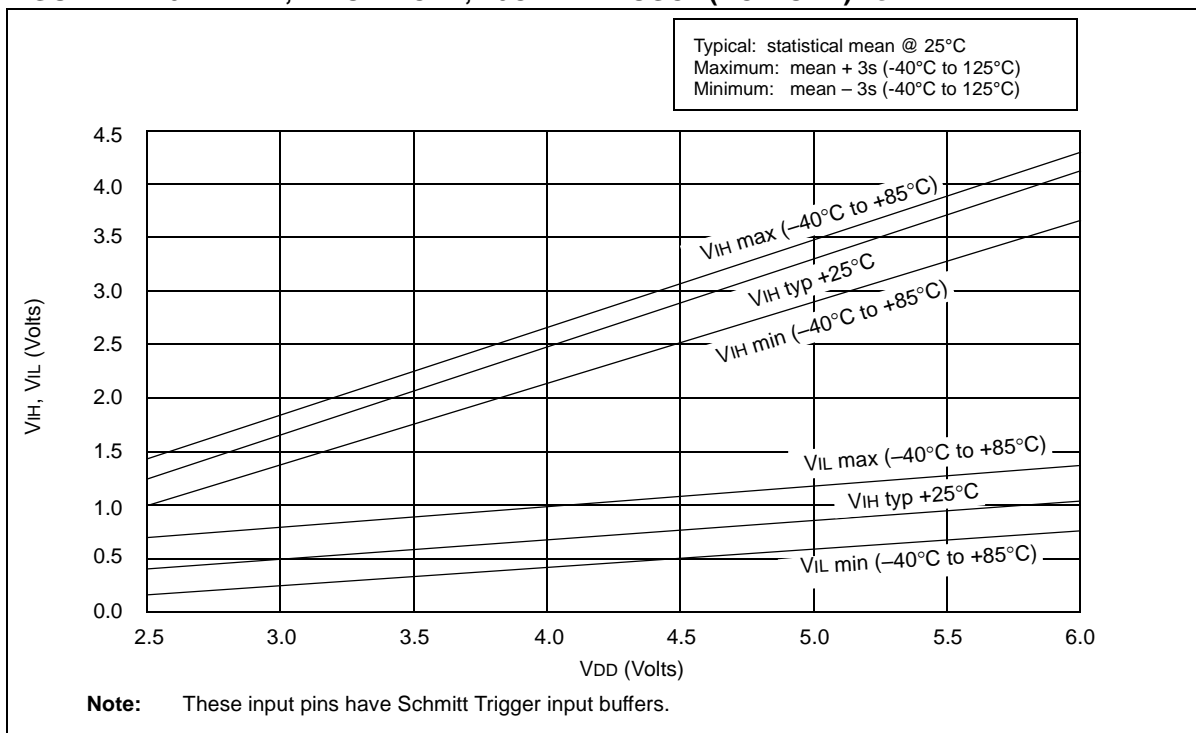


FIGURE 14-10: V_{IH} , V_{IL} OF MCLR, T0CKI AND OSC1 (RC MODE) vs. V_{DD}



15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial) PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial)

PIC16LC54A-04 PIC16LC54A-04I (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
PIC16C54A-04, 10, 20 PIC16C54A-04I, 10I, 20I (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
D006	IPD	Power-down Current ⁽²⁾ PIC16LC5X	—	2.5	12	μA	V _{DD} = 2.5V, WDT enabled, Commercial
				0.25	4.0	μA	V _{DD} = 2.5V, WDT disabled, Commercial
				2.5	14	μA	V _{DD} = 2.5V, WDT enabled, Industrial
				0.25	5.0	μA	V _{DD} = 2.5V, WDT disabled, Industrial
D006A		PIC16C5X	—	4.0	12	μA	V _{DD} = 3.0V, WDT enabled, Commercial
				0.25	4.0	μA	V _{DD} = 3.0V, WDT disabled, Commercial
				5.0	14	μA	V _{DD} = 3.0V, WDT enabled, Industrial
				0.3	5.0	μA	V _{DD} = 3.0V, WDT disabled, Industrial

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all I_{DD} measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS}, T_{OCKI} = V_{DD}, MCLR = V_{DD}; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through R_{EXT}. The current through the resistor can be estimated by the formula: I_R = V_{DD}/2R_{EXT} (mA) with R_{EXT} in kΩ.

FIGURE 15-3: CLKOUT AND I/O TIMING - PIC16C54A

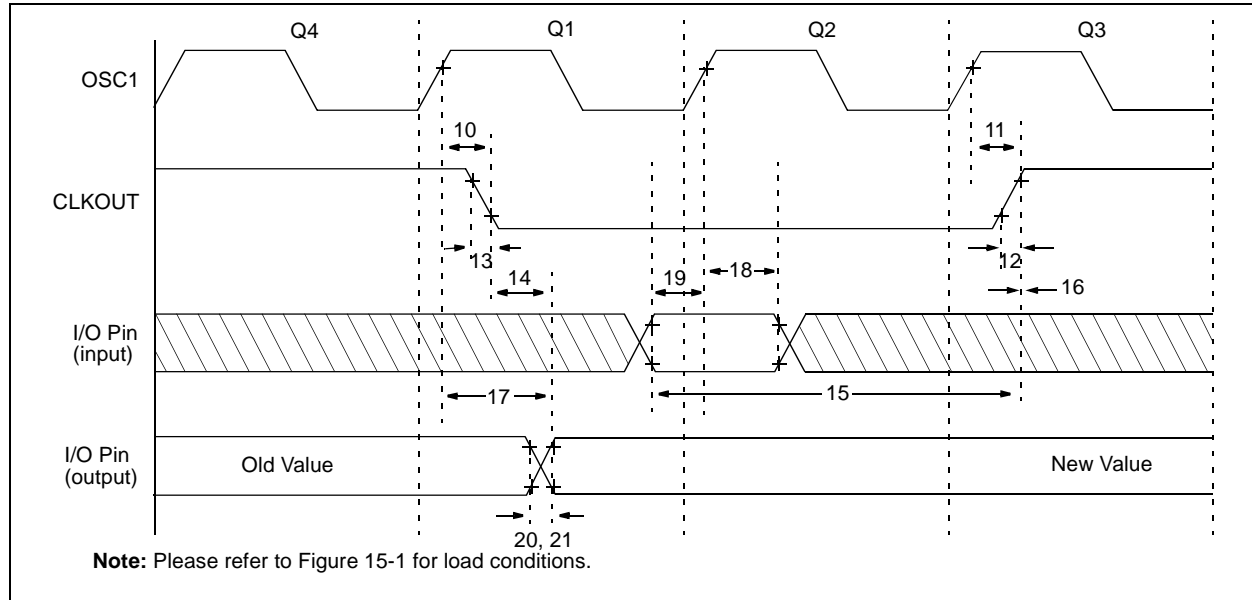


TABLE 15-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54A

Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-20^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial - PIC16LV54A-02I $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended						
AC Characteristics						
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽¹⁾	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽¹⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽¹⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽¹⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽¹⁾	$0.25 \text{ TCY} + 30^*$	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ ⁽¹⁾	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽²⁾	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽²⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽²⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

2: Please refer to Figure 15-1 for load conditions.

FIGURE 16-16: WDT TIMER TIME-OUT PERIOD vs. VDD⁽¹⁾

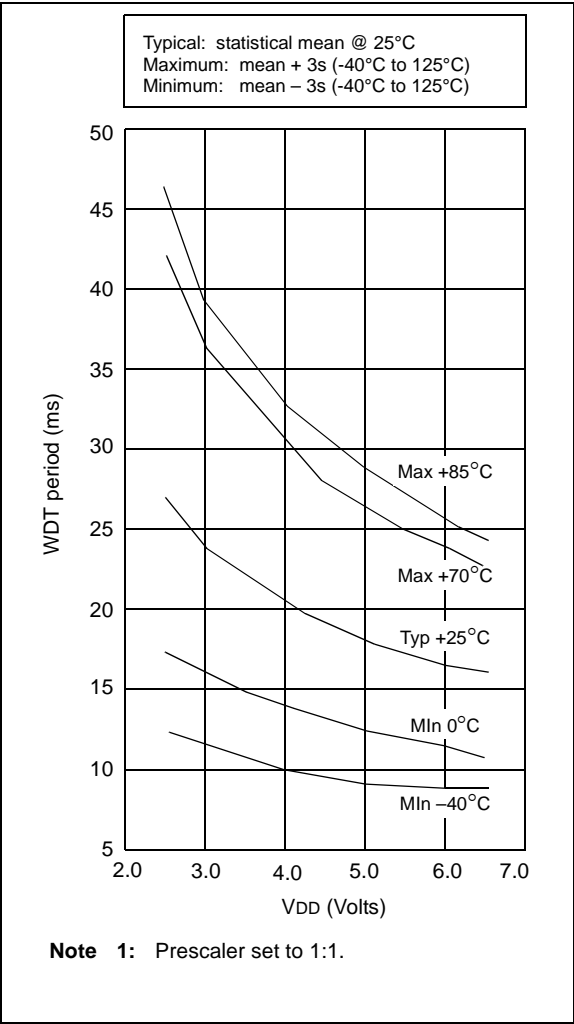
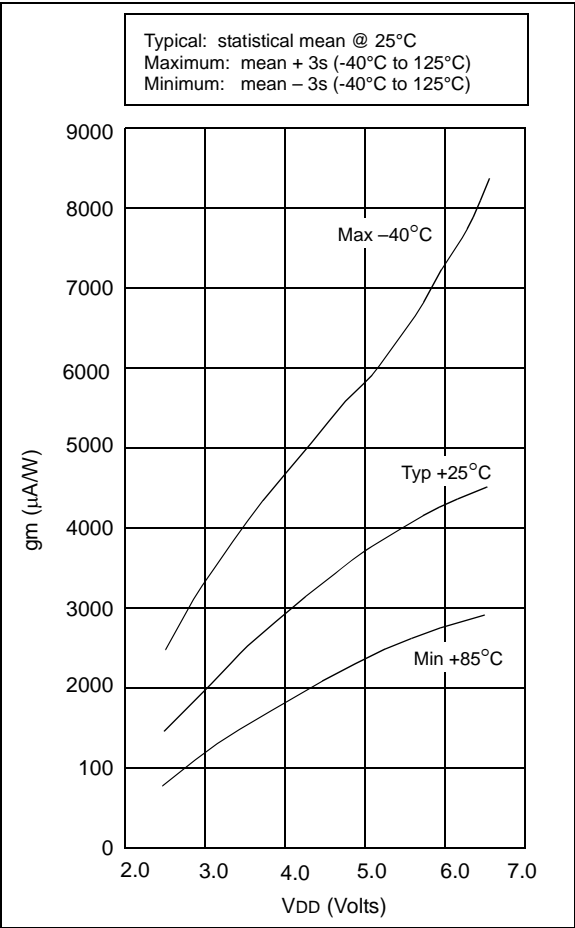


FIGURE 16-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD



PIC16C5X

17.5 Timing Diagrams and Specifications

FIGURE 17-6: EXTERNAL CLOCK TIMING - PIC16C5X, PIC16CR5X

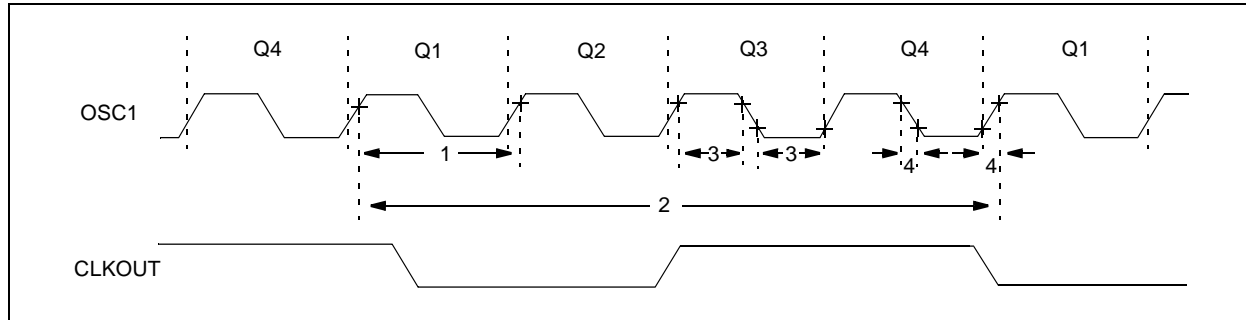


TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended							
AC Characteristics							
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency ⁽¹⁾	DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency ⁽¹⁾	DC	—	4.0	MHz	RC osc mode
			0.45	—	4.0	MHz	XT osc mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	20	MHz	HS osc mode (20)
			5.0	—	200	kHz	LP osc mode
1	TOSC	External CLKIN Period ⁽¹⁾	250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	μs	LP osc mode
		Oscillator Period ⁽¹⁾	250	—	—	ns	RC osc mode
			250	—	2,200	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	μs	LP osc mode

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 18-16: PORTA, B AND C I_{OH} vs. V_{OH} , $V_{DD} = 5\text{ V}$

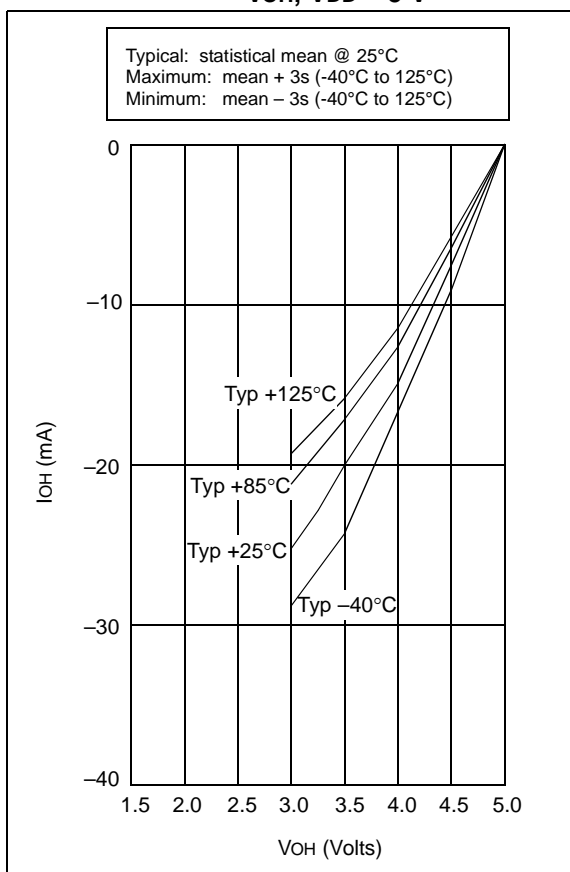
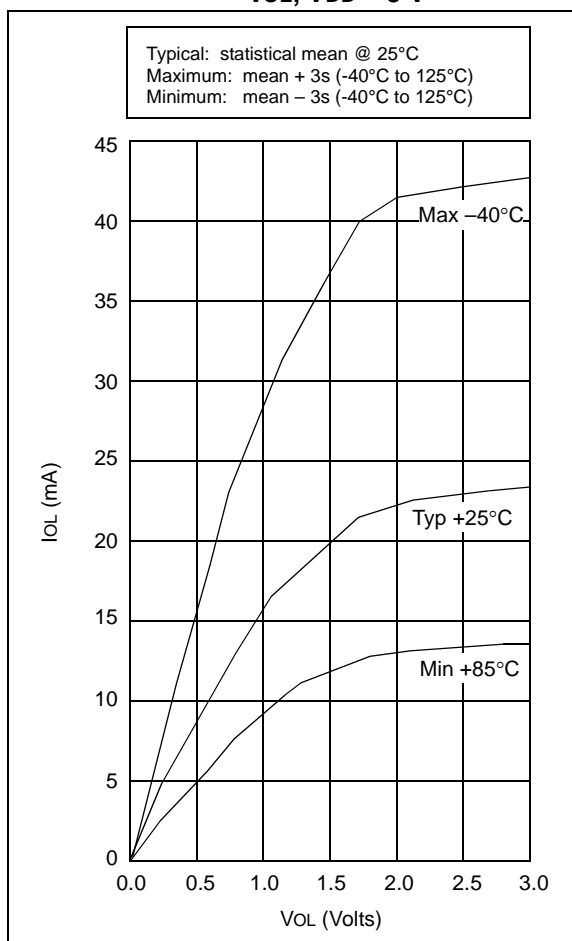


FIGURE 18-17: PORTA, B AND C I_{OL} vs. V_{OL} , $V_{DD} = 3\text{ V}$



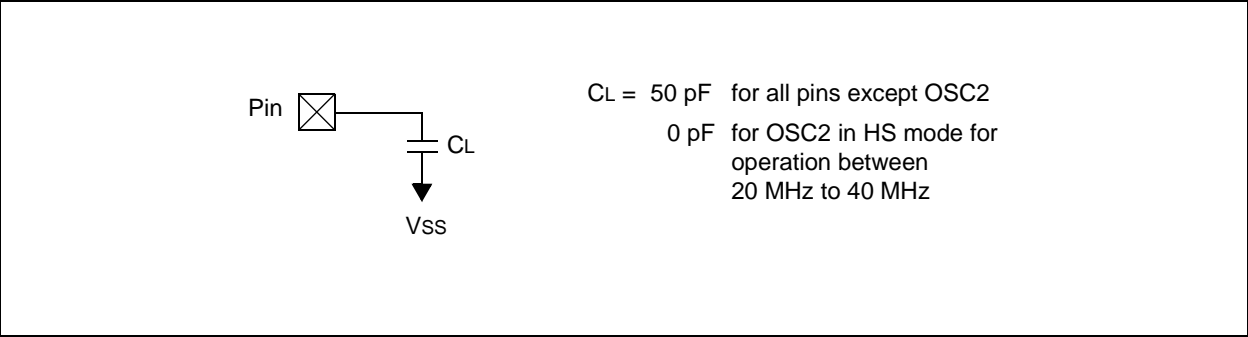
19.3 Timing Parameter Symbolology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

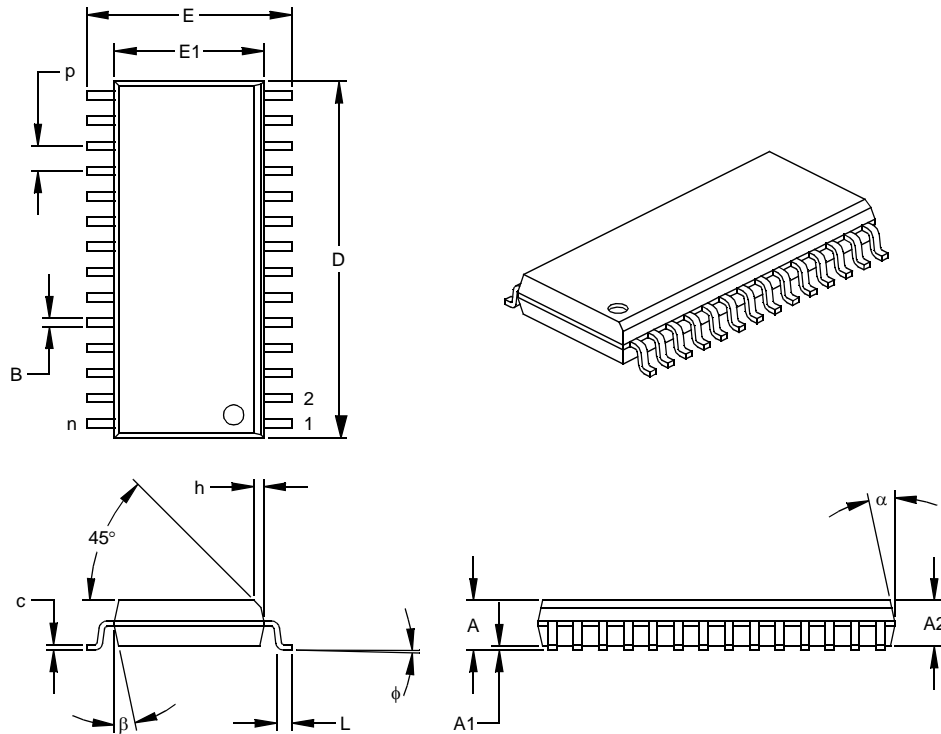
T		T	Time
F	Frequency		
Lowercase letters (pp) and their meanings:			
pp		mc	MCLR
2	to	osc	oscillator
ck	CLKOUT	os	OSC1
cy	cycle time	t0	T0CKI
drt	device reset timer	wdt	watchdog timer
io	I/O port		
Uppercase letters and their meanings:			
S		P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	Hi-impedance
L	Low		

FIGURE 19-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54C/C55A/C56A/C57C/C58B-40



28-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59
Overall Length	D	.695	.704	.712	17.65	17.87	18.08
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle Top	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-013

Drawing No. C04-052

W

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X

XORLW 60
XORWF 60

Z

Zero (Z) bit 9, 29

