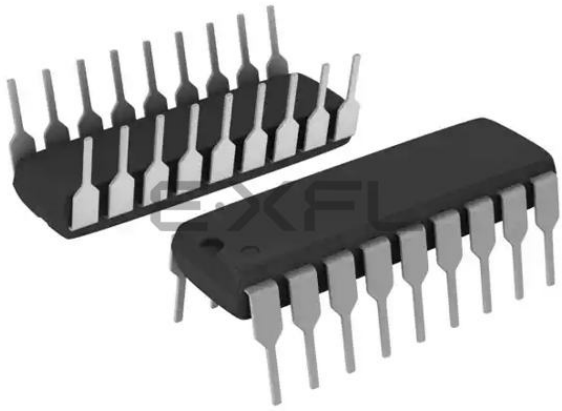

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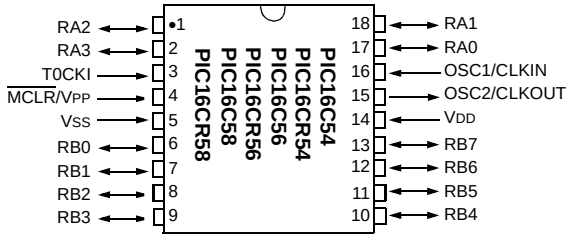
Applications of "Embedded - Microcontrollers"

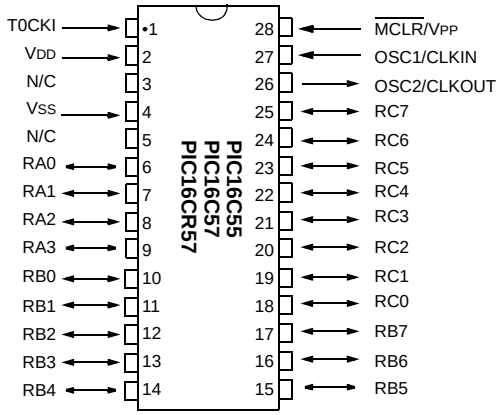
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c54a-04i-p

Pin Diagrams

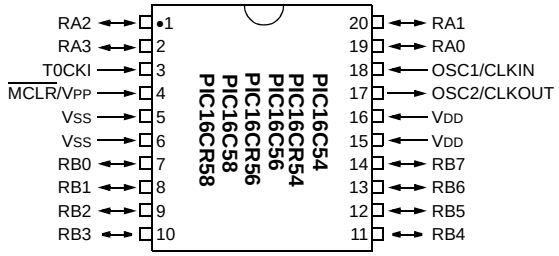
PDIP, SOIC, Windowed CERDIP



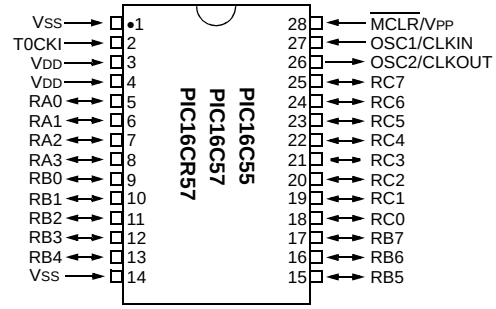
PDIP, SOIC, Windowed CERDIP



SSOP



SSOP



Device Differences

Device	Voltage Range	Oscillator Selection (Program)	Oscillator	Process Technology (Microns)	ROM Equivalent	$\overline{\text{MCLR}}$ Filter
PIC16C54	2.5-6.25	Factory	See **Note 1**	1.2	PIC16CR54A	No
PIC16C54A	2.0-6.25	User	See **Note 1**	0.9	—	No
PIC16C54C	2.5-5.5	User	See **Note 1**	0.7	PIC16CR54C	Yes
PIC16C55	2.5-6.25	Factory	See **Note 1**	1.7	—	No
PIC16C55A	2.5-5.5	User	See **Note 1**	0.7	—	Yes
PIC16C56	2.5-6.25	Factory	See **Note 1**	1.7	—	No
PIC16C56A	2.5-5.5	User	See **Note 1**	0.7	PIC16CR56A	Yes
PIC16C57	2.5-6.25	Factory	See **Note 1**	1.2	—	No
PIC16C57C	2.5-5.5	User	See **Note 1**	0.7	PIC16CR57C	Yes
PIC16C58B	2.5-5.5	User	See **Note 1**	0.7	PIC16CR58B	Yes
PIC16CR54A	2.5-6.25	Factory	See **Note 1**	1.2	N/A	Yes
PIC16CR54C	2.5-5.5	Factory	See **Note 1**	0.7	N/A	Yes
PIC16CR56A	2.5-5.5	Factory	See **Note 1**	0.7	N/A	Yes
PIC16CR57C	2.5-5.5	Factory	See **Note 1**	0.7	N/A	Yes
PIC16CR58B	2.5-5.5	Factory	See **Note 1**	0.7	N/A	Yes

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

Note: The table shown above shows the generic names of the PIC16C5X devices. For device varieties, please refer to Section 2.0.

TABLE 1-1: PIC16C5X FAMILY OF DEVICES

Features	PIC16C54	PIC16CR54	PIC16C55	PIC16C56	PIC16CR56
Maximum Operation Frequency	40 MHz	20 MHz	40 MHz	40 MHz	20 MHz
EPROM Program Memory (x12 words)	512	—	512	1K	—
ROM Program Memory (x12 words)	—	512	—	—	1K
RAM Data Memory (bytes)	25	25	24	25	25
Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0
I/O Pins	12	12	20	12	12
Number of Instructions	33	33	33	33	33
Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP
All PIC® Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.					

Features	PIC16C57	PIC16CR57	PIC16C58	PIC16CR58
Maximum Operation Frequency	40 MHz	20 MHz	40 MHz	20 MHz
EPROM Program Memory (x12 words)	2K	—	2K	—
ROM Program Memory (x12 words)	—	2K	—	2K
RAM Data Memory (bytes)	72	72	73	73
Timer Module(s)	TMR0	TMR0	TMR0	TMR0
I/O Pins	20	20	12	12
Number of Instructions	33	33	33	33
Packages	28-pin DIP, SOIC; 28-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP
All PIC® Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.				

TABLE 3-2: PINOUT DESCRIPTION - PIC16C55, PIC16C57, PIC16CR57

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	DIP	SOIC	SSOP			
RA0	6	6	5	I/O	TTL	Bi-directional I/O port
RA1	7	7	6	I/O	TTL	
RA2	8	8	7	I/O	TTL	
RA3	9	9	8	I/O	TTL	
RB0	10	10	9	I/O	TTL	Bi-directional I/O port
RB1	11	11	10	I/O	TTL	
RB2	12	12	11	I/O	TTL	
RB3	13	13	12	I/O	TTL	
RB4	14	14	13	I/O	TTL	
RB5	15	15	15	I/O	TTL	
RB6	16	16	16	I/O	TTL	
RB7	17	17	17	I/O	TTL	
RC0	18	18	18	I/O	TTL	Bi-directional I/O port
RC1	19	19	19	I/O	TTL	
RC2	20	20	20	I/O	TTL	
RC3	21	21	21	I/O	TTL	
RC4	22	22	22	I/O	TTL	
RC5	23	23	23	I/O	TTL	
RC6	24	24	24	I/O	TTL	
RC7	25	25	25	I/O	TTL	
T0CKI	1	1	2	I	ST	Clock input to Timer0. Must be tied to V_{SS} or V_{DD}, if not in use, to reduce current consumption.
$\overline{MCLR}$	28	28	28	I	ST	Master clear (RESET) input. This pin is an active low RESET to the device.
OSC1/CLKIN	27	27	27	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	26	26	26	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
V_{DD}	2	2	3,4	P	—	Positive supply for logic and I/O pins.
V_{SS}	4	4	1,14	P	—	Ground reference for logic and I/O pins.
N/C	3,5	3,5	—	—	—	Unused, do not connect.

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2 and Example 3-1.

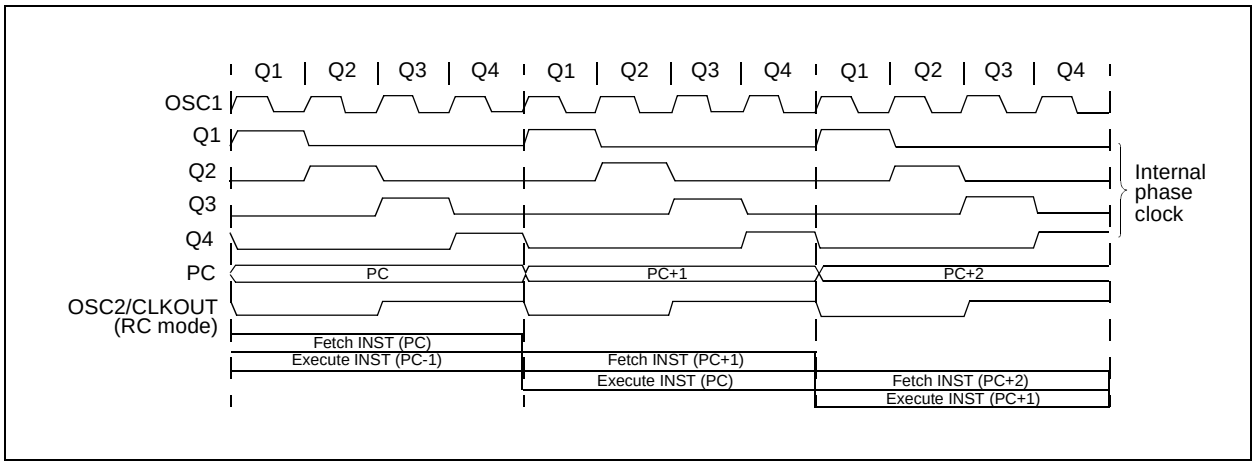
3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., `GOTO`), then two cycles are required to complete the instruction (Example 3-1).

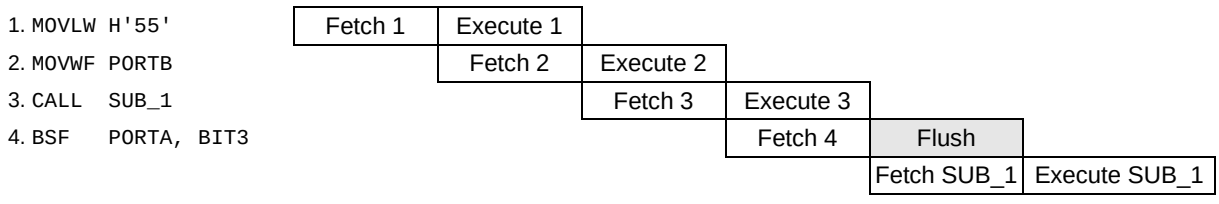
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is “flushed” from the pipeline, while the new instruction is being fetched and then executed.

5.2 Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides an 18 ms nominal time-out on RESET regardless of Oscillator mode used. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows VDD to rise above VDD min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after the voltage on the MCLR/VPP pin has reached a logic high (VIH) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The Device Reset time delay will vary from chip to chip due to VDD, temperature, and process variation. See AC parameters for details.

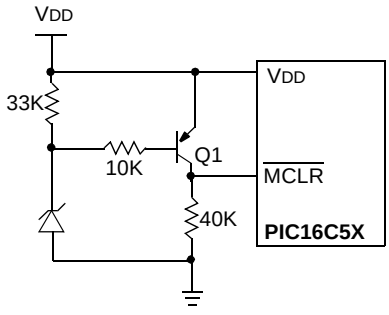
The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the PIC16C5X from SLEEP mode automatically.

5.3 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be RESET in the event of a brown-out.

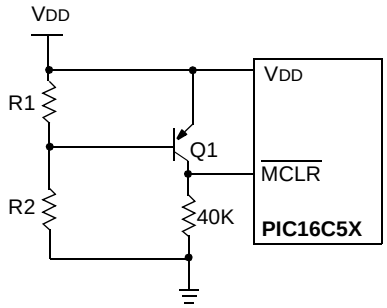
To RESET PIC16C5X devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 5-6, Figure 5-7 and Figure 5-8.

FIGURE 5-6: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate RESET when VDD goes below Vz + 0.7V (where Vz = Zener voltage).

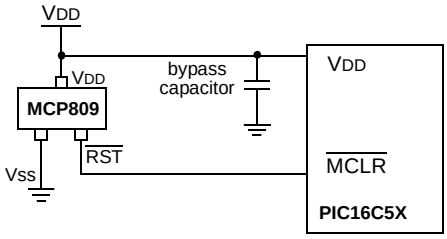
FIGURE 5-7: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \cdot \frac{R1}{R1 + R2} = 0.7V$$

FIGURE 5-8: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX families of supervisors provide push-pull and open collector outputs with both "active high and active low" RESET pins. There are 7 different trip point selections to accommodate 5V and 3V systems.

6.4 OPTION Register

The OPTION Register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the `OPTION` instruction, the contents of the W Register will be transferred to the OPTION Register. A RESET sets the OPTION<5:0> bits.

REGISTER 6-2: OPTION REGISTER

U-0	U-0	W-1	W-1	W-1	W-1	W-1	W-1
—	—	T0CS	TOSE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7-6: **Unimplemented**: Read as '0'

bit 5: **T0CS**: Timer0 clock source select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: Timer0 source edge select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3: **PSA**: Prescaler assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0: **PS<2:0>**: Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

REGISTER 9-2: CONFIGURATION WORD FOR PIC16C54/C55/C56/C57

—	—	—	—	—	—	—	—	CP	WDTE	FOSC1	FOSC0

bit 11 bit 0

bit 11-4: **Unimplemented**: Read as '0'

bit 3: **CP:** Code protection bit.
1 = Code protection off
0 = Code protection on

bit 2: **WDTE:** Watchdog timer enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator selection bits(2)
00 = LP oscillator
01 = XT oscillator
10 = HS oscillator
11 = RC oscillator

Note 1: Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.
2: PIC16LV54A supports XT, RC and LP oscillator only.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

12.5 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D030	VIL	**Input Low Voltage**					
		I/O ports	Vss	—	0.15 VDD	V	Pin at hi-impedance
		MCLR (Schmitt Trigger)	Vss	—	0.15 VDD	V	
		T0CKI (Schmitt Trigger)	Vss	—	0.15 VDD	V	
		OSC1 (Schmitt Trigger)	Vss	—	0.15 VDD	V	PIC16C5X-RC only(3)
		OSC1 (Schmitt Trigger)	Vss	—	0.3 VDD	V	PIC16C5X-XT, 10, HS, LP
D040	VIH	**Input High Voltage**					
		I/O ports	0.45 VDD	—	VDD	V	For all VDD(4)
		I/O ports	2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(4)
		I/O ports	0.36 VDD	—	VDD	V	VDD > 5.5 V
		MCLR (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		T0CKI (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		OSC1 (Schmitt Trigger)	0.85 VDD	—	VDD	V	PIC16C5X-RC only(3)
		OSC1 (Schmitt Trigger)	0.7 VDD	—	VDD	V	PIC16C5X-XT, 10, HS, LP
D050	VHYS	**Hysteresis of Schmitt Trigger inputs**	0.15 VDD*	—	—	V	
D060	IIL	**Input Leakage Current (1,2)**					**For VDD ≤ 5.5 V:**
		I/O ports	–1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
		MCLR	–5	—	—	µA	VPIN = VSS + 0.25V
		MCLR	—	0.5	+5	µA	VPIN = VDD
		T0CKI	–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
		OSC1	–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, 10, HS, LP
D080	VOL	**Output Low Voltage**					
		I/O ports	—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
		OSC2/CLKOUT	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC
D090	VOH	**Output High Voltage(2)**					
		I/O ports	VDD – 0.7	—	—	V	IOH = –5.4 mA, VDD = 4.5V
		OSC2/CLKOUT	VDD – 0.7	—	—	V	IOH = –1.0 mA, VDD = 4.5V, PIC16C5X-RC

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the $\overline{\text{MCLR}}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 **PIC16LCR54A-04I** (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
PIC16CR54A-04, 10, 20 **PIC16CR54A-04I, 10I, 20I** (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Symbol**	**Characteristic/Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**					
D001		PIC16LCR54A	2.0	—	6.25	V	
D001 D001A		PIC16CR54A	2.5 4.5	— —	6.25 5.5	V V	RC and XT modes HS mode
D002	VDR	**RAM Data Retention Voltage(1)**	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
	IDD	**Supply Current(2)**					
D005		PICLCR54A	— —	10 —	20 70	µA µA	Fosc = 32 kHz, VDD = 2.0V Fosc = 32 kHz, VDD = 6.0V
D005A		PIC16CR54A					**RC(3) and XT modes:**
			— — —	2.0 0.8 90	3.6 1.8 350	mA mA µA	FOSC = 4.0 MHz, VDD = 6.0V FOSC = 4.0 MHz, VDD = 3.0V FOSC = 200 kHz, VDD = 2.5V
							HS mode:
			— —	4.8 9.0	10 20	mA mA	FOSC = 10 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

14.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean – 3σ) respectively, where σ is a standard deviation, over the whole temperature range.

FIGURE 14-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

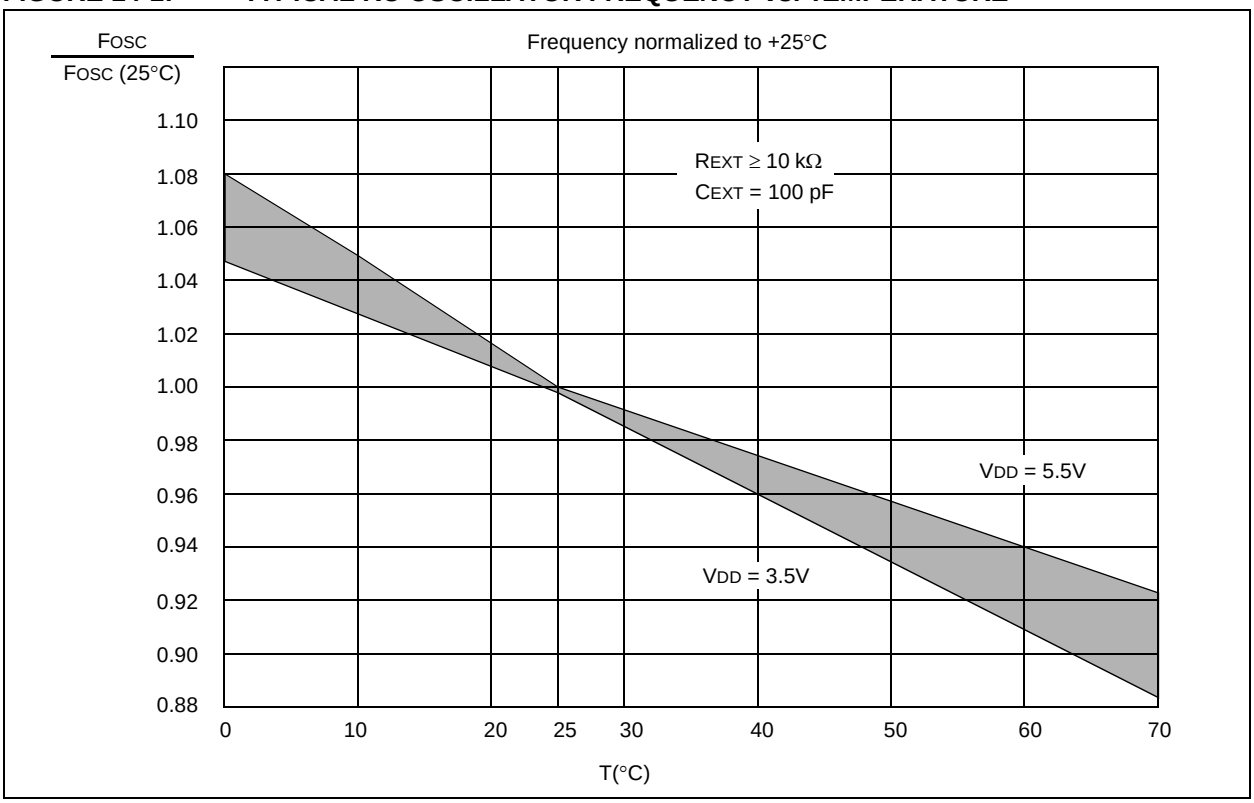


TABLE 14-1: RC OSCILLATOR FREQUENCIES

CEXT	REXT	Average FOSC @ 5 V, 25°C	
20 pF	3.3K	5 MHz	± 27%
	5K	3.8 MHz	± 21%
	10K	2.2 MHz	± 21%
	100K	262 kHz	± 31%
100 pF	3.3K	1.6 MHz	± 13%
	5K	1.2 MHz	± 13%
	10K	684 kHz	± 18%
	100K	71 kHz	± 25%
300 pF	3.3K	660 kHz	± 10%
	5.0K	484 kHz	± 14%
	10K	267 kHz	± 15%
	100K	29 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviations from the average value for VDD = 5V.

15.5 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T	
F Frequency	T Time

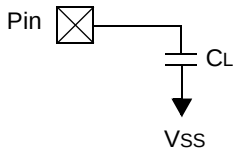
Lowercase letters (pp) and their meanings:

pp	
2 to	mc $\overline{\text{MCLR}}$
ck CLKOUT	osc oscillator
cy cycle time	os OSC1
drt device reset timer	t0 T0CKI
io I/O port	wdt watchdog timer

Uppercase letters and their meanings:

S	
F Fall	P Period
H High	R Rise
I Invalid (Hi-impedance)	V Valid
L Low	Z Hi-impedance

FIGURE 15-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54A



C_L = 50 pF for all pins and OSC2 for RC modes

0 -15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial –20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I –40°C ≤ TA ≤ +125°C for extended						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
1	TOSC	External CLKIN Period(1)	250	—	—	ns	XT OSC mode
			500	—	—	ns	XT OSC mode (PIC16LV54A)
			250	—	—	ns	HS OSC mode (04)
			100	—	—	ns	HS OSC mode (10)
			50	—	—	ns	HS OSC mode (20)
			5.0	—	—	µs	LP OSC mode
		Oscillator Period(1)	250	—	—	ns	RC OSC mode
			500	—	—	ns	RC OSC mode (PIC16LV54A)
			250	—	10,000	ns	XT OSC mode
			500	—	—	ns	XT OSC mode (PIC16LV54A)
			250	—	250	ns	HS OSC mode (04)
			100	—	250	ns	HS OSC mode (10)
			50	—	250	ns	HS OSC mode (20)
			5.0	—	200	µs	LP OSC mode
2	Tcy	Instruction Cycle Time(2)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

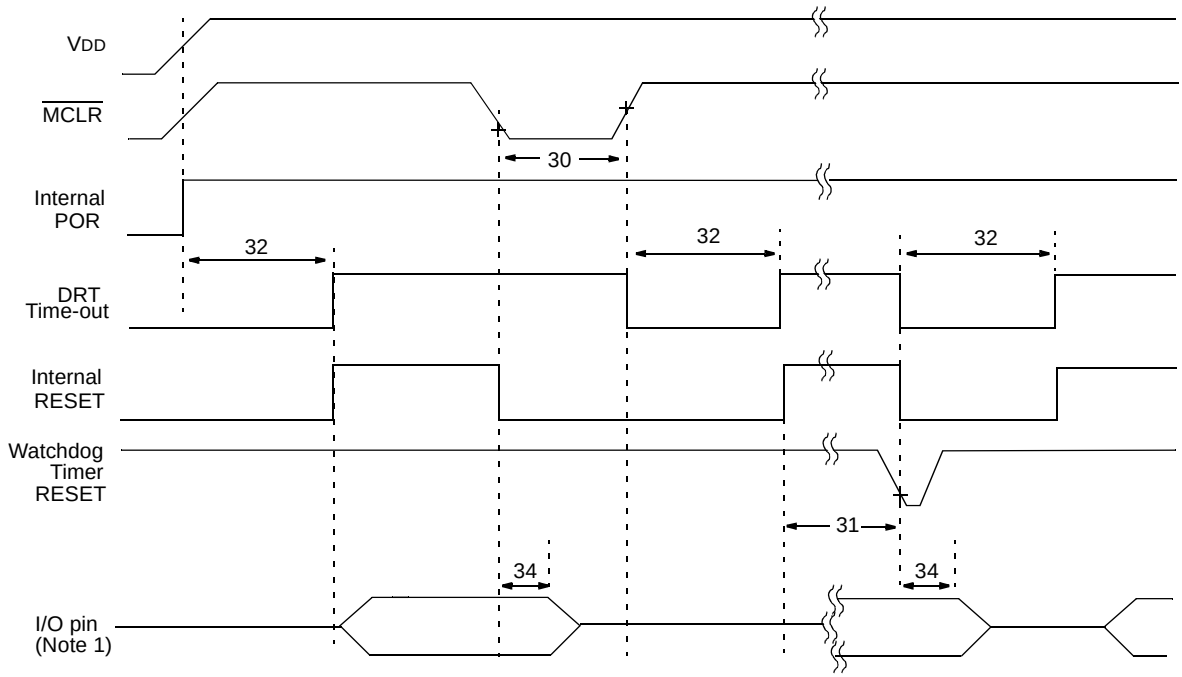
* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 15-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A



Note 1: Please refer to Figure 15-1 for load conditions.

TABLE 15-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial –20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I –40°C ≤ TA ≤ +125°C for extended						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	100* 1	— —	— —	ns µs	VDD = 5.0V VDD = 5.0V (PIC16LV54A only)
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from $\overline{MCLR}$ Low	— —	— —	100* 1µs	ns —	 (PIC16LV54A only)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 16-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF, 25°C

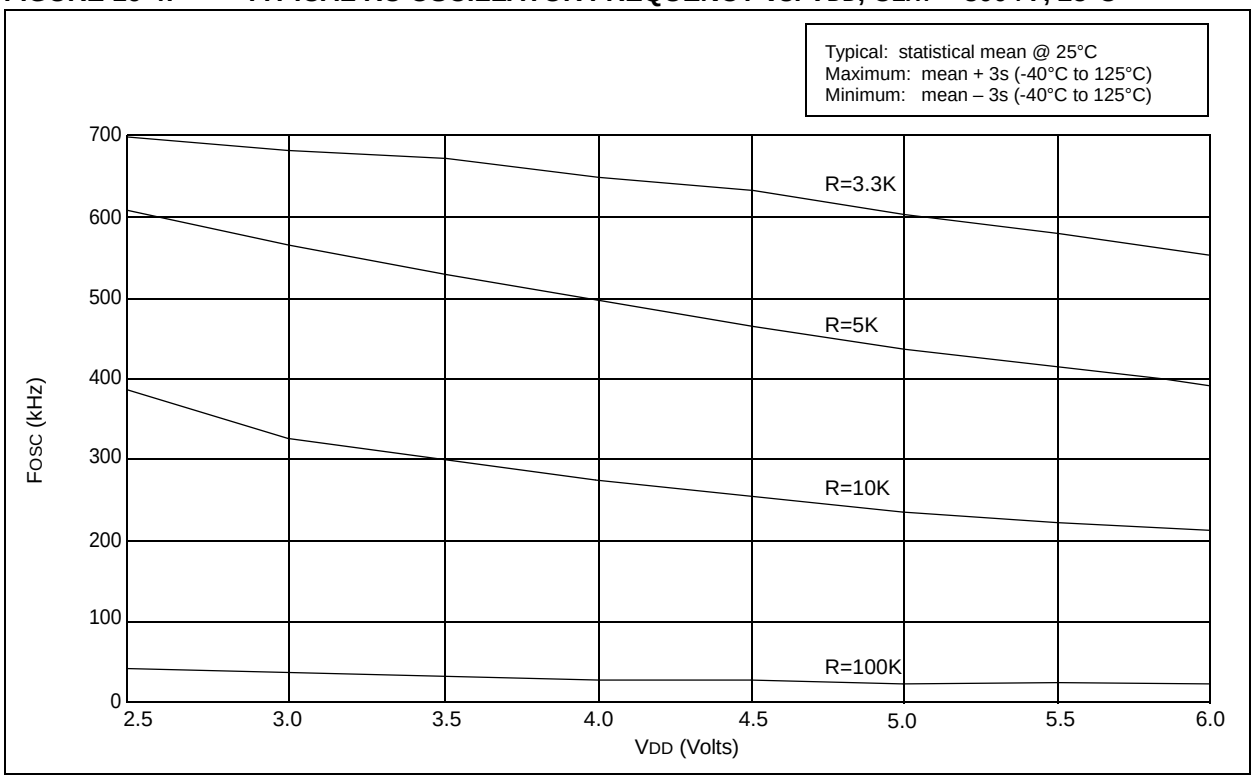


FIGURE 16-18: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

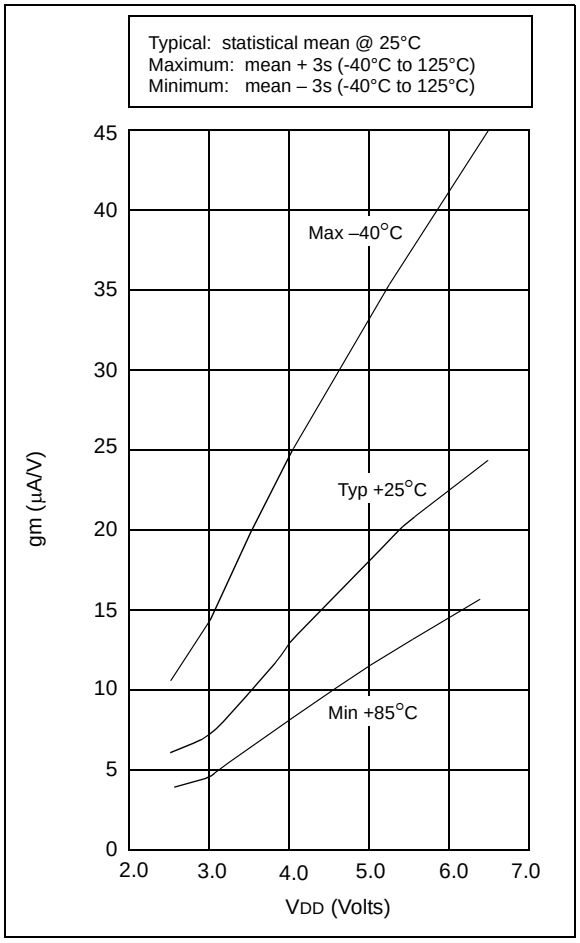


FIGURE 16-19: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

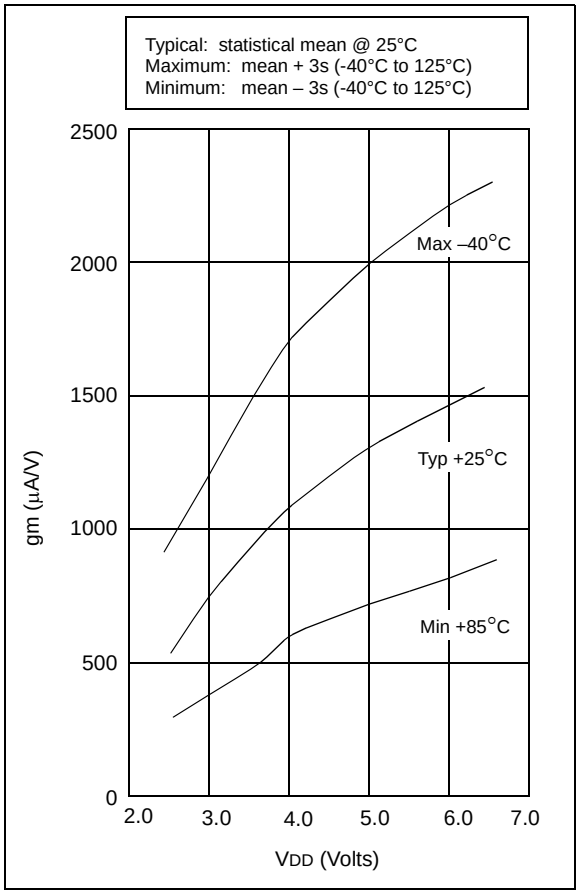


FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF, 25°C

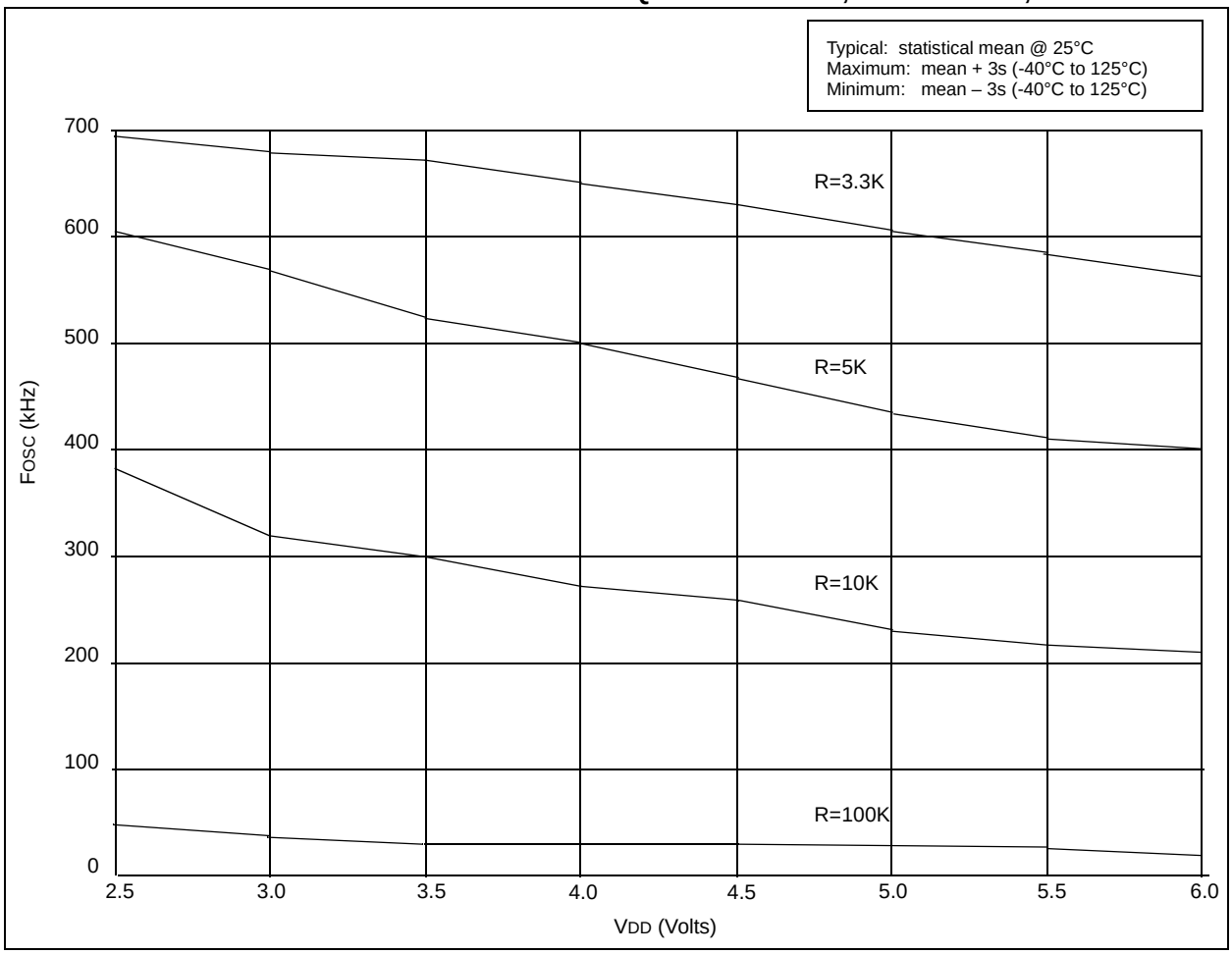


FIGURE 18-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)

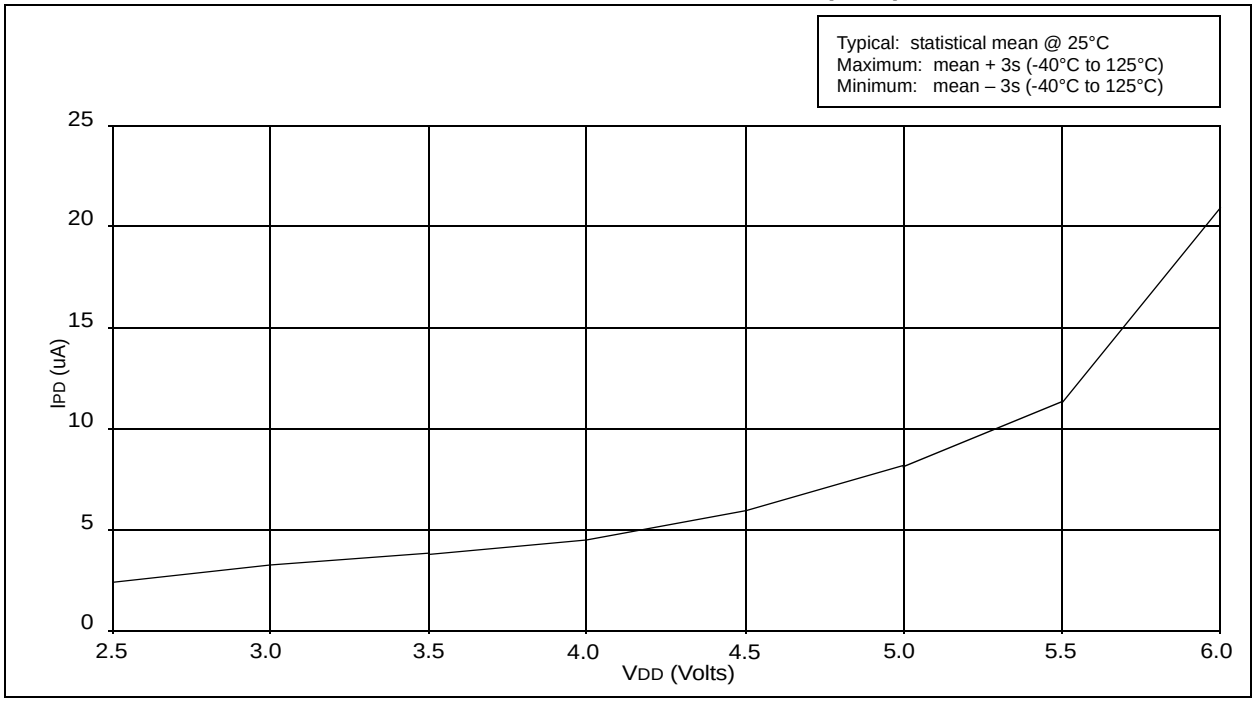
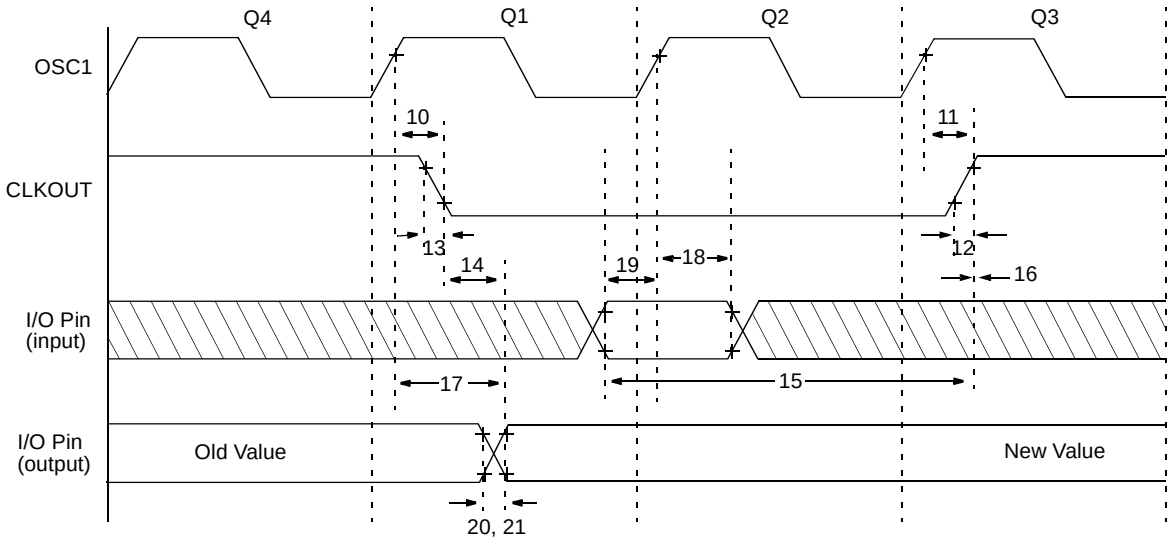


FIGURE 19-4: CLKOUT AND I/O TIMING - PIC16C5X-40



Note: Refer to Figure 19-2 for load conditions.

TABLE 19-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X-40

AC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓ **(1,2)**	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ **(1,2)**	—	15	30**	ns
12	TckR	CLKOUT rise time **(1,2)**	—	5.0	15**	ns
13	TckF	CLKOUT fall time **(1,2)**	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid **(1,2)**	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ **(1,2)**	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑ **(1,2)**	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid **(2)**	—	—	100	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time **(2)**	—	10	25**	ns
21	TioF	Port output fall time **(2)**	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

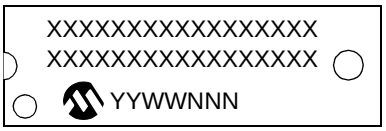
Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

2: Refer to Figure 19-2 for load conditions.

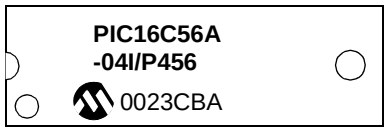
21.0 PACKAGING INFORMATION

21.1 Package Marketing Information

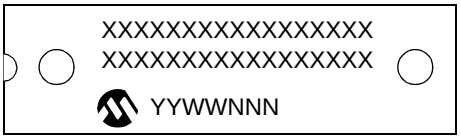
18-Lead PDIP



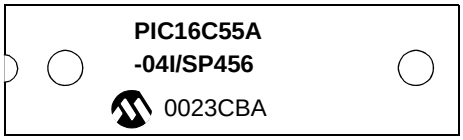
Example



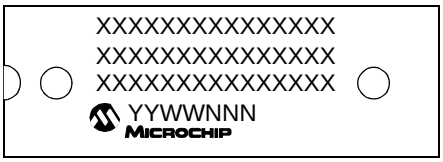
28-Lead Skinny PDIP (.300")



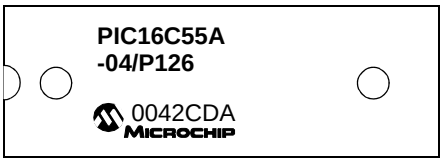
Example



28-Lead PDIP (.600")



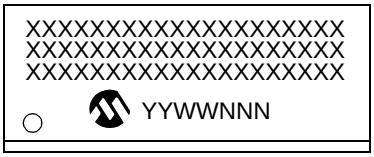
Example



18-Lead SOIC

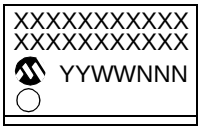
Example

28-Lead SOIC



Example

20-Lead SSOP



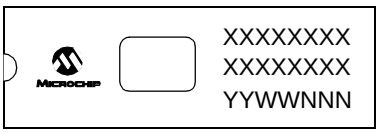
Example

28-Lead SSOP

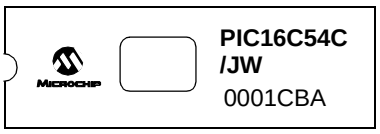
Example

Package Marking Information (Cont'd)

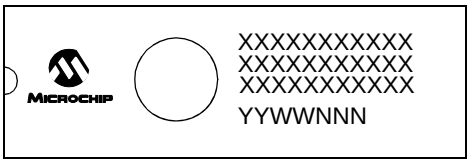
18-Lead CERDIP Windowed



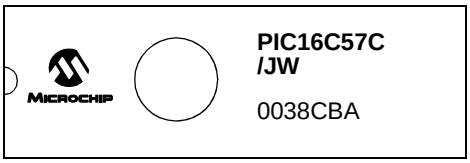
Example



28-Lead CERDIP Windowed



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

