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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c54c-04-ss

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TABLE 1-1: PIC16C5X FAMILY OF DEVICES

Features	PIC16C54	PIC16CR54	PIC16C55	PIC16C56	PIC16CR56	
Maximum Operation Frequency	40 MHz	20 MHz	40 MHz	40 MHz	20 MHz	
EPROM Program Memory (x12 words)	512	—	512	1K	—	
ROM Program Memory (x12 words)	—	512	—	—	1K	
RAM Data Memory (bytes)	25	25	24	25	25	
Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	
I/O Pins	12	12	20	12	12	
Number of Instructions	33	33	33	33	33	
Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	
All PIC [®] Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.						

PIC16C58 Features **PIC16C57** PIC16CR57 PIC16CR58 Maximum Operation Frequency 20 MHz 40 MHz 40 MHz 20 MHz EPROM Program Memory (x12 words) 2K 2K ____ _ ROM Program Memory (x12 words) 2K 2K _ _ RAM Data Memory (bytes) 72 72 73 73 Timer Module(s) TMR0 TMR0 TMR0 TMR0 I/O Pins 20 20 12 12 Number of Instructions 33 33 33 33 28-pin DIP, SOIC; 28-pin DIP, SOIC; 18-pin DIP, SOIC; 18-pin DIP, SOIC; Packages 28-pin SSOP 28-pin SSOP 20-pin SSOP 20-pin SSOP All PIC® Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.

6.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers and General Purpose Registers.

The Special Function Registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Purpose Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

For the PIC16C54, PIC16CR54, PIC16C56 and PIC16CR56, the register file is composed of 7 Special Function Registers and 25 General Purpose Registers (Figure 6-4).

For the PIC16C55, the register file is composed of 8 Special Function Registers and 24 General Purpose Registers.

For the PIC16C57 and PIC16CR57, the register file is composed of 8 Special Function Registers, 24 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-5).

For the PIC16C58 and PIC16CR58, the register file is composed of 7 Special Function Registers, 25 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-6).

6.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the File Select Register (FSR). The FSR Register is described in Section 6.7.

FIGURE 6-4:

PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56 REGISTER FILE MAP



6.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 6-1).

The Special Registers can be classified into two sets. The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Details on Page
N/A	TRIS	I/O Cont	trol Regis	ters (TRIS	SA, TRIS	B, TRISC	;)			1111 1111	35
N/A	OPTION	Contains	s control b	oits to cor	figure Ti	mer0 and	Timer0/V	VDT pres	caler	11 1111	30
00h	INDF	Uses co	Uses contents of FSR to address data memory (not a physical register)				egister)	XXXX XXXX	32		
01h	TMR0	Timer0 I	Timer0 Module Register						XXXX XXXX	38	
02h ⁽¹⁾	PCL	Low ord	er 8 bits c	of PC						1111 1111	31
03h	STATUS	PA2	PA1	PA0	TO	PD	Z	DC	С	0001 1xxx	29
04h	FSR	Indirect	Indirect data memory address pointer				•	1xxx xxxx (3)	32		
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	xxxx	35
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	XXXX XXXX	35
07h ⁽²⁾	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	XXXX XXXX	35

|--|

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 6.5 for an explanation of how to access these bits.

2: File address 07h is a General Purpose Register on the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16CR58 and PIC16CR58.

3: These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for MCLR and WDT Reset, the value is 111u uuuu.

6.5.1 PAGING CONSIDERATIONS – PIC16C56/CR56, PIC16C57/CR57 AND PIC16C58/CR58

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS Register will not be updated. Therefore, the next GOTO, CALL or modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA<1:0>).

For example, a NOP at location 1FFh (page 0) increments the PC to 200h (page 1). A GOTO xxx at 200h will return the program to address xxh on page 0 (assuming that PA<1:0> are clear).

To prevent this, the page preselect bits must be updated under program control.

6.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the RESET vector).

The STATUS Register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a GOTO instruction at the RESET vector location will automatically cause the program to jump to page 0.

6.6 Stack

PIC16C5X devices have a 10-bit or 11-bit wide, two-level hardware push/pop stack.

A CALL instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W Register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the RETLW instruction, the PC is loaded with the Top of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC, therefore, paging is not an issue when returning from a subroutine.

7.6 I/O Programming Considerations

7.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 7-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 7-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;

;				PORT	latch	PORT	pins
;							
	BCF	PORTB,	7	;01pp	pppp	11pp	pppp
	BCF	PORTB,	6	;10pp	pppp	11pp	pppp
	MOVLW	H'3F'		;			
	TRIS	PORTB		;10pp	pppp	10pp	pppp
;							

;Note that the user may have expected the pin ;values to be 00pp pppp. The 2nd BCF caused ;RB7 to be latched as the pin value (High).

7.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 7-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.



FIGURE 7-2: SUCCESSIVE I/O OPERATION

9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of realtime applications. The PIC16C5X family of microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator Selection (Section 4.0)
- RESET (Section 5.0)
- Power-On Reset (Section 5.1)
- Device Reset Timer (Section 5.2)
- Watchdog Timer (WDT) (Section 9.2)
- SLEEP (Section 9.3)
- Code protection (Section 9.4)
- ID locations (Section 9.5)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in RESET until the crystal oscillator is stable. With this timer on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake up from SLEEP through external RESET or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

10.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 10-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers in that bank is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 10-1:	OPCODE FIELD
	DESCRIPTIONS

Field	Description				
f	Register file address (0x00 to 0x1F)				
W	Working register (accumulator)				
b	Bit address within an 8-bit file register				
k	Literal field, constant data or label				
x Don't care location (= 0 or 1)					
The assembler will generate code with x = 0					
	It is the recommended form of use for com-				
	patibility with all Microchip software tools.				
d	Destination select;				
	d = 0 (store result in W)				
d = 1 (store result in file register 'f')					
	Default is d = 1				
label	Label name				
TOS	Top of Stack				
PC	Program Counter				
WDT	Watchdog Timer Counter				
TO	Time-out bit				
PD	Power-down bit				
dest	Destination, either the W register or the				
	specified register file location				
[]	Options				
()	Contents				
\rightarrow	Assigned to				
< >	Register bit field				
E	In the set of				
italics	User defined term (font is courier)				

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time would be 1 μ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time would be 2 μ s.

Figure 10-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file regist	Byte-oriented file register operations				
<u>11 6</u>	5	4 0			
OPCODE	d	f (FILE #)			
d = 0 for destination W d = 1 for destination f f = 5-bit file register address					
Bit-oriented file register operations					
11 8	7	5 4 0			
OPCODE	b (Bl	IT #) f (FILE #)			
 f = 5-bit file register address Literal and control operations (except GOTO) 					
<u>11</u>	8	7 0			
OPCODE		k (literal)			
k = 8-bit immediate value					
Literal and control operations - GOTO instruction					
11	9	8 0			
OPCODE		k (literal)			
k = 9-bit immediate value					

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Mnemonic,		Description	Cualas	12-1	Bit Opc	ode	Status	Netes
Opera	nds	Description		MSb		LSb	Affected	Notes
ADDWF	f,d	Add W and f	1	0001	11df	ffff	C,DC,Z	1,2,4
ANDWF	f,d	AND W with f	1	0001	01df	ffff	Z	2,4
CLRF	f	Clear f	1	0000	011f	ffff	Z	4
CLRW	_	Clear W	1	0000	0100	0000	Z	
COMF	f, d	Complement f	1	0010	01df	ffff	Z	
DECF	f, d	Decrement f	1	0000	11df	ffff	Z	2,4
DECFSZ	f, d	Decrement f, Skip if 0	1 ⁽²⁾	0010	11df	ffff	None	2,4
INCF	f, d	Increment f	1	0010	10df	ffff	Z	2,4
INCFSZ	f, d	Increment f, Skip if 0	1 ⁽²⁾	0011	11df	ffff	None	2,4
IORWF	f, d	Inclusive OR W with f	1	0001	00df	ffff	Z	2,4
MOVF	f, d	Move f	1	0010	00df	ffff	Z	2,4
MOVWF	f	Move W to f	1	0000	001f	ffff	None	1,4
NOP	_	No Operation	1	0000	0000	0000	None	
RLF	f, d	Rotate left f through Carry	1	0011	01df	ffff	С	2,4
RRF	f, d	Rotate right f through Carry	1	0011	00df	ffff	С	2,4
SUBWF	f, d	Subtract W from f	1	0000	10df	ffff	C,DC,Z	1,2,4
SWAPF	f, d	Swap f	1	0011	10df	ffff	None	2,4
XORWF	f, d	Exclusive OR W with f	1	0001	10df	ffff	Z	2,4
BIT-ORIEN	TED FIL	E REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	0100	bbbf	ffff	None	2,4
BSF	f, b	Bit Set f	1	0101	bbbf	ffff	None	2,4
BTFSC	f, b	Bit Test f, Skip if Clear	1 ⁽²⁾	0110	bbbf	ffff	None	
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	0111	bbbf	ffff	None	
LITERAL A	ND CON	ITROL OPERATIONS		r				
ANDLW	k	AND literal with W	1	1110	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	1001	kkkk	kkkk	None	1
CLRWDT	k	Clear Watchdog Timer	1	0000	0000	0100	TO, PD	
GOTO	k	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW	k	Inclusive OR Literal with W	1	1101	kkkk	kkkk	Z	
MOVLW	k	Move Literal to W	1	1100	kkkk	kkkk	None	
OPTION	k	Load OPTION register	1	0000	0000	0010	None	
RETLW	k	Return, place Literal in W	2	1000	kkkk	kkkk	None	
SLEEP	-	Go into standby mode	1	0000	0000	0011	TO, PD	
TRIS	f	Load TRIS register	1	0000	0000	Offf	None	3
XORLW	k	Exclusive OR Literal to W	1	1111	kkkk	kkkk	Z	

TABLE 10-2: INSTRUCTION SET SUMMARY

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO (see Section 6.5 for more on program counter).

2: When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

3: The instruction TRIS f, where f = 5, 6 or 7 causes the contents of the W register to be written to the tristate latches of PORTA, B or C respectively. A '1' forces the pin to a hi-impedance state and disables the output buffers.

4: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

ADDWF	Add	W	and f			
Syntax:	[lab	e/]/	ADDWF	f,d		
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$					
Operation:	$(W) + (f) \to (dest)$					
Status Affected:	C, D	C, Z				
Encoding:	00	01	11df	ff	ff	
	and is st '1' th regi	regi ored ne re ister	ster 'f'. If 'o I in the W sult is sto 'f'.	d' is regi red	0 the ster. I back	result If 'd' is in
Words:	1					
Cycles:	1					
Example:	ADD	WF	TEMP_RE	G,	0	
Before Instruc		n				
W		=	0x17			
TEMP_RE After Instructio		=	0xC2			
W		=	0xD9			
TEMP_F	REG	=	0xC2			

ANDWF	AND W with f			
Syntax:	[label] ANDWF f,d			
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$			
Operation:	(W) .AND. (f) \rightarrow (dest)			
Status Affected:	Ζ			
Encoding:	0001 01df ffff			
Description:	The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W regis- ter. If 'd' is '1' the result is stored back in register 'f'.			
Words:	1			
Cycles:	1			
Example:	ANDWF TEMP_REG, 1			
Before Instru W TEMP_I After Instruct W TEMP_I	action = $0x17$ REG = $0xC2$ ion = $0x17$ REG = $0x02$			

ANDLW	AND literal with W					
Syntax:	[<i>label</i>] ANDLW k					
Operands:	$0 \le k \le 255$					
Operation:	(W).AND. (k) \rightarrow (W)					
Status Affected:	Z					
Encoding:	1110 kkkk kkkk					
Description:	The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W regis- ter.					
Words:	1					
Cycles:	1					
Example:	ANDLW H'5F'					
Before Instru W = After Instruct W =	ction 0xA3 ion 0x03					

BCF	Bit Clear f							
Syntax:	[label]	BCF f,t)					
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ 0 \leq b \leq 7 \end{array}$							
Operation:	$0 \rightarrow (f < b >)$							
Status Affected: None								
Encoding:	0100	bbbf	ffff					
Description:	Bit 'b' in	register 'f'	is cleare	d.				
Words:	1							
Cycles:	1							
Example:	BCF	FLAG_RE	G, 7					
Before Instru FLAG_R After Instruct	ction EG = ion	0xC7						
FLAG_R	EG =	0x47						

GOTO	Unconditional Branch					
Syntax:	[label]	GOTO	k			
Operands:	$0 \le k \le 5^{-1}$	11				
Operation:	$k \rightarrow PC < 8:0>;$ STATUS<6:5> $\rightarrow PC < 10:9>$					
Status Affected:	None					
Encoding:	101k	kkkk	kkkk			
Description:	GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two- cycle instruction.					
Words:	1					
Cycles:	2					
Example:	GOTO TH	IERE				
After Instructi PC =	on address	G (THER	E)			

INCF	Increment f
Syntax:	[label] INCF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$
Operation:	(f) + 1 \rightarrow (dest)
Status Affected:	Z
Encoding:	0010 10df ffff
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
Words:	1
Cycles:	1
Example:	INCF CNT, 1
Before Instru CNT Z After Instructi CNT Z	ction = 0xFF = 0 ion = 0x00 = 1

INCFSZ	Increment f, Skip if 0					
Syntax:	[label] INCFSZ f,d					
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$					
Operation:	(f) + 1 \rightarrow (dest), skip if result = 0					
Status Affected:	None					
Encoding:	0011 11df ffff					
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-					
Words:	1					
Cycles:	1(2)					
Example:	HERE INCFSZ CNT, 1 GOTO LOOP					
	CONTINUE • • •					
Before Instru	iction					
PC	= address (HERE)					
After Instruct	ion					
CNT	= CNT + 1;					
if CNT	= 0,					
PC	= address (CONTINUE);					
if CNT	≠ 0, 					
PC	= address (HERE +1)					

12.4 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial) PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

DC CH	ARACTE	RISTICS	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \end{array}$					
Param No.	Symbol	Characteristic/Device	Min	Min Typ† Max Units			Conditions	
D030	VIL	Input Low Voltage I/O ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1 (Schmitt Trigger)	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>	Pin at hi-impedance PIC16C5X-RC only ⁽³⁾ PIC16C5X-XT, 10, HS, LP	
D040 D050	VIH	Input High Voltage I/O ports I/O ports I/O ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1 (Schmitt Trigger) Hysteresis of Schmitt	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD 0.15 VDD*		VDD VDD VDD VDD VDD VDD VDD	V V V V V V V	For all $VDD^{(4)}$ 4.0V < $VDD \le 5.5V^{(4)}$ VDD > 5.5V PIC16C5X-RC only ⁽³⁾ PIC16C5X-XT, 10, HS, LP	
D060	lı.	Trigger inputs Input Leakage Current ^(1,2) I/O ports MCLR MCLR TOCKI OSC1	-1 -5 -3 -3 -3	0.5 — 0.5 0.5 0.5	+1 +5 +3 +3	μΑ μΑ μΑ μΑ	$\label{eq:ForVDD} \begin{split} & \leq \textbf{5.5V:} \\ & VSS \leq VPIN \leq VDD, \\ & pin \text{ at hi-impedance} \\ & VPIN = VSS + 0.25V \\ & VPIN = VDD \\ & VSS \leq VPIN \leq VDD \\ & VSS \leq VPIN \leq VDD, \\ & PIC16C5X-XT, \ 10, \ HS, \ LP \end{split}$	
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT			0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC	
D090	Vон	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	Vdd - 0.7 Vdd - 0.7		_	V V	ІОН = –5.4 mA, VDD = 4.5V ІОН = –1.0 mA, VDD = 4.5V, PIC16C5X-RC	

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- **Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
 - 2: Negative current is defined as coming out of the pin.
 - **3:** For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
 - 4: The user may use the better of the two specifications.

13.4 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

DC CH	ARACTE	RISTICS	Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended				
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions
D030	VIL	Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vss Vss Vss Vss Vss		0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V	Pin at hi-impedance RC mode only ⁽³⁾ XT, HS and LP modes
D040	Vih	Input High Voltage I/O ports I/O ports I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD VDD	V V V V V V V	For all VDD ⁽⁴⁾ 4.0V < VDD ≤ 5.5V ⁽⁴⁾ VDD > 5.5V RC mode only ⁽³⁾ XT, HS and LP modes
D050	VHYS	Hysteresis of Schmitt Trigger inputs	0.15 Vdd*	—	—	V	
D060	lı∟	Input Leakage Current ^(1,2) I/O ports MCLR MCLR T0CKI OSC1	-1.0 -5.0 -3.0 -3.0	0.5 — 0.5 0.5 0.5	+1.0 	μΑ μΑ μΑ μΑ	$\label{eq:For VDD} \begin{split} & \leq \textbf{5.5V:} \\ & \forall SS \leq \forall PIN \leq \forall DD, \\ & pin \text{ at hi-impedance} \\ & \forall PIN = \forall SS + 0.25 \forall \\ & \forall PIN = \forall DD \\ & \forall SS \leq \forall \forall PIN \leq \forall DD \\ & \forall SS \leq \forall \forall PIN \leq \forall DD, \\ & \forall XT, \ HS \text{ and } \ LP \ modes \end{split}$
D080	Vol	Output Low Voltage I/O ports OSC2/CLKOUT		_	0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, RC mode only
D090	Vон	Output High Voltage ⁽²⁾ I/O ports OSC2/CLKOUT	VDD - 0.7 VDD - 0.7			V V	IOH = -5.4 mA, VDD = 4.5 V IOH = -1.0 mA, VDD = 4.5 V, RC mode only

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

FIGURE 13-5: TIMER0 CLOCK TIMINGS - PIC16CR54A



TABLE 13-4: TIMER0 CLOCK REQUIREMENTS - PIC16CR54A

	Standard Operating Conditions (unless otherwise specified)							
	AC Char	actorictics	Operating Temperat	ture $0^{\circ}C \le TA \le +70^{\circ}C$ for commercial				
	AC Citaracteristics				$TA \le +8$	B5°C f	or indus	strial
			$-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					ended
Param No.	Symbol		Characteristic	Min	Тур†	Max	Units	Conditions
40	Tt0H	T0CKI High	Pulse Width					
			- No Prescaler	0.5 TCY + 20*	—	—	ns	
			- With Prescaler	10*		—	ns	
41	Tt0L	T0CKI Low	Pulse Width					
			- No Prescaler	0.5 TCY + 20*	—	—	ns	
			- With Prescaler	10*	_	—	ns	
42	Tt0P	T0CKI Peric	od	20 or <u>Tcy + 40</u> *		—	ns	Whichever is greater.
				N				N = Prescale Value
								(1, 2, 4,, 256)

These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

14.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.





TABLE 14-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Average Fosc @ 5 V, 25°C				
20 pF	3.3K	5 MHz	± 27%			
	5K	3.8 MHz	± 21%			
	10K	2.2 MHz	± 21%			
	100K	262 kHz	± 31%			
100 pF	3.3K	1.6 MHz	± 13%			
	5K	1.2 MHz	± 13%			
	10K	684 kHz	± 18%			
	100K	71 kHz	± 25%			
300 pF	3.3K	660 kHz	± 10%			
	5.0K	484 kHz	± 14%			
	10K	267 kHz	± 15%			
	100K	29 kHz	± 19%			

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviations from the average value for VDD = 5V.

16.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.



FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

TABLE 16-1: RC OSCILLATOR FREQUENCIES

Сехт	Rext	Average Fosc @ 5 V, 25°C			
20 pF	3.3K	5 MHz	± 27%		
	5K	3.8 MHz	± 21%		
	10K	2.2 MHz	± 21%		
	100K	262 kHz	± 31%		
100 pF	3.3K	1.6 MHz	± 13%		
	5K	1.2 MHz	± 13%		
	10K	684 kHz	± 18%		
	100K	71 kHz	± 25%		
300 pF	3.3K	660 kHz	± 10%		
	5.0K	484 kHz	± 14%		
	10K	267 kHz	± 15%		
	100K	29 kHz	± 19%		

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for VDD = 5V.

17.0 ELECTRICAL CHARACTERISTICS - PIC16LC54A

Absolute Maximum Ratings^(†)

Ambient temperature under bias	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	–0.6V to (VDD + 0.6V)
Total power dissipation ⁽¹⁾	
Max. current out of Vss pin	150 mA
Max. current into Vod pin	100 mA
Max. current into an input pin (T0CKI only)	±500 μA
Input clamp current, Iк (Vi < 0 or Vi > VDD)	±20 mA
Output clamp current, Iок (Vo < 0 or Vo > Voo)	±20 mA
Max. output current sunk by any I/O pin	25 mA
Max. output current sourced by any I/O pin	20 mA
Max. output current sourced by a single I/O (Port A, B or C)	50 mA
Max. output current sunk by a single I/O (Port A, B or C)	50 mA
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH} + \sum {(VD	D-VOH) X IOH} + Σ (VOL X IOL)

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.







17.5 Timing Diagrams and Specifications



FIGURE 17-6: EXTERNAL CLOCK TIMING - PIC16C5X, PIC16CR5X

TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

$\begin{tabular}{ c c c c c } AC \ Characteristics \end{tabular} \begin{tabular}{lllllllllllllllllllllllllllllllllll$					4)		
Param No.	Symbol	Characteristic	Min	Тур†	Мах	Units	Conditions
	Fosc	External CLKIN Frequency ⁽¹⁾	DC		4.0	MHz	XT OSC mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	20	MHz	HS osc mode (20)
			DC		200	kHz	LP OSC mode
		Oscillator Frequency ⁽¹⁾	DC	—	4.0	MHz	RC osc mode
			0.45	—	4.0	MHz	XT OSC mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	20	MHz	HS osc mode (20)
			5.0		200	kHz	LP OSC mode
1	Tosc	External CLKIN Period ⁽¹⁾	250		—	ns	XT OSC mode
			250	—	—	ns	HS osc mode (04)
			50	—	—	ns	HS osc mode (20)
			5.0		—	μS	LP OSC mode
		Oscillator Period ⁽¹⁾	250		—	ns	RC osc mode
			250	—	2,200	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	μS	LP OSC mode

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: Instruction cycle period (TCY) equals four times the input oscillator time base period.

18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	р		.100			2.54	
Top to Seating Plane	А	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	Е	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	ß	5	10	15	5	10	15

* Controlling Parameter § Significant Characteristic

Notes:

n

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-001 Drawing No. C04-007

28-Lead Ceramic Dual In-line with Window (JW) - 600 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.100			2.54	
Top to Seating Plane	А	.195	.210	.225	4.95	5.33	5.72
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.038	.060	0.38	0.95	1.52
Shoulder to Shoulder Width	Е	.595	.600	.625	15.11	15.24	15.88
Ceramic Pkg. Width	E1	.514	.520	.526	13.06	13.21	13.36
Overall Length	D	1.430	1.460	1.490	36.32	37.08	37.85
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	С	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.058	.065	1.27	1.46	1.65
Lower Lead Width	В	.016	.020	.023	0.41	0.51	0.58
Overall Row Spacing §	eB	.610	.660	.710	15.49	16.76	18.03
Window Diameter	W	.270	.280	.290	6.86	7.11	7.37

Sontolling Parameter
 Significant Characteristic
 JEDEC Equivalent: MO-103
 Drawing No. C04-013