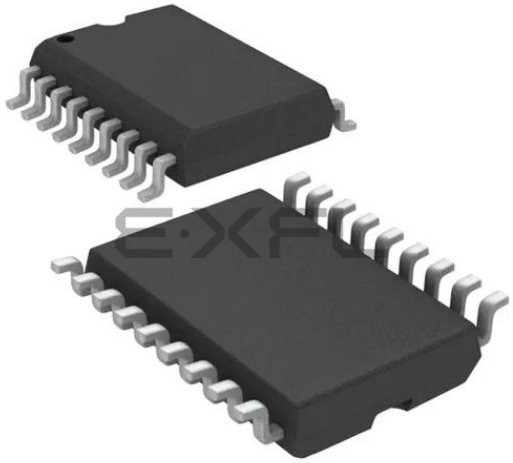

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c54c-04i-so

NOTES:

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5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the MCLR/VPP pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is RESET. The DRT timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where MCLR is not tied to VDD is shown in Figure 5-3. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset TDRT msec after MCLR goes high.

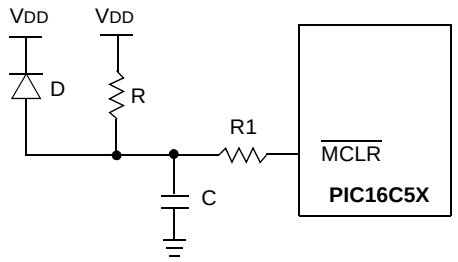
In Figure 5-4, the on-chip Power-On Reset feature is being used (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the MCLR/VPP pin, and when the MCLR/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

Note:	When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the Embedded Control Handbook.

The POR circuit does not produce an internal RESET when VDD declines.

FIGURE 5-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

9.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT Reset or Wake-up Reset generates a device RESET.

The $\overline{TO}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset (Section 6.3).

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 9.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

9.2.1 WDT PERIOD

An 8-bit counter is available as a prescaler for the Timer0 module (Section 8.2), or as a postscaler for the Watchdog Timer (WDT), respectively. For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio (Section 6.4).

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see Device Characterization).

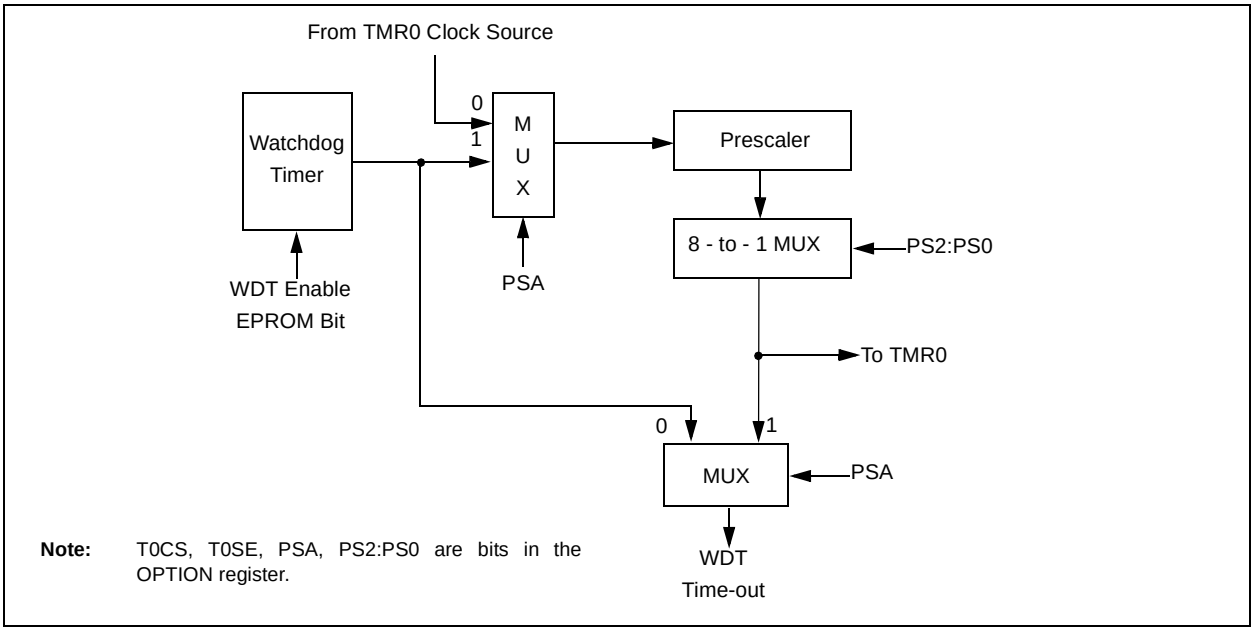
Under worst case conditions (VDD = Min., Temperature = Max., WDT prescaler = 1:128), it may take several seconds before a WDT time-out occurs.

9.2.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction RESETS the WDT and the prescaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.

FIGURE 9-1: WATCHDOG TIMER BLOCK DIAGRAM



Note: T0CS, T0SE, PSA, PS2:PS0 are bits in the OPTION register.

TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	OPTION	—	—	Tosc	Tose	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: u = unchanged, - = unimplemented, read as '0'. Shaded cells not used by Watchdog Timer.

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10.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 10-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers in that bank is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 10-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x1F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit
dest	Destination, either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

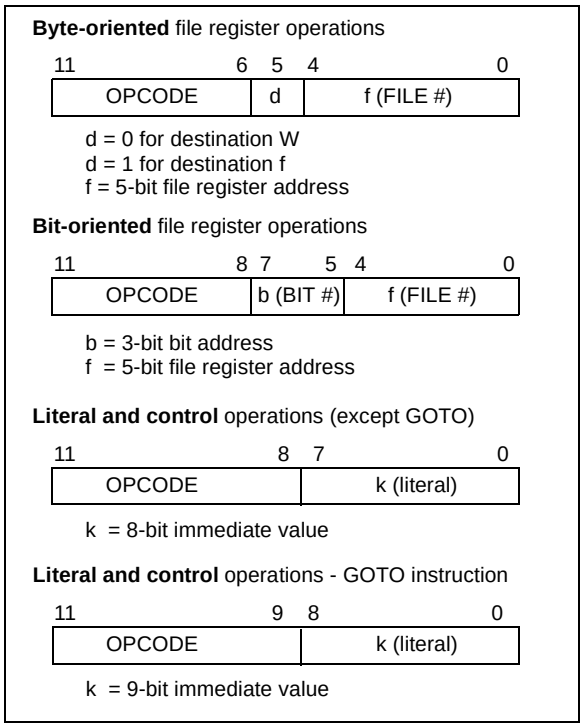
All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time would be 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time would be 2 μs.

Figure 10-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS



RLF **Rotate Left f through Carry**

Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

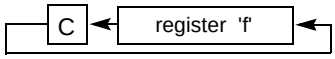
Operation: See description below

Status Affected: C

Encoding:

0011	01df	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example:
```
RLF    REG1,0
```
Before Instruction
```
REG1    =  1110 0110
C       =  0
```
After Instruction
```
REG1    =  1110 0110
W       =  1100 1100
C       =  1
```

RRF **Rotate Right f through Carry**

Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

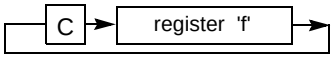
Operation: See description below

Status Affected: C

Encoding:

0011	00df	ffff

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Example:
```
RRF    REG1,0
```
Before Instruction
```
REG1    =  1110 0110
C       =  0
```
After Instruction
```
REG1    =  1110 0110
W       =  0111 0011
C       =  0
```

SLEEP **Enter SLEEP Mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler; if assigned
1 → $\overline{TO}$;
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

0000	0000	0011

Description: Time-out status bit ($\overline{TO}$) is set. The power-down status bit ($\overline{PD}$) is cleared. The WDT and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example:
```
SLEEP
```

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12.5 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D030	VIL	**Input Low Voltage**					
		I/O ports	Vss	—	0.15 VDD	V	Pin at hi-impedance
		MCLR (Schmitt Trigger)	Vss	—	0.15 VDD	V	
		T0CKI (Schmitt Trigger)	Vss	—	0.15 VDD	V	
		OSC1 (Schmitt Trigger)	Vss	—	0.15 VDD	V	PIC16C5X-RC only(3)
		OSC1 (Schmitt Trigger)	Vss	—	0.3 VDD	V	PIC16C5X-XT, 10, HS, LP
D040	VIH	**Input High Voltage**					
		I/O ports	0.45 VDD	—	VDD	V	For all VDD(4)
		I/O ports	2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(4)
		I/O ports	0.36 VDD	—	VDD	V	VDD > 5.5 V
		MCLR (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		T0CKI (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		OSC1 (Schmitt Trigger)	0.85 VDD	—	VDD	V	PIC16C5X-RC only(3)
		OSC1 (Schmitt Trigger)	0.7 VDD	—	VDD	V	PIC16C5X-XT, 10, HS, LP
D050	VHYS	**Hysteresis of Schmitt Trigger inputs**	0.15 VDD*	—	—	V	
D060	IIL	**Input Leakage Current (1,2)**					**For VDD ≤ 5.5 V:**
		I/O ports	–1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
		MCLR	–5	—	—	µA	VPIN = VSS + 0.25V
		MCLR	—	0.5	+5	µA	VPIN = VDD
		T0CKI	–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
		OSC1	–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, 10, HS, LP
D080	VOL	**Output Low Voltage**					
		I/O ports	—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
		OSC2/CLKOUT	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC
D090	VOH	**Output High Voltage(2)**					
		I/O ports	VDD – 0.7	—	—	V	IOH = –5.4 mA, VDD = 4.5V
		OSC2/CLKOUT	VDD – 0.7	—	—	V	IOH = –1.0 mA, VDD = 4.5V, PIC16C5X-RC

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the $\overline{\text{MCLR}}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

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13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

PIC16LCR54A-04 **PIC16LCR54A-04I** (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
PIC16CR54A-04, 10, 20 **PIC16CR54A-04I, 10I, 20I** (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Symbol**	**Characteristic/Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	IPD	**Power-down Current(2)**					
D006		PIC16LCR54A-Commercial	—	1.0	6.0	µA	VDD = 2.5V, WDT disabled
			—	2.0	8.0*	µA	VDD = 4.0V, WDT disabled
			—	3.0	15	µA	VDD = 6.0V, WDT disabled
			—	5.0	25	µA	VDD = 6.0V, WDT enabled
D006A		PIC16CR54A-Commercial	—	1.0	6.0	µA	VDD = 2.5V, WDT disabled
			—	2.0	8.0*	µA	VDD = 4.0V, WDT disabled
			—	3.0	15	µA	VDD = 6.0V, WDT disabled
			—	5.0	25	µA	VDD = 6.0V, WDT enabled
D007		PIC16LCR54A-Industrial	—	1.0	8.0	µA	VDD = 2.5V, WDT disabled
			—	2.0	10*	µA	VDD = 4.0V, WDT disabled
			—	3.0	20*	µA	VDD = 4.0V, WDT enabled
			—	3.0	18	µA	VDD = 6.0V, WDT disabled
			—	5.0	45	µA	VDD = 6.0V, WDT enabled
D007A		PIC16CR54A-Industrial	—	1.0	8.0	µA	VDD = 2.5V, WDT disabled
			—	2.0	10*	µA	VDD = 4.0V, WDT disabled
			—	3.0	20*	µA	VDD = 4.0V, WDT enabled
			—	3.0	18	µA	VDD = 6.0V, WDT disabled
			—	5.0	45	µA	VDD = 6.0V, WDT enabled

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

13.3 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D030	VIL	**Input Low Voltage**					
		I/O ports	VSS	—	0.2 VDD	V	Pin at hi-impedance
		MCLR (Schmitt Trigger)	VSS	—	0.15 VDD	V	
		T0CKI (Schmitt Trigger)	VSS	—	0.15 VDD	V	
		OSC1 (Schmitt Trigger)	VSS	—	0.15 VDD	V	RC mode only(3)
		OSC1	VSS	—	0.15 VDD	V	XT, HS and LP modes
D040	VIH	**Input High Voltage**					
		I/O ports	2.0	—	VDD	V	VDD = 3.0V to 5.5V(4)
		I/O ports	0.6 VDD	—	VDD	V	Full VDD range(4)
		MCLR (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		T0CKI (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		OSC1 (Schmitt Trigger)	0.85 VDD	—	VDD	V	RC mode only(3)
		OSC1	0.85 VDD	—	VDD	V	XT, HS and LP modes
D050	VHYS	**Hysteresis of Schmitt Trigger inputs**	0.15 VDD*	—	—	V	
D060	IIL	**Input Leakage Current(1,2)**					**For VDD ≤ 5.5V:**
		I/O ports	–1.0	—	+1.0	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
		MCLR	–5.0	—	—	µA	VPIN = VSS + 0.25V
		MCLR	—	0.5	+5.0	µA	VPIN = VDD
		T0CKI	–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
		OSC1	–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP modes
D080	VOL	**Output Low Voltage**					
		I/O ports	—	—	0.5	V	IOL = 10 mA, VDD = 6.0V
		OSC2/CLKOUT	—	—	0.5	V	IOL = 1.9 mA, VDD = 6.0V, RC mode only
D090	VOH	**Output High Voltage(2)**					
		I/O ports	VDD – 0.5	—	—	V	IOH = –4.0 mA, VDD = 6.0V
		OSC2/CLKOUT	VDD – 0.5	—	—	V	IOH = –0.8 mA, VDD = 6.0V, RC mode only

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

2: Negative current is defined as coming out of the pin.

3: For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

4: The user may use the better of the two specifications.

FIGURE 14-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD

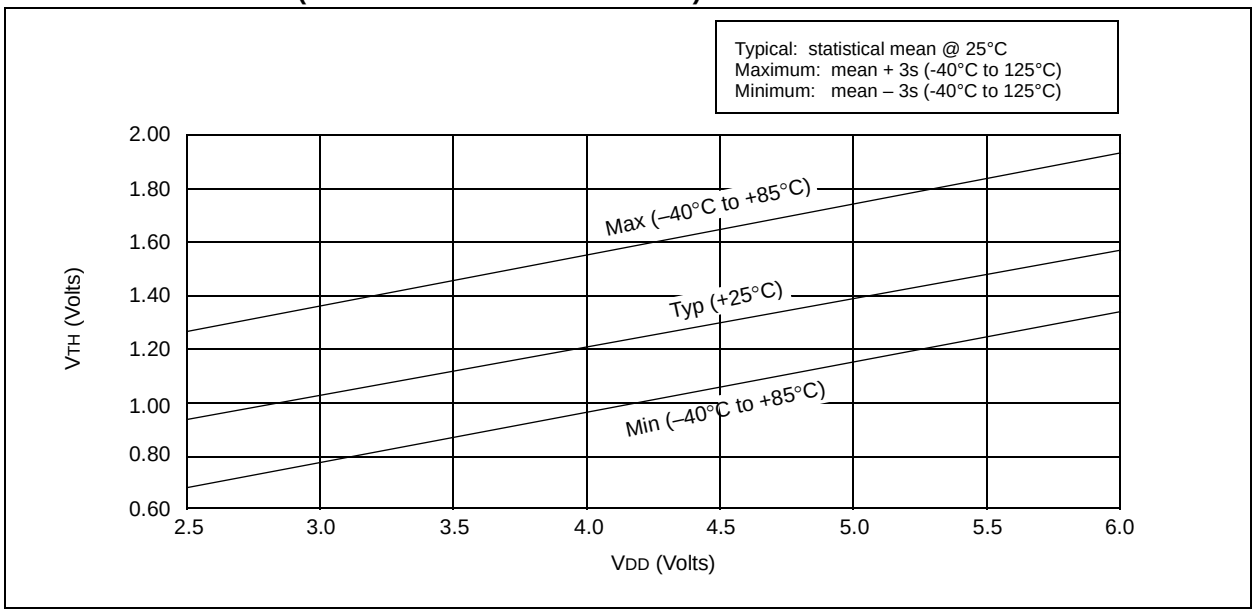
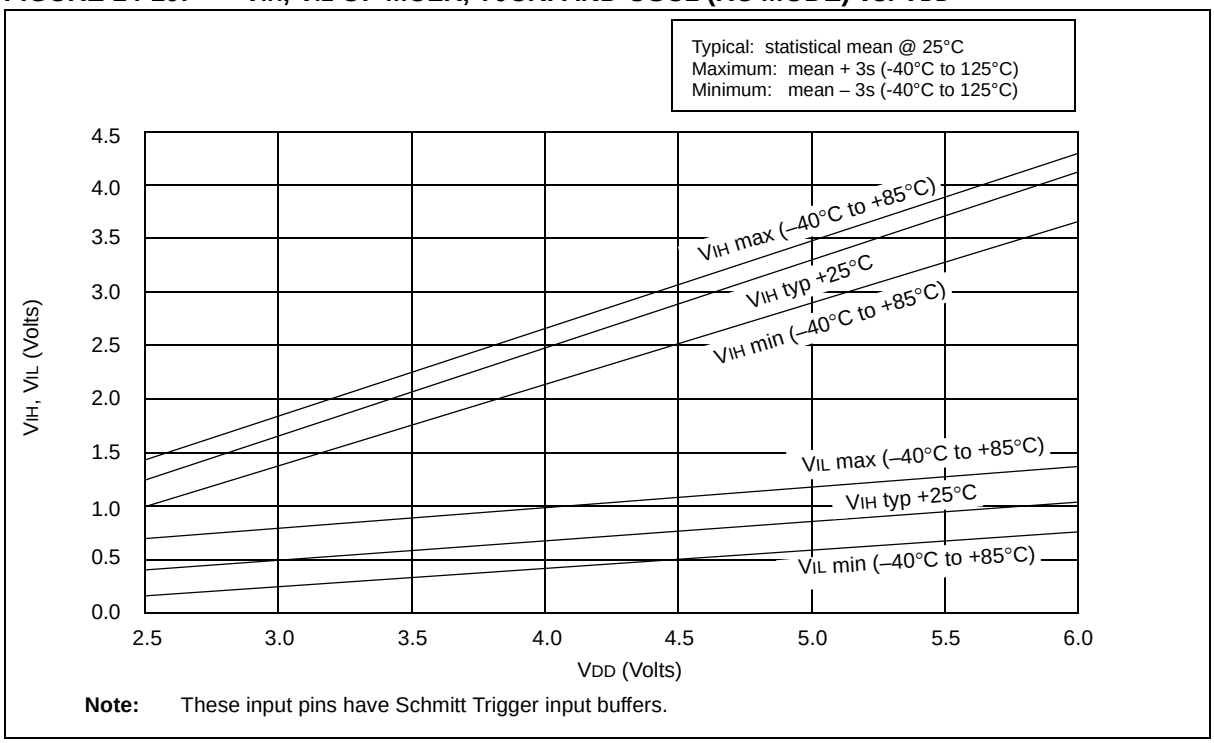


FIGURE 14-10: VIH, VIL OF $\overline{\text{MCLR}}$, T0CKI AND OSC1 (RC MODE) vs. VDD



Note: These input pins have Schmitt Trigger input buffers.

15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial)
PIC16C54A-04I, 10I, 20I (Industrial)
PIC16LC54A-04 (Commercial)
PIC16LC54A-04I (Industrial)

PIC16LC54A-04 **PIC16LC54A-04I** (Commercial, Industrial)	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial
PIC16C54A-04, 10, 20 **PIC16C54A-04I, 10I, 20I** (Commercial, Industrial)	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial

Param No.	Symbol	Characteristic/Device	Min	Typ†	Max	Units	Conditions
	IPD	**Power-down Current(2)**					
D006		PIC16LC5X	—	2.5	12	µA	VDD = 2.5V, WDT enabled, Commercial
			—	0.25	4.0	µA	VDD = 2.5V, WDT disabled, Commercial
			—	2.5	14	µA	VDD = 2.5V, WDT enabled, Industrial
			—	0.25	5.0	µA	VDD = 2.5V, WDT disabled, Industrial
D006A		PIC16C5X	—	4.0	12	µA	VDD = 3.0V, WDT enabled, Commercial
			—	0.25	4.0	µA	VDD = 3.0V, WDT disabled, Commercial
			—	5.0	14	µA	VDD = 3.0V, WDT enabled, Industrial
			—	0.3	5.0	µA	VDD = 3.0V, WDT disabled, Industrial

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

15.3 DC Characteristics: PIC16LV54A-02 (Commercial) PIC16LV54A-02I (Industrial)

PIC16LV54A-02 PIC16LV54A-02I (Commercial, Industrial)			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –20°C ≤ TA ≤ +85°C for industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage** RC and XT modes	2.0	—	3.8	V	
D002	VDR	**RAM Data Retention Voltage(1)**	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	Vss	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset
D010	IDD	**Supply Current(2)** RC(3) and XT modes LP mode, Commercial LP mode, Industrial	 — — —	 0.5 11 14	 — 27 35	 mA µA µA	 FOSC = 2.0 MHz, VDD = 3.0V FOSC = 32 kHz, VDD = 2.5V WDT disabled FOSC = 32 kHz, VDD = 2.5V WDT disabled
D020	IPD	**Power-down Current(2,4)** Commercial Commercial Industrial Industrial	 — — — —	 2.5 0.25 3.5 0.3	 12 4.0 14 5.0	 µA µA µA µA	 VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

4: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection on wake-up from SLEEP mode or during initial power-up.

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15.5 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T	
F Frequency	T Time

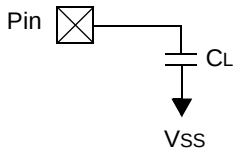
Lowercase letters (pp) and their meanings:

pp	
2 to	mc $\overline{\text{MCLR}}$
ck CLKOUT	osc oscillator
cy cycle time	os OSC1
drt device reset timer	t0 T0CKI
io I/O port	wdt watchdog timer

Uppercase letters and their meanings:

S	
F Fall	P Period
H High	R Rise
I Invalid (Hi-impedance)	V Valid
L Low	Z Hi-impedance

FIGURE 15-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54A



C_L = 50 pF for all pins and OSC2 for RC modes

0 -15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

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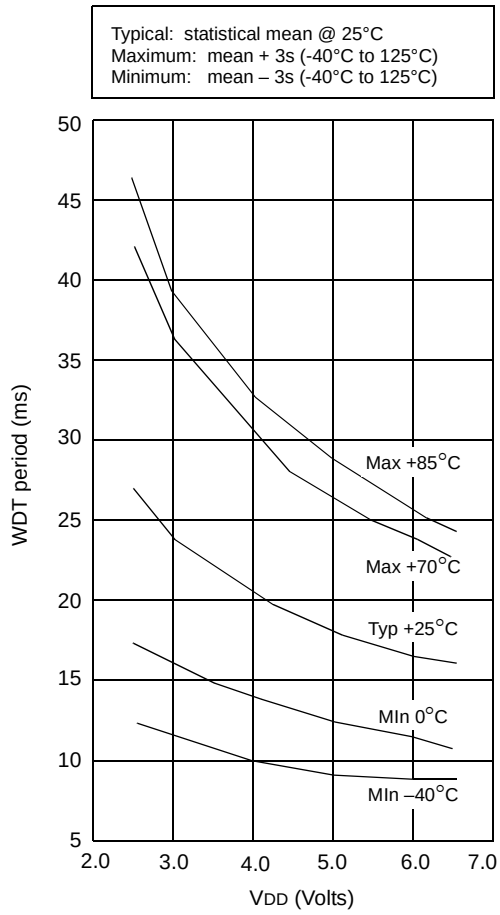
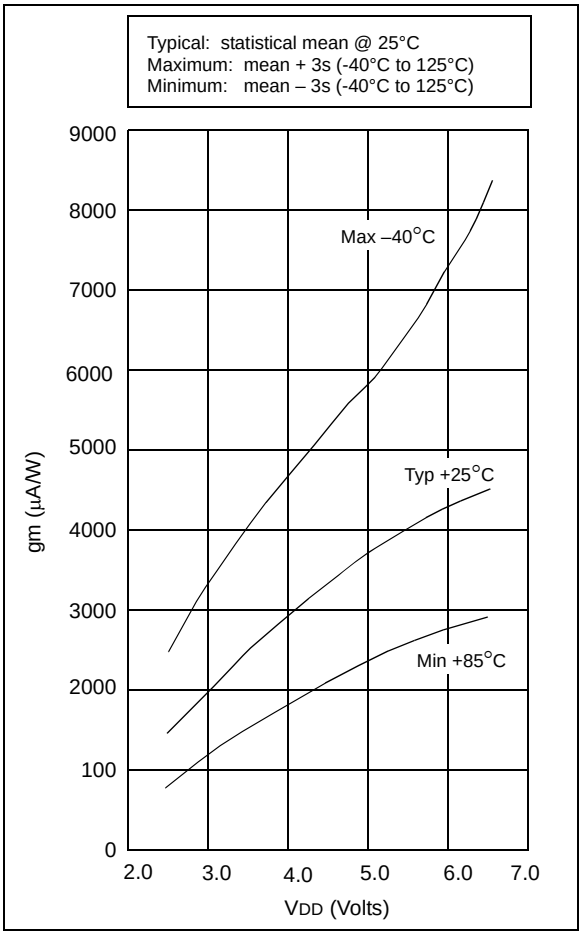
FIGURE 16-16: WDT TIMER TIME-OUT PERIOD vs. V_{DD} (1)



Note 1: Prescaler set to 1:1.

FIGURE 16-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. V_{DD}



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17.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial)
PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial)
PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial)
PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X **PIC16LCR5X** (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
PIC16C5X **PIC16CR5X** (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Symbol**	**Characteristic/Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**					
D001		PIC16LC5X	2.5 2.7 2.5	— — —	5.5 5.5 5.5	V V V	–40°C ≤ TA ≤ + 85°C, 16LCR5X –40°C ≤ TA ≤ 0°C, 16LC5X 0°C ≤ TA ≤ + 85°C 16LC5X
D001A		PIC16C5X	 3.0 4.5	 — —	 5.5 5.5	 V V	RC, XT, LP and HS mode from 0 - 10 MHz from 10 - 20 MHz
D002	VDR	**RAM Data Retention Voltage(1)**	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	**VDD Start Voltage** to ensure Power-on Reset	—	VSS	—	V	See Section 5.1 for details on Power-on Reset
D004	SVDD	**VDD Rise Rate** to ensure Power-on Reset	0.05*	—	—	V/ms	See Section 5.1 for details on Power-on Reset

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

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17.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

PIC16LC5X **PIC16LCR5X** (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
PIC16C5X **PIC16CR5X** (Commercial, Industrial)			**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Symbol**	**Characteristic/Device**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	IPD	**Power-down Current(2)**					
D020		PIC16LC5X	—	0.25	2	µA	VDD = 2.5V, WDT disabled, Commercial
			—	0.25	3	µA	VDD = 2.5V, WDT disabled, Industrial
			—	1	5	µA	VDD = 2.5V, WDT enabled, Commercial
			—	1.25	8	µA	VDD = 2.5V, WDT enabled, Industrial
D020A		PIC16C5X	—	0.25	4.0	µA	VDD = 3.0V, WDT disabled, Commercial
			—	0.25	5.0	µA	VDD = 3.0V, WDT disabled, Industrial
			—	1.8	7.0*	µA	VDD = 5.5V, WDT disabled, Commercial
			—	2.0	8.0*	µA	VDD = 5.5V, WDT disabled, Industrial
			—	4	12*	µA	VDD = 3.0V, WDT enabled, Commercial
			—	4	14*	µA	VDD = 3.0V, WDT enabled, Industrial
			—	9.8	27*	µA	VDD = 5.5V, WDT enabled, Commercial
			—	12	30*	µA	VDD = 5.5V, WDT enabled, Industrial

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

3: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

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FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF, 25°C

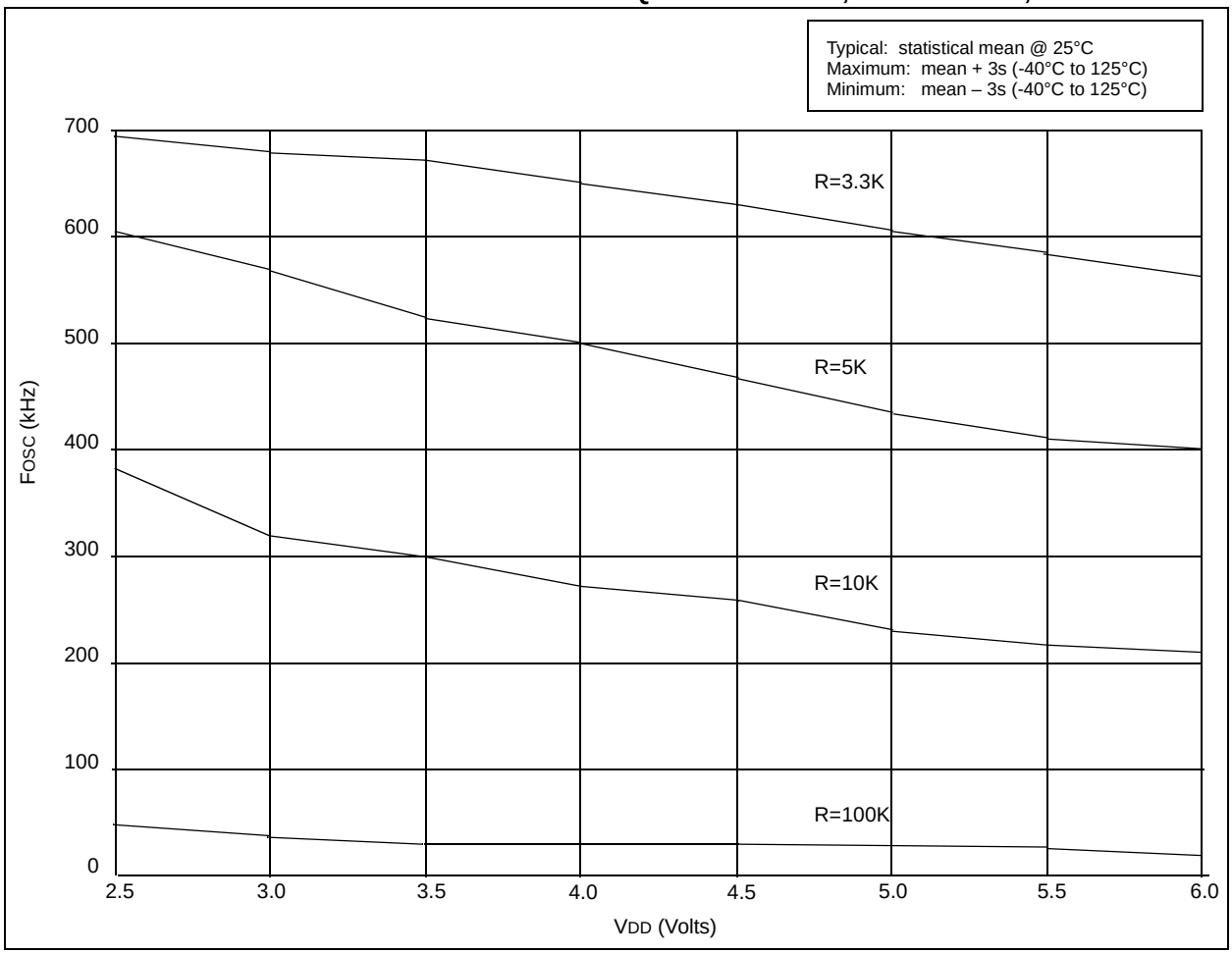


FIGURE 18-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)

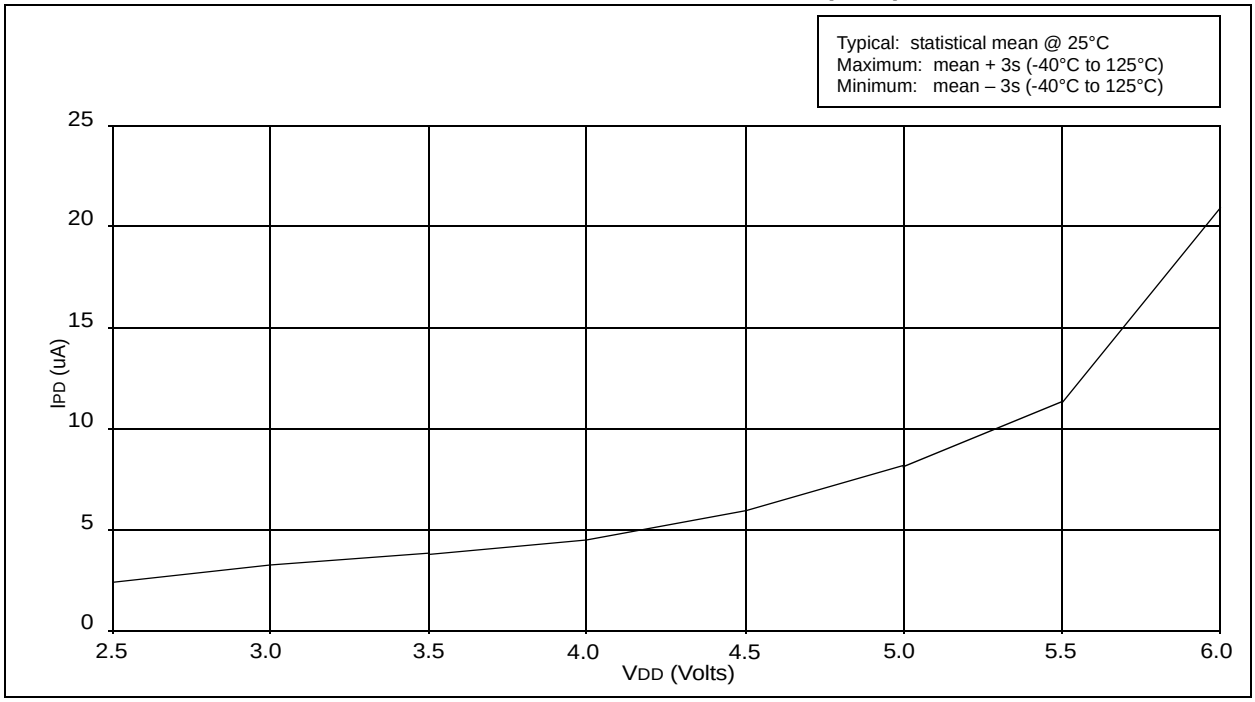


FIGURE 18-6: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (25°C)

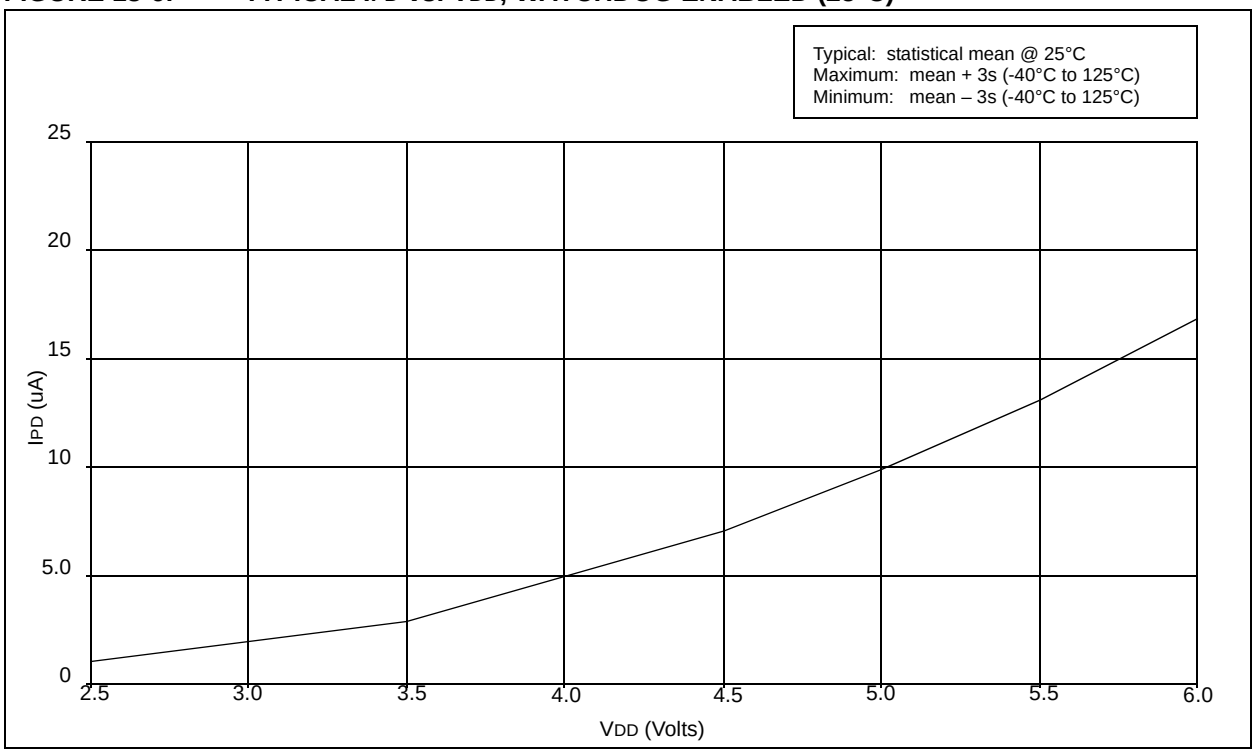
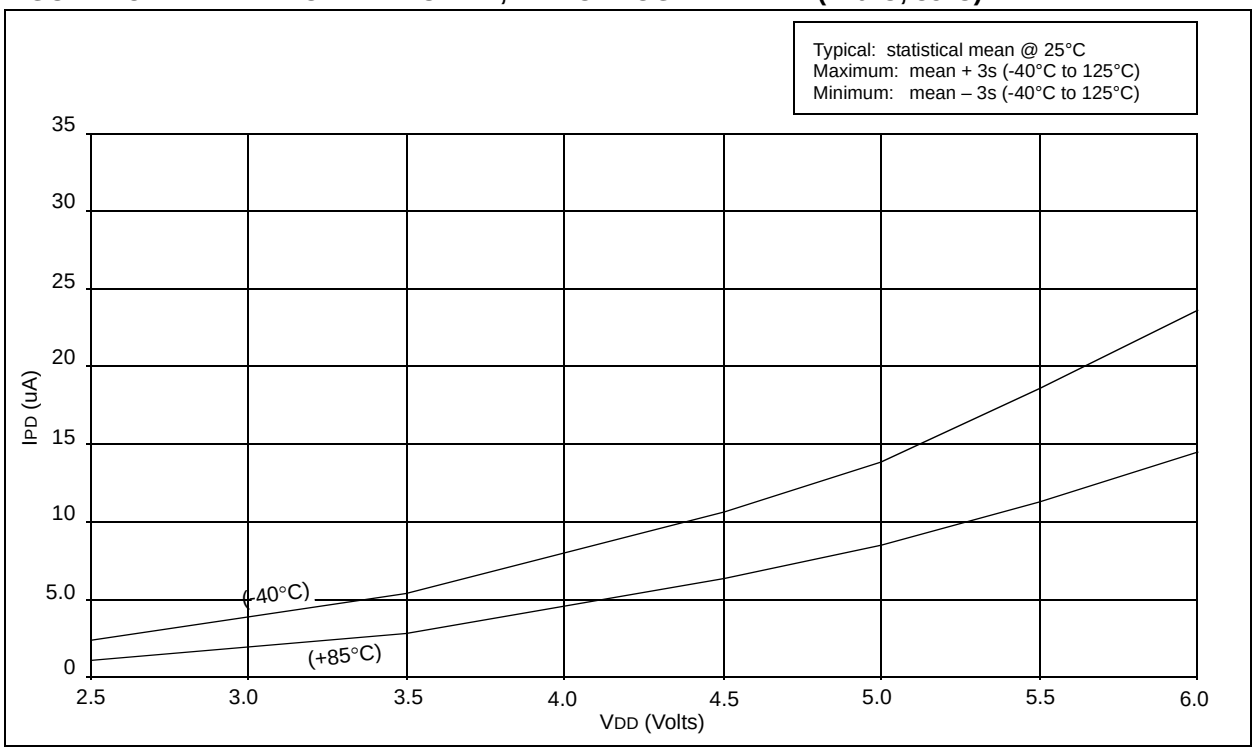


FIGURE 18-7: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (–40°C, 85°C)



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19.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)(1)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D030	VIL	**Input Low Voltage**					
		I/O Ports	VSS	—	0.8	V	4.5V <VDD ≤ 5.5V
		MCLR (Schmitt Trigger)	VSS	—	0.15 VDD	V	
		T0CKI (Schmitt Trigger)	VSS	—	0.15 VDD	V	
		OSC1	VSS	—	0.2 VDD	V	HS, 20 MHz ≤ FOSC ≤ 40 MHz
D040	VIH	**Input High Voltage**					
		I/O ports	2.0	—	VDD	V	4.5V < VDD ≤ 5.5V
		MCLR (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		T0CKI (Schmitt Trigger)	0.85 VDD	—	VDD	V	
		OSC1	0.8 VDD	—	VDD	V	HS, 20 MHz ≤ FOSC ≤ 40 MHz
D050	VHYS	**Hysteresis of Schmitt Trigger inputs**	0.15 VDD*	—	—	V	
D060	IIL	**Input Leakage Current(2,3)**					**For VDD ≤ 5.5V:**
		I/O ports	-1.0	0.5	+1.0	µA	VSS ≤ VPIN ≤ VDD, pin at hi-impedance
		MCLR	-5.0	—	+5.0	µA	VPIN = VSS +0.25V
		MCLR	—	0.5	+3.0	µA	VPIN = VDD
		T0CKI	-3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
		OSC1	-3.0	0.5	—	µA	VSS ≤ VPIN ≤ VDD, HS
D080	VOL	**Output Low Voltage**					
		I/O ports	—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
D090	VOH	**Output High Voltage(3)**					
		I/O ports	VDD - 0.7	—	—	V	IOH = -5.4 mA, VDD = 4.5V

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

Note 1: Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected and HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 17.3.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

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19.3 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T	
F Frequency	T Time

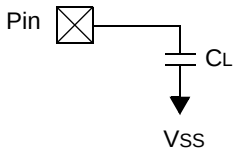
Lowercase letters (pp) and their meanings:

pp	
2 to	mc $\overline{\text{MCLR}}$
ck CLKOUT	osc oscillator
cy cycle time	os OSC1
drt device reset timer	t0 T0CKI
io I/O port	wdt watchdog timer

Uppercase letters and their meanings:

S	
F Fall	P Period
H High	R Rise
I Invalid (Hi-impedance)	V Valid
L Low	Z Hi-impedance

FIGURE 19-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54C/C55A/C56A/C57C/C58B-40



C_L = 50 pF for all pins except OSC2
0 pF for OSC2 in HS mode for operation between 20 MHz to 40 MHz

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