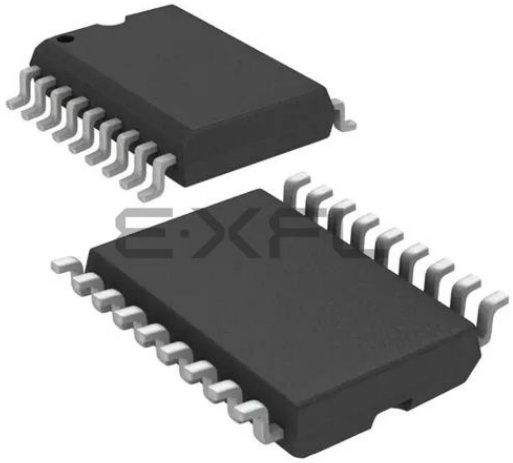

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	12
Program Memory Size	768B (512 x 12)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	25 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	18-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c54c-20i-so

NOTES:

TABLE 3-2: PINOUT DESCRIPTION - PIC16C55, PIC16C57, PIC16CR57

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	DIP	SOIC	SSOP			
RA0	6	6	5	I/O	TTL	Bi-directional I/O port
RA1	7	7	6	I/O	TTL	
RA2	8	8	7	I/O	TTL	
RA3	9	9	8	I/O	TTL	
RB0	10	10	9	I/O	TTL	Bi-directional I/O port
RB1	11	11	10	I/O	TTL	
RB2	12	12	11	I/O	TTL	
RB3	13	13	12	I/O	TTL	
RB4	14	14	13	I/O	TTL	
RB5	15	15	15	I/O	TTL	
RB6	16	16	16	I/O	TTL	
RB7	17	17	17	I/O	TTL	
RC0	18	18	18	I/O	TTL	Bi-directional I/O port
RC1	19	19	19	I/O	TTL	
RC2	20	20	20	I/O	TTL	
RC3	21	21	21	I/O	TTL	
RC4	22	22	22	I/O	TTL	
RC5	23	23	23	I/O	TTL	
RC6	24	24	24	I/O	TTL	
RC7	25	25	25	I/O	TTL	
T0CKI	1	1	2	I	ST	Clock input to Timer0. Must be tied to V_{SS} or V_{DD}, if not in use, to reduce current consumption.
$\overline{MCLR}$	28	28	28	I	ST	Master clear (RESET) input. This pin is an active low RESET to the device.
OSC1/CLKIN	27	27	27	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	26	26	26	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
V_{DD}	2	2	3,4	P	—	Positive supply for logic and I/O pins.
V_{SS}	4	4	1,14	P	—	Ground reference for logic and I/O pins.
N/C	3,5	3,5	—	—	—	Unused, do not connect.

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the MCLR/VPP pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is RESET. The DRT timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where MCLR is not tied to VDD is shown in Figure 5-3. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset TDRT msec after MCLR goes high.

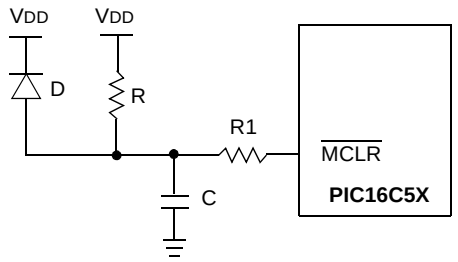
In Figure 5-4, the on-chip Power-On Reset feature is being used (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the MCLR/VPP pin, and when the MCLR/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

Note:	When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the Embedded Control Handbook.

The POR circuit does not produce an internal RESET when VDD declines.

FIGURE 5-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

7.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., MOVF PORTB,W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

7.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used (RA<3:0>). Bits 7-4 are unimplemented and read as '0's.

7.2 PORTB

PORTB is an 8-bit I/O Register (PORTB<7:0>).

7.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58 and PIC16CR58.

7.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the TRIS f instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

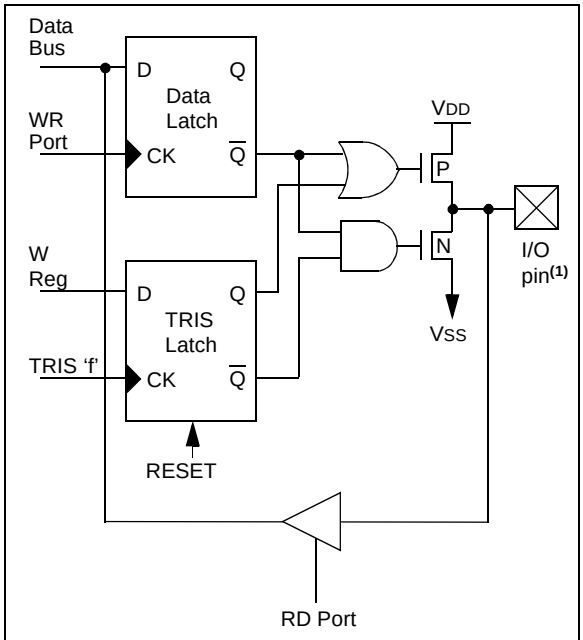
Note:	A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

7.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 7-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

FIGURE 7-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



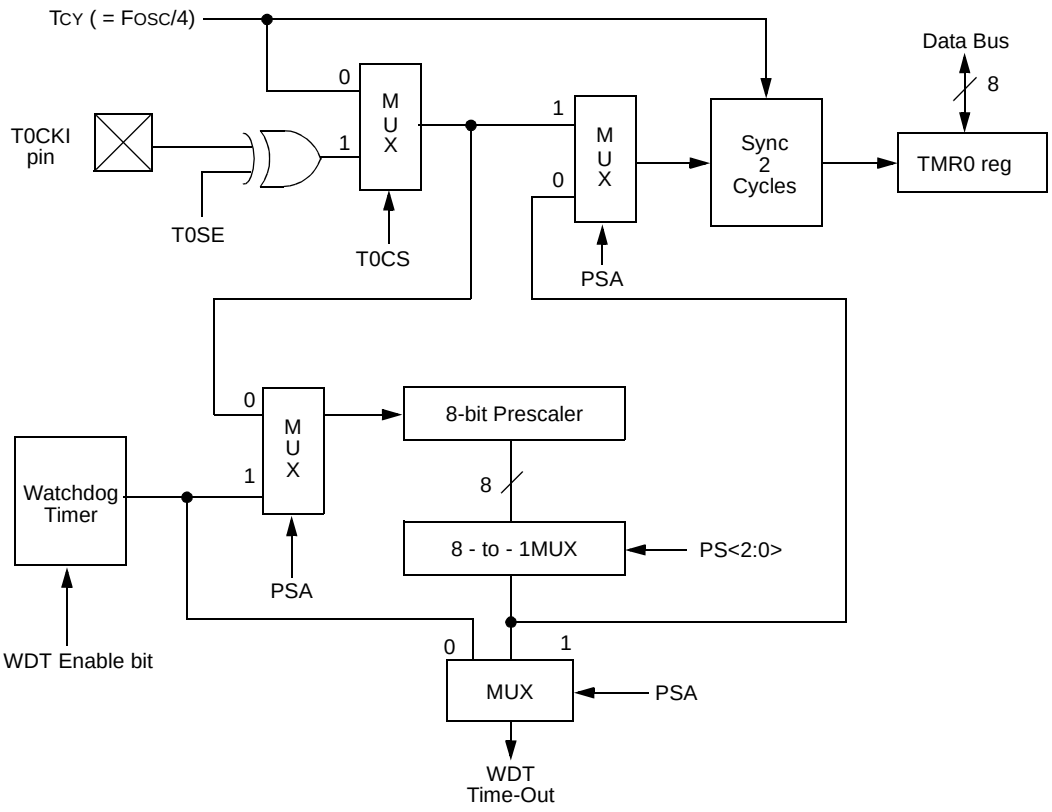
Note 1: I/O pins have protection diodes to VDD and VSS.

TABLE 7-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	TRIS	I/O Control Registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'

FIGURE 8-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

ADDWF **Add W and f**

Syntax: [*label*] ADDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

0001	11df	ffff

Description: Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ADDWF  TEMP_REG, 0
```
Before Instruction
W = 0x17
TEMP_REG = 0xC2
After Instruction
W = 0xD9
TEMP_REG = 0xC2

ANDWF **AND W with f**

Syntax: [*label*] ANDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) .AND. (f) → (dest)

Status Affected: Z

Encoding:

0001	01df	ffff

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ANDWF  TEMP_REG, 1
```
Before Instruction
W = 0x17
TEMP_REG = 0xC2
After Instruction
W = 0x17
TEMP_REG = 0x02

ANDLW **AND literal with W**

Syntax: [*label*] ANDLW k

Operands: $0 \le k \le 255$

Operation: (W).AND. (k) → (W)

Status Affected: Z

Encoding:

1110	kkkk	kkkk

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ANDLW  H'5F'
```
Before Instruction
W = 0xA3
After Instruction
W = 0x03

BCF **Bit Clear f**

Syntax: [*label*] BCF f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: 0 → (f<b>)

Status Affected: None

Encoding:

0100	bbbf	ffff

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example:
```
BCF    FLAG_REG,  7
```
Before Instruction
FLAG_REG = 0xC7
After Instruction
FLAG_REG = 0x47

COMF **Complement f**

Syntax: [*label*] COMF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(\bar{f}) \rightarrow (dest)$

Status Affected: Z

Encoding:

0010	01df	ffff

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
COMF   REG1,0
```
Before Instruction
REG1 = 0x13
After Instruction
REG1 = 0x13
W = 0xEC

DECF **Decrement f**

Syntax: [*label*] DECF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – 1 → (dest)

Status Affected: Z

Encoding:

0000	11df	ffff

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
DECF    CNT, 1
```
Before Instruction
CNT = 0x01
Z = 0
After Instruction
CNT = 0x00
Z = 1

DECFSZ **Decrement f, Skip if 0**

Syntax: [*label*] DECFSZ f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – 1 → d; skip if result = 0

Status Affected: None

Encoding:

0010	11df	ffff

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE      DECFSZ   CNT, 1
          GOTO     LOOP
CONTINUE  •
          •
          •
```
Before Instruction
PC = address (HERE)
After Instruction
CNT = CNT - 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT ≠ 0,
PC = address (HERE+1)

IORLW **Inclusive OR literal with W**

Syntax: [*label*] IORLW k

Operands: $0 \le k \le 255$

Operation: (W) .OR. (k) → (W)

Status Affected: Z

Encoding:

1101	kkkk	kkkk

Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
IORLW  0x35
```
Before Instruction
W = 0x9A
After Instruction
W = 0xBF
Z = 0

IORWF **Inclusive OR W with f**

Syntax: [*label*] IORWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W).OR. (f) → (dest)

Status Affected: Z

Encoding:

0001	00df	ffff

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example:
```
IORWF          RESULT, 0
```
Before Instruction
RESULT = 0x13
W = 0x91
After Instruction
RESULT = 0x13
W = 0x93
Z = 0

MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Encoding:

0010	00df	ffff

Description: The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example:
```
MOVF   FSR,   0
```
After Instruction
W = value in FSR register

MOVLW **Move Literal to W**

Syntax: [*label*] MOVLW k

Operands: $0 \le k \le 255$

Operation: k → (W)

Status Affected: None

Encoding:

1100	kkkk	kkkk

Description: The eight bit literal 'k' is loaded into the W register.

Words: 1

Cycles: 1

Example:
```
MOVLW  0x5A
```
After Instruction
W = 0x5A

12.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings(†)

Ambient Temperature under bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} .....0V to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS}(1) .....0V to +14V

Voltage on all other pins with respect to V_{SS} .....–0.6V to (V_{DD} + 0.6V)

Total power dissipation(2) ..... 800 mW

Max. current out of V_{SS} pin ..... 150 mA

Max. current into V_{DD} pin ..... 100 mA

Max. current into an input pin (T0CKI only)..... ±500 μA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Max. output current sunk by any I/O pin ..... 25 mA

Max. output current sourced by any I/O pin ..... 20 mA

Max. output current sourced by a single I/O port (PORTA, B or C) ..... 40 mA

Max. output current sunk by a single I/O port (PORTA, B or C)..... 50 mA

Note 1: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

2: Power Dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

12.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T	
F Frequency	T Time

Lowercase letters (pp) and their meanings:

pp	
2 to	mc $\overline{\text{MCLR}}$
ck CLKOUT	osc oscillator
cy cycle time	os OSC1
drt device reset timer	t0 T0CKI
io I/O port	wdt watchdog timer

Uppercase letters and their meanings:

S	
F Fall	P Period
H High	R Rise
I Invalid (Hi-impedance)	V Valid
L Low	Z Hi-impedance

FIGURE 12-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54/55/56/57

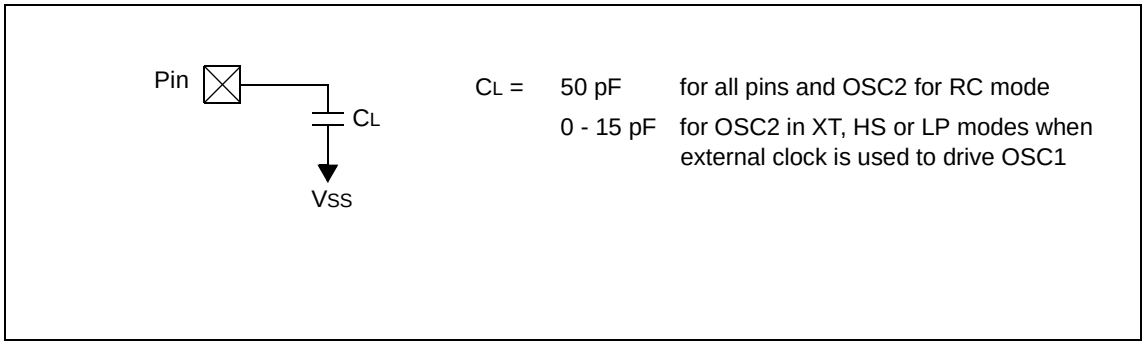
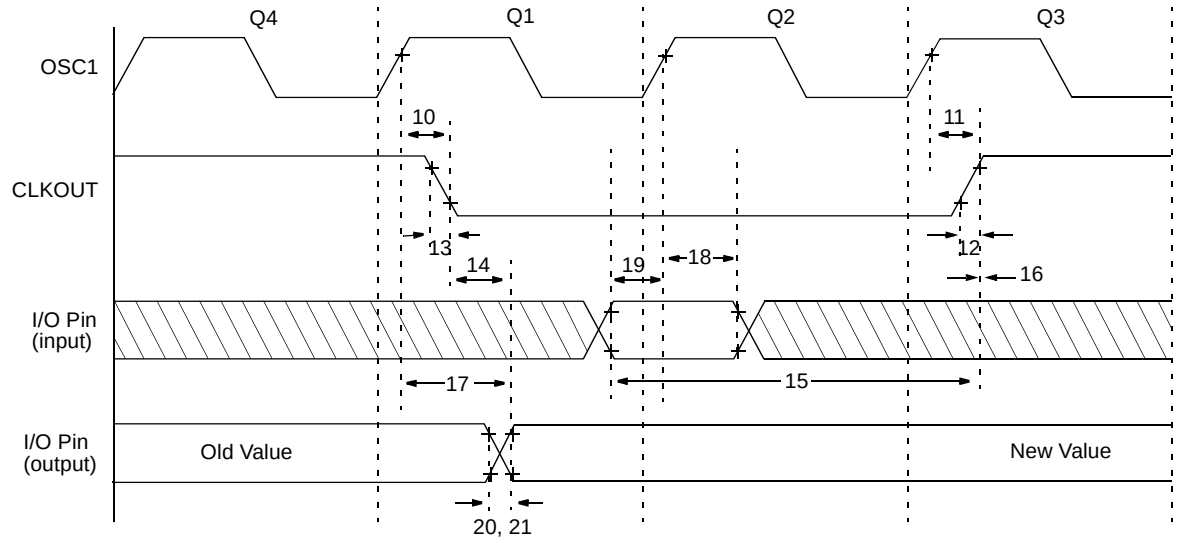


FIGURE 12-3: CLKOUT AND I/O TIMING - PIC16C54/55/56/57



Note: Please refer to Figure 12-1 for load conditions.

TABLE 12-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial –40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓(1)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(1)	—	15	30**	ns
12	TckR	CLKOUT rise time(1)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(1)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(1)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(1)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(1)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(2)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(2)	—	10	25**	ns
21	TioF	Port output fall time(2)	—	10	25**	ns

* These parameters are characterized but not tested.

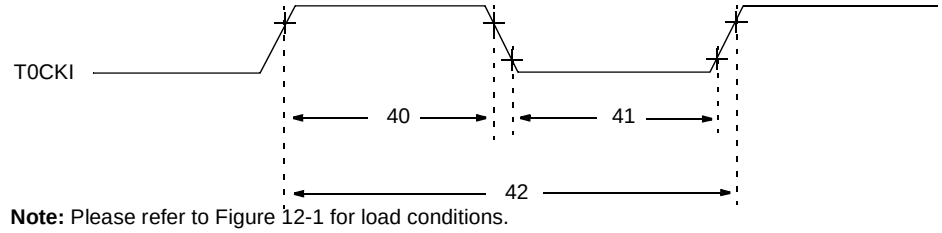
** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

2: Please refer to Figure 12-1 for load conditions.

FIGURE 12-5: TIMER0 CLOCK TIMINGS - PIC16C54/55/56/57



Note: Please refer to Figure 12-1 for load conditions.

TABLE 12-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial –40°C ≤ TA ≤ +125°C for extended					
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 14-19: PORTA, B AND C I_{OH} vs. V_{OH}, V_{DD} = 3 V

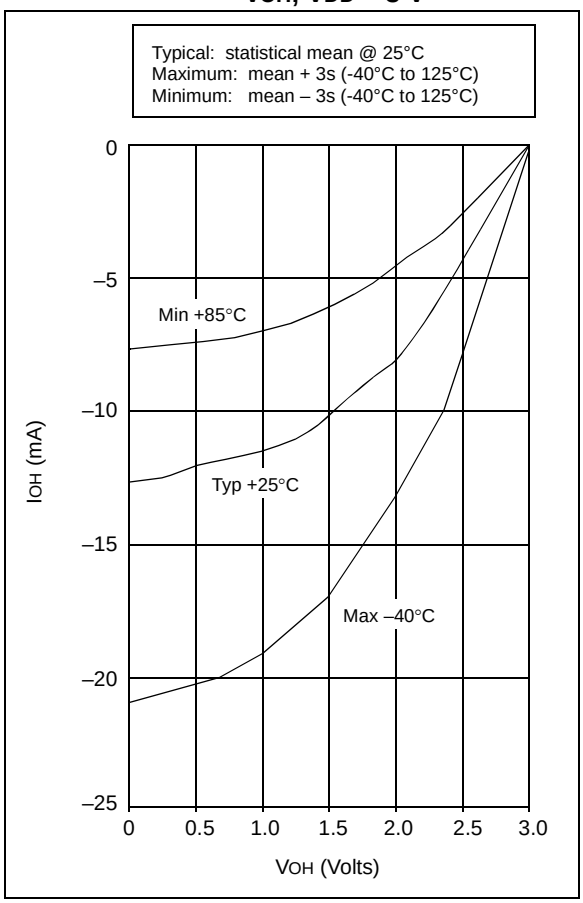


FIGURE 14-20: PORTA, B AND C I_{OH} vs. V_{OH}, V_{DD} = 5 V

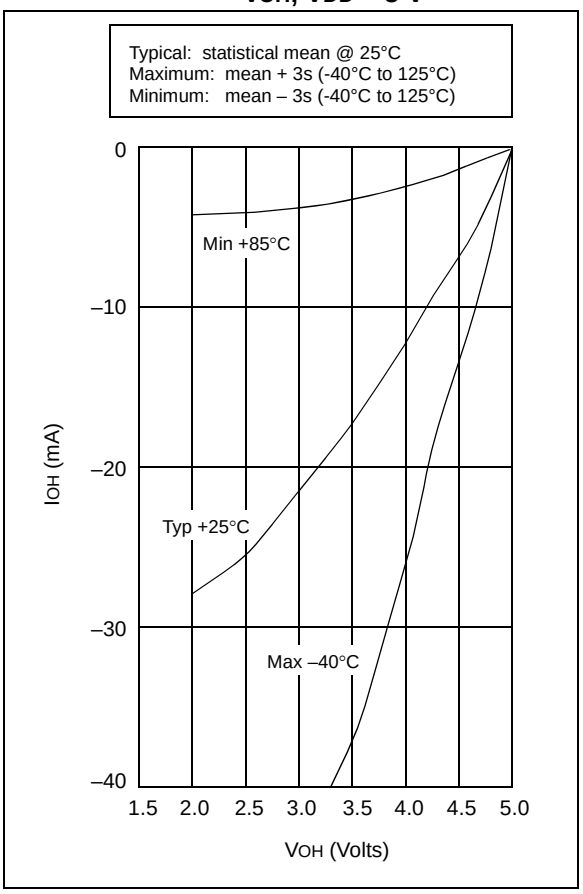
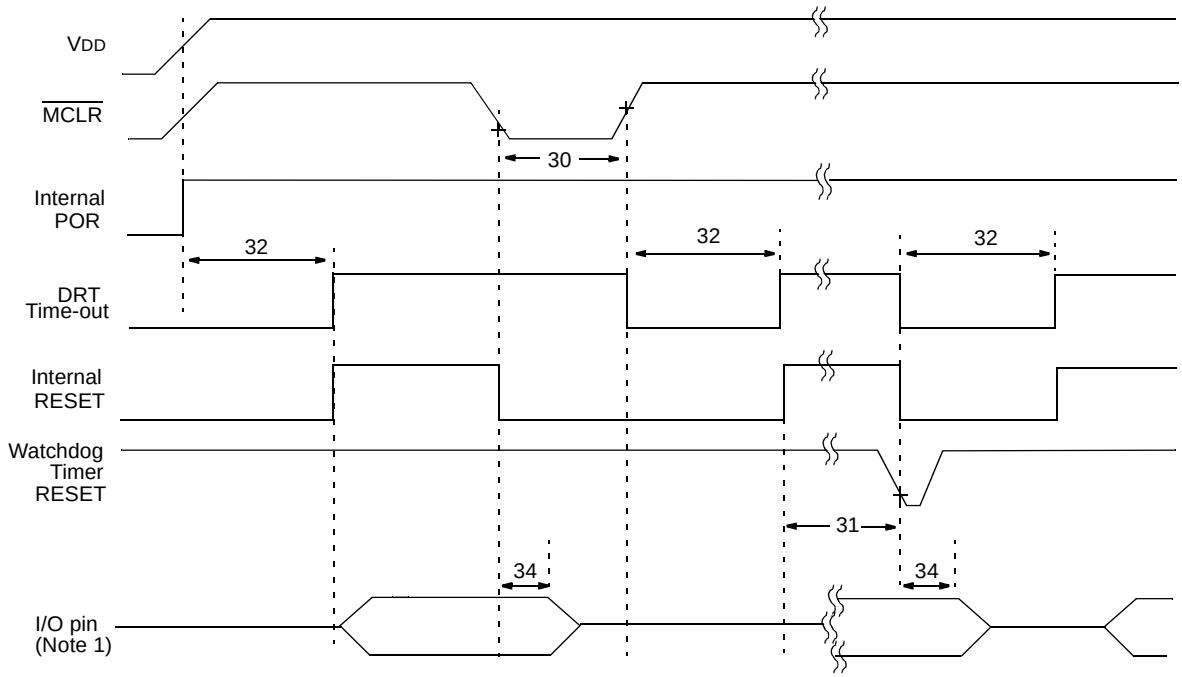


FIGURE 15-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A



Note 1: Please refer to Figure 15-1 for load conditions.

TABLE 15-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial –40°C ≤ TA ≤ +85°C for industrial –20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I –40°C ≤ TA ≤ +125°C for extended						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	100* 1	— —	— —	ns µs	VDD = 5.0V VDD = 5.0V (PIC16LV54A only)
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Comm)
34	Tioz	I/O Hi-impedance from $\overline{MCLR}$ Low	— —	— —	100* 1µs	ns —	 (PIC16LV54A only)

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 16-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF, 25°C

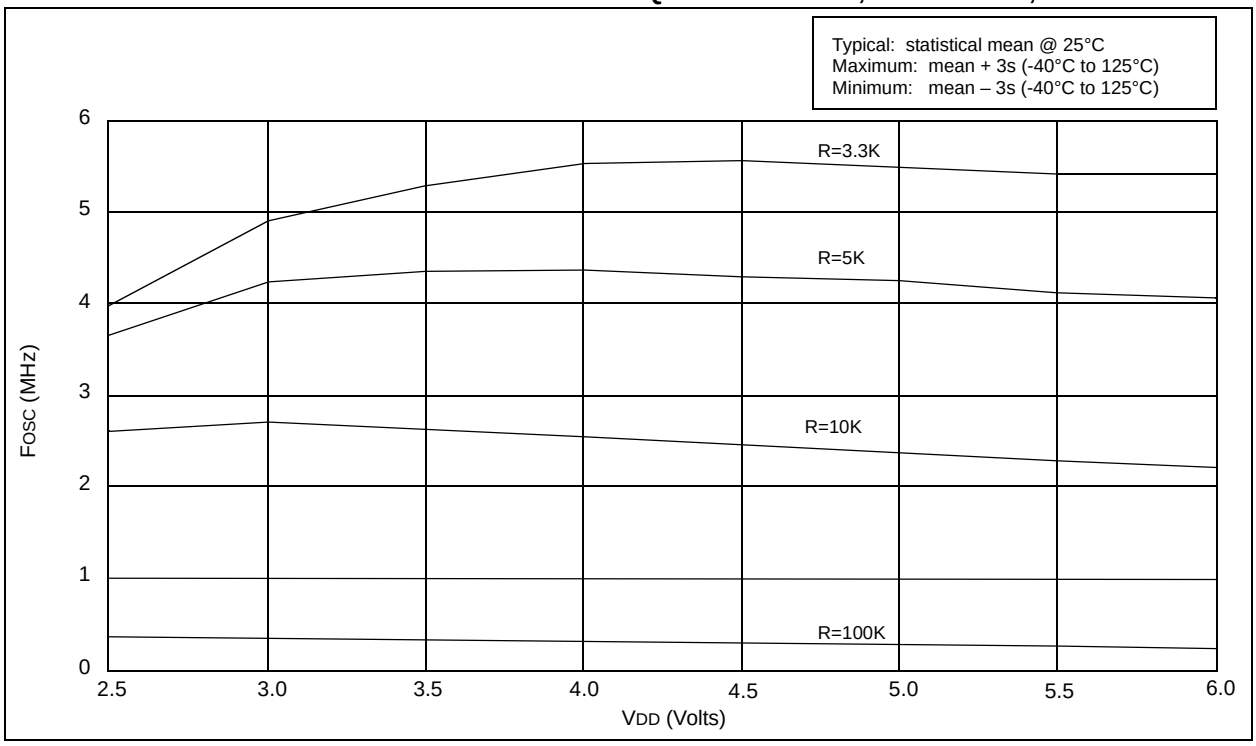


FIGURE 16-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF, 25°C

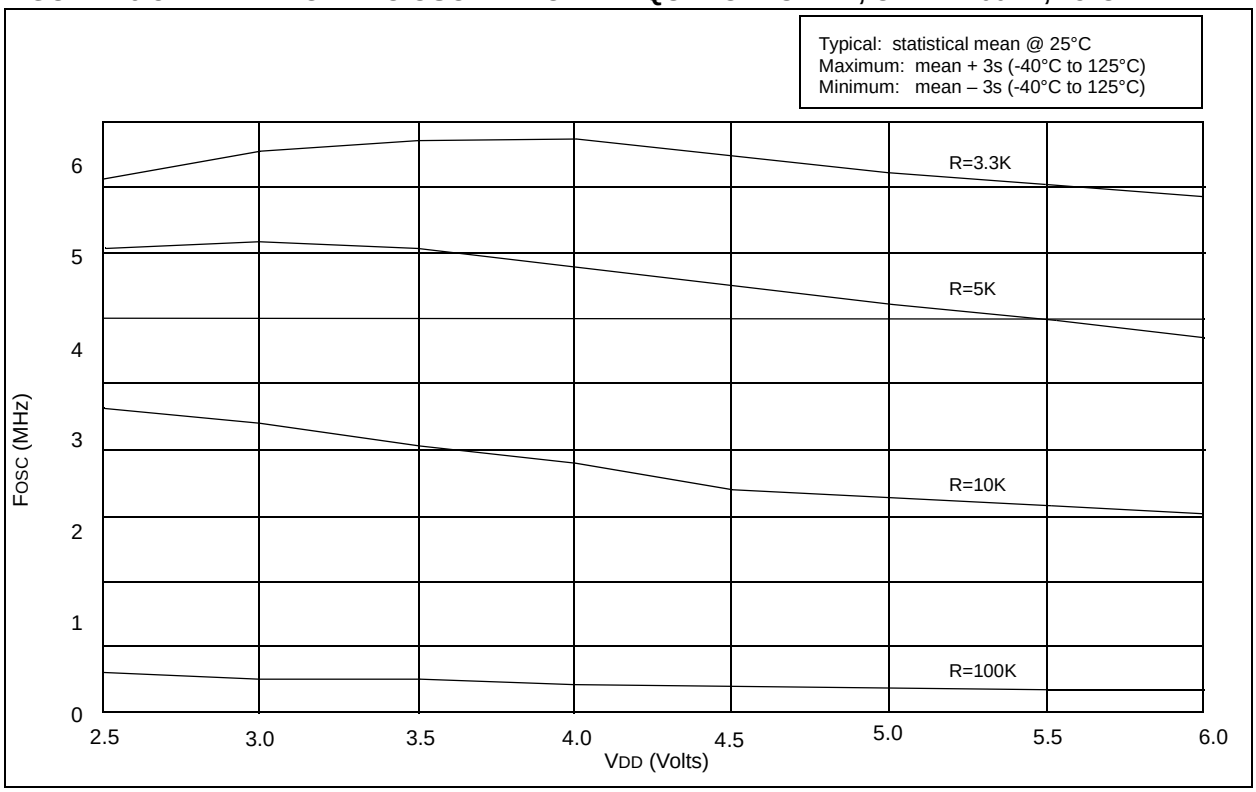


FIGURE 16-12: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, 25°C)

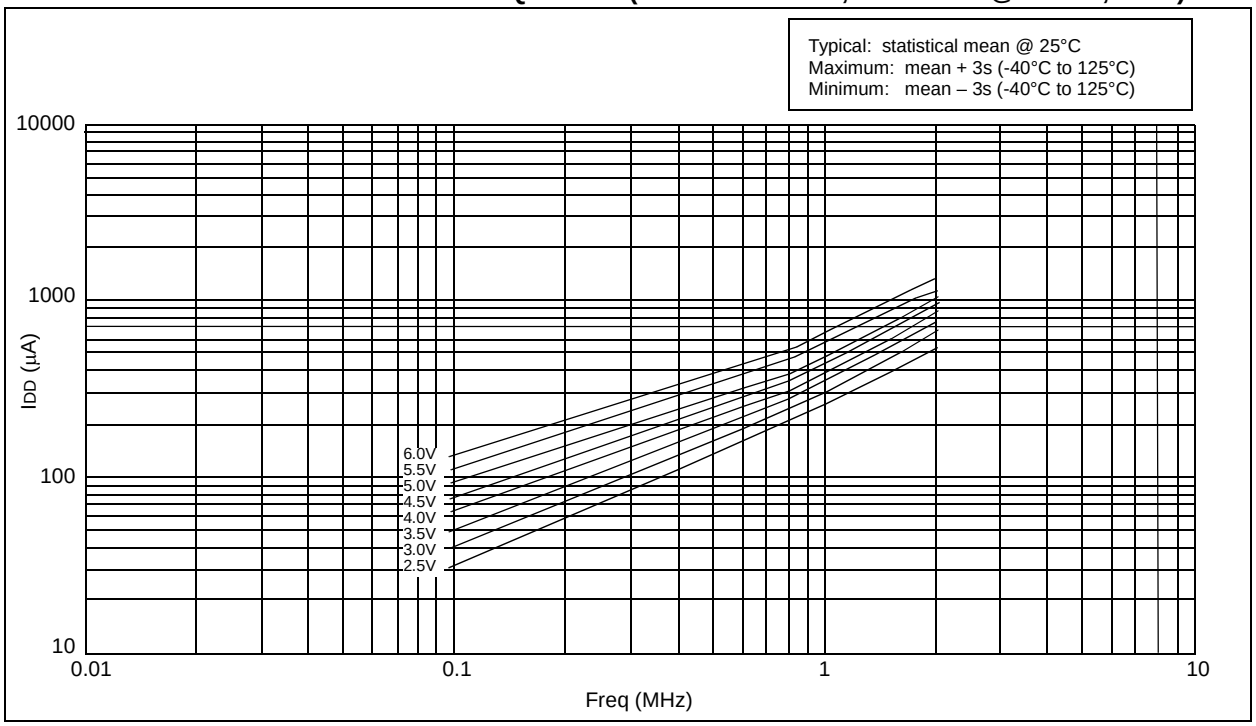


FIGURE 16-13: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, –40°C to +85°C)

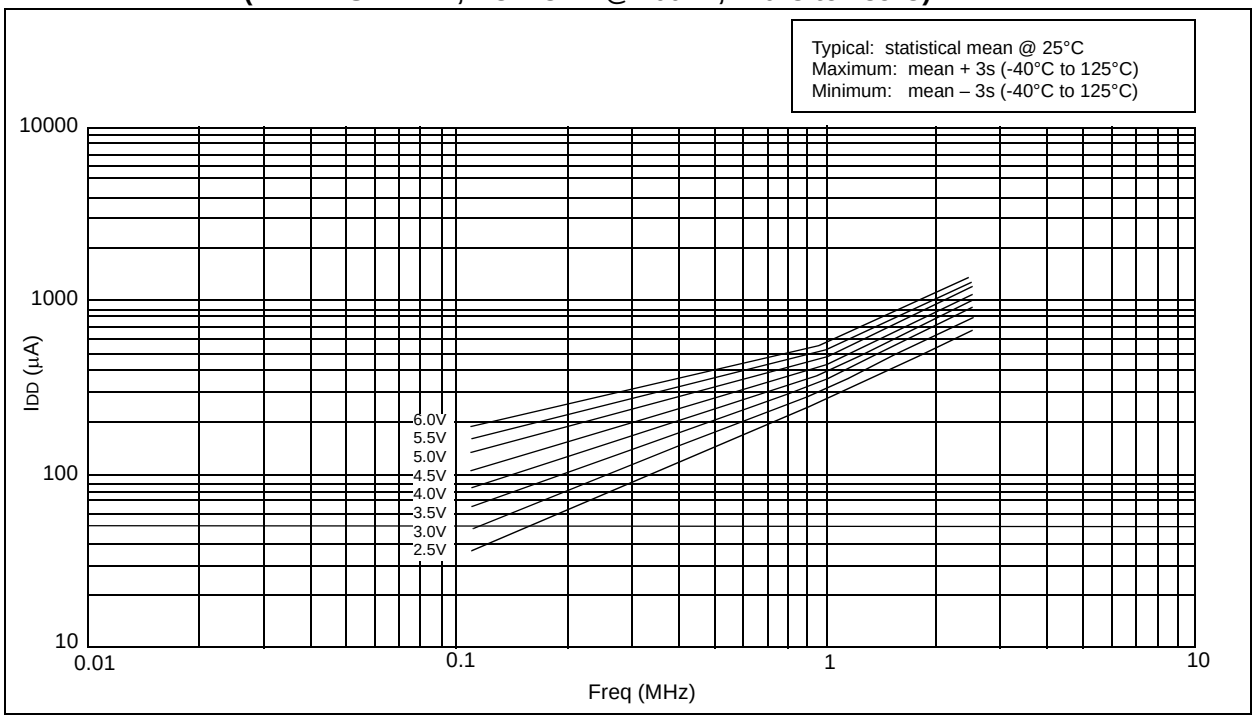


FIGURE 20-2: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (25°C)

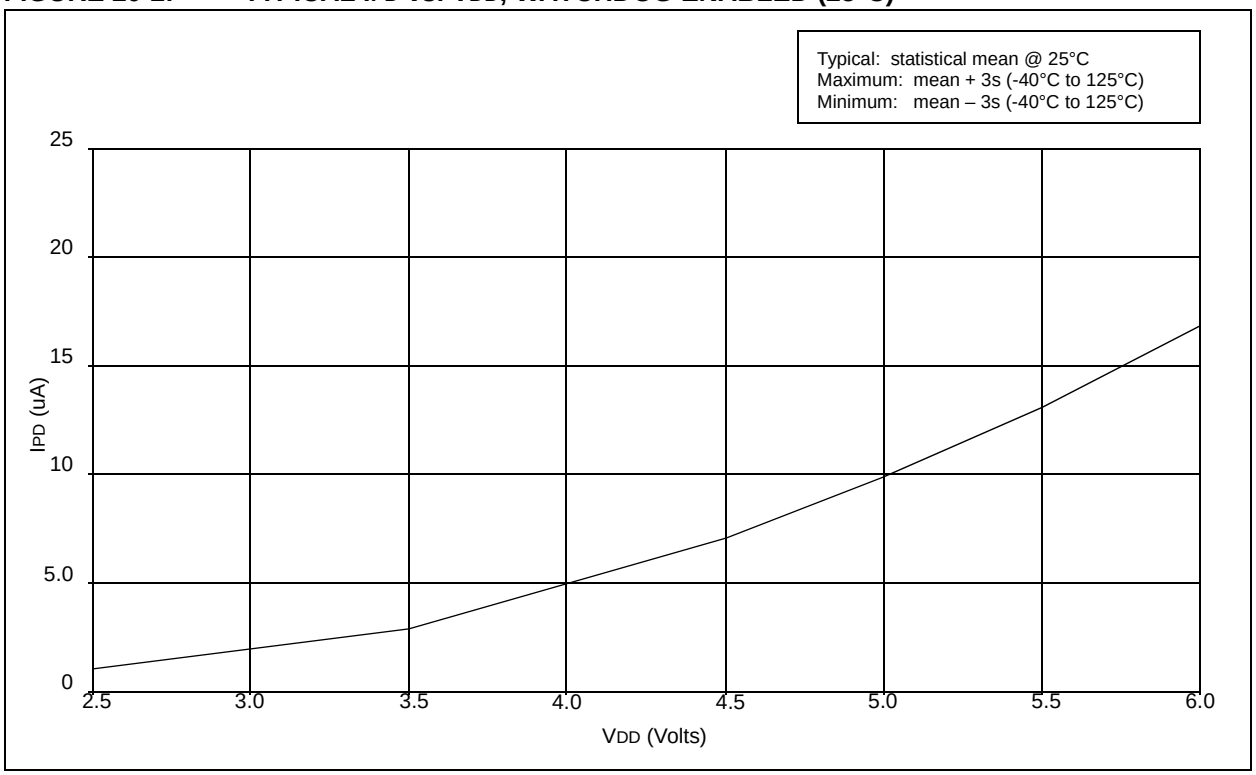


FIGURE 20-3: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (–40°C, 85°C)

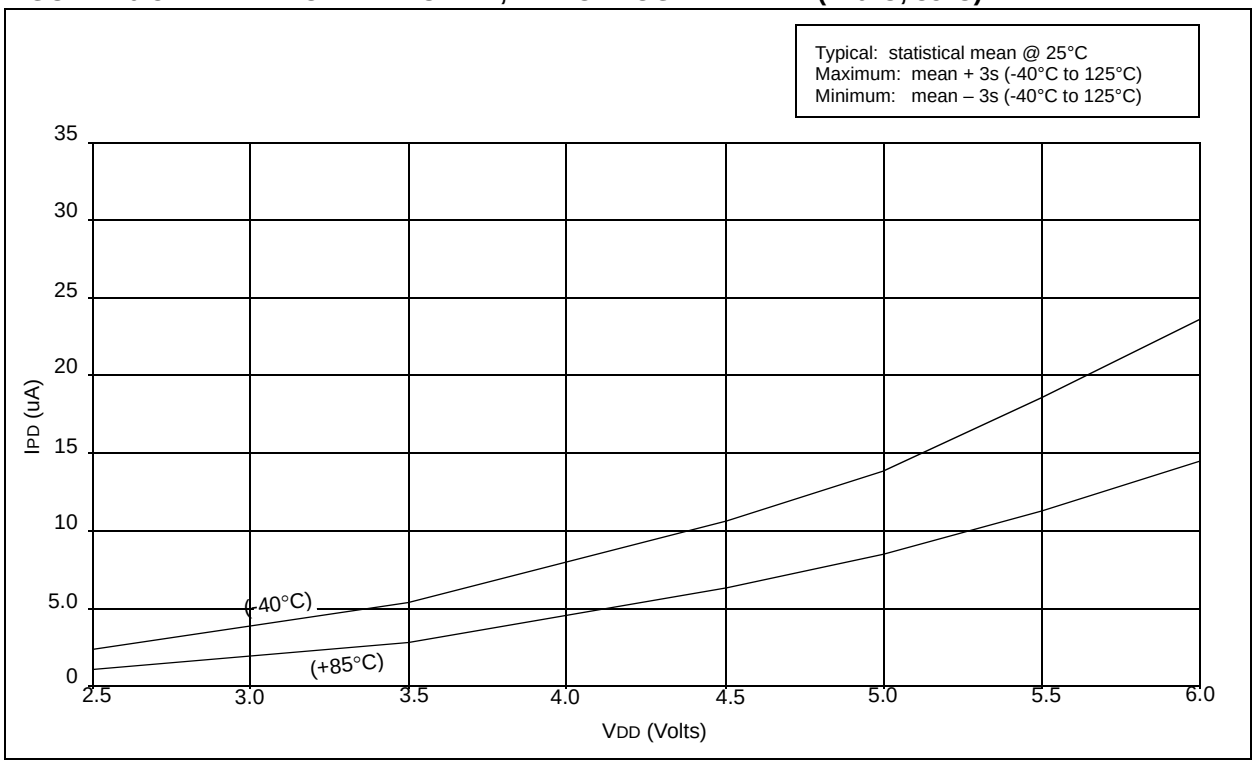


FIGURE 20-4: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. VDD

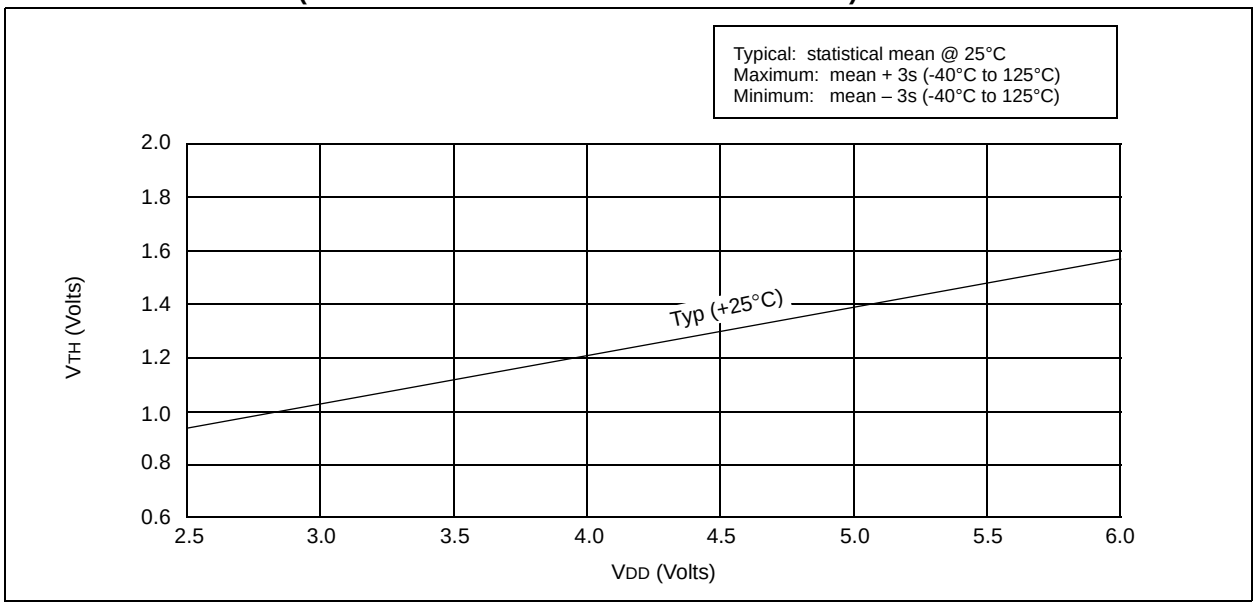
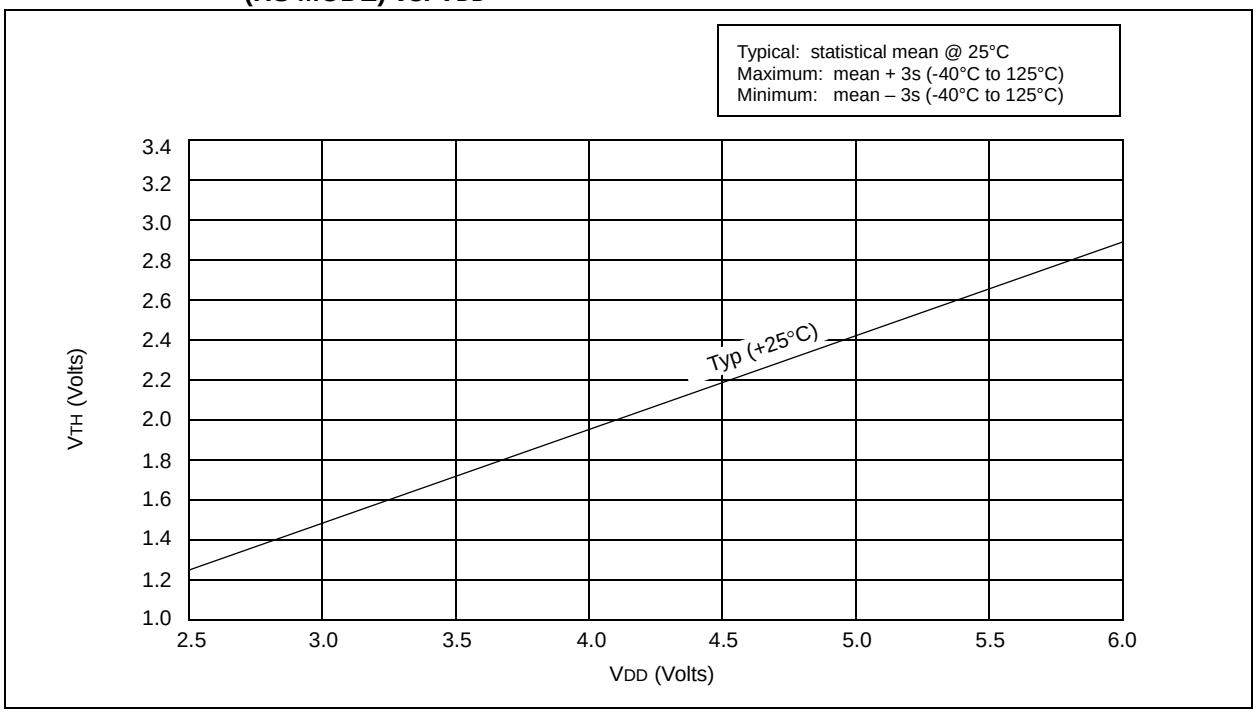


FIGURE 20-5: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (HS MODE) vs. VDD



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